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RBAN TRAFFIC CONTROL AND BUS RIORITY SYSTEM SOFTWARE MANUAL

Vol. I. Functional Description and Flow Charts

NOV 7 1977

June 1976
Final Report Revision C

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16. Abstract

An Urban Traffic Control and Bus Priority System has been implemented by the Sperry Systems Management Division in the District of Columbia under Federal Highway Administration contract No. FH-11-7605, Advanced Control Technology in Urban Traffic Control Systems - Installation. The system includes on-street surveillance and control elements and a central office data processing facility. This manual describes the software for this system. This is Volume I of 2 volumes which comprise the UTCS/BPS Software Manual. It contains Section 1, Introduction and Section 2, Programming Specifications.

The other report of this pair is:

Report FHWA-RD-76-186 Vol. II
UTCS/BPS Software Manual - Variable Definitions; Algorithm and Off-line Software Descriptions.
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Report FHWA-RD-76-182 Addenda to Urban Traffic Control and Bus Priority System Software Manual For UTCS/CIC, UTCS/MGVD, and UTCS/PBPS.
Report FHWA-RD-73-9 UTCS/BPS Design and Installation
Report FHWA-RD-76-183 UTCS/BPS Operator's Manual
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SOFTWARE MANUAL

(Pub. No. GF-16-1003)

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FOREWORD

An Urban Traffic Control and Bus Priority System has been implemented by the Sperry Systems Management Division in the District of Columbia under Federal Highway Administration contract No. FH-11-7605, Advanced Control Technology in Urban Traffic Control Systems - Installation. The system includes on-street surveillance and control elements and a central office data processing facility. This manual describes the software for this system. The manual is composed of the following volumes:

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	Section 2	Programming Specifications
Volume II	Section 3	Glossary
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1. Introduction

The purpose of the software manual is to provide documentation that will be of use to systems and programming oriented personnel. The systems analyst will find useful information in Sections 1, 2, 3, and 4. Section 1 contains generalized information consisting of the organization of the Urban Traffic Control System (UTCS) and Bus Priority System (BPS), Central Processing Unit (CPU) functions, a description of the UTCS/BPS data processing equipment, the software operating system used, the priority interrupt system, input/output, and entry and working storage for pattern changes. Section 2 contains the programming specifications for each of the routines. These specifications contain five subsections describing the purpose, method, repetition rate, cross reference and flow chart. The flow charts contain detailed functional information and equations for use by the systems analyst. Section 3 contains the glossary which define each symbol referenced on the flow charts and Section 4 contains appendices. The appendices useful to the systems analyst are the ones containing the UTCS and BPS traffic algorithms. The programmer will find useful information in all sections of this manual. In addition to the functional information on the flow charts, the programmer will find detailed coding data. Section 5 contains listings of all the assembled routines and a listing of the SYSGEN. The computer manufacturer's documentation is also listed in the appendices.

The UTCS/BPS software was constructed around Xerox Data Systems (XDS) Real-Time Batch Monitor (RBM) operating system and programmed in its entirety in their symbolic assembly language (Macro-Symbol). RBM and Macro-Symbol are adequately described in XDS's documentation listed in Section 4.10. However, in order to fully understand the UTCS/BPS software, the reader should familiarize himself with RBM, Macro-Symbol and XDS's Sigma 5 hardware/software architecture. A description of the data processing equipment used by the UTCS/BPS system is contained in Section 1.3.

1.1 Organization of UTCS CPU Functions

The UTCS computer routines are organized in accordance with the frequency at which various functions are required to be performed. The UTCS Executive Routine controls the sequence by which other UTCS cyclical routines are performed in accordance with pre-defined assignments of priority and elapsed time. Functions that are performed 32 times per second are specified in routines that are assigned to Priority Level 1. Priority Level 2 routines are those that are entered twice per second. All the remaining routines except the Start-Up Routine are assigned to Priority Level 3. The Start-Up Routine is not assigned to a priority level.

The timing for the UTCS Executive Routine is controlled by an internal clock which causes a program interrupt 32 times per second. When the interrupt occurs, any routine in progress is suspended and control is given to the UTCS Executive Routine which performs all multiplexer (MUX) input/output (I/O), triggers an interprocessor interrupt for timing in the BPS CPU and executes the UTCS Level 1 routines. When a half-second mark is encountered, the UTCS Executive Routine causes the Priority Level 2 routines to be performed. At the completion of Priority Level 1 and Priority Level 2 (if on the half second), the UTCS Executive Routine allows the Priority Level 3 routines to be resumed from the point at which they had been interrupted. If the Priority Level 3 routines are completed before Level 1 is scheduled to start again, the system is returned to the Monitor. The Monitor is a program that supervises the processing, loading and execution of other programs. Refer to Section 1.4 for further details.

The routines are identified by letters (A to Y), but these designations do not signify any particular relationship or sequence of operation. The over-all flow charts, Figures 1.1, 1.2 and 1.3, show how the routines are inter-related.

Priority Level 1

Priority Level 1 routines embody those functions which are directly associated with the measurement of vehicular traffic and executive control. The sequence of non-executive type functions performed at this level is illustrated by Figure 1.1.

Executive, Routine A

The Executive Routine controls the sequence by which other routines are performed in accordance with pre-defined assignments of priority and elapsed time. In addition, the Executive Routine reads in vehicle presence data from the detectors, A-Phase Green Return data from the controllers, switch configuration data from the traffic control panel, and master synchronization pulse data from the district's radio link. The Executive Routine puts out controller advance and hold pulses and sends signals to the traffic control panel and map display. The timing and control of data transmission between the UTCS and the BPS computers is also maintained by the Executive Routine.

Detector Data Input and Interpretation, Routine B

The Detector Data Input and Interpretation Routine samples the output of each detector for an indication of vehicle presence. From this, the routine determines the beginning and end times of each vehicle passage. Whenever an end of vehicle is sensed, the Once per Vehicle Routine is called.

Once per Vehicle, Routine C

The Once per Vehicle Routine accumulates raw volume, raw speed and occupancy data, updates zone count for those lanes that are instrumented with more than one detector, and sets flags for timing the computation of stops.

Priority Level 2

The Priority Level 2 routines are primarily those associated with controller commands, error checking, and data evaluation. The routines that comprise Priority Level 2 and their relationships are illustrated by Figure 1.2. Central to the Priority Level 2 functions is a sequence of routines performed for each controller. These routines, which are included in the "Do-Loop" in Figure 1.2, provide the functions of sequencing the controller through its cycle, placing it on or off line as desired, and adjusting split and offset in accordance with traffic volumes or operator commands. Other Level 2 routines provide error checking for each controller, controller cycle time keeping, data computation, and the operation of semi-actuated controllers.

Traffic Cycle Time Keeping, Routine N

This routine maintains the time elapsed since the start of a controller cycle for all possible cycle lengths that can be selected for on-street use. When the end of one of the cycles is reached, a flag is set for that cycle for use by other routines, and the cycle elapsed time count is set to zero.

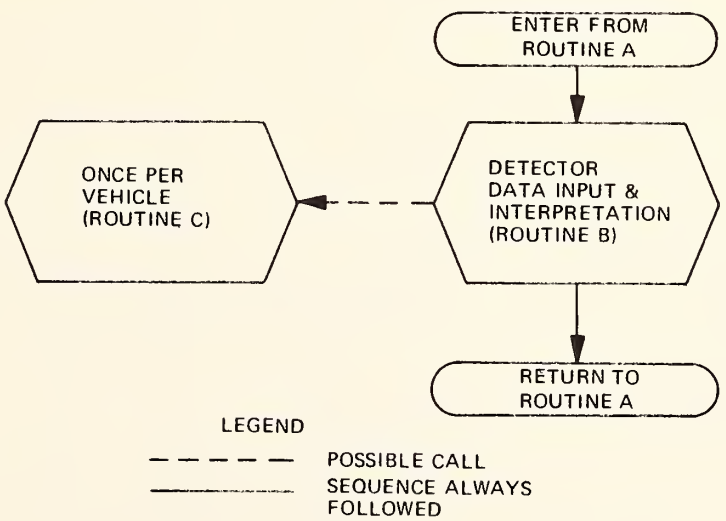


FIGURE 1.1 UTCS NON-EXECUTIVE PRIORITY LEVEL ONE ROUTINES

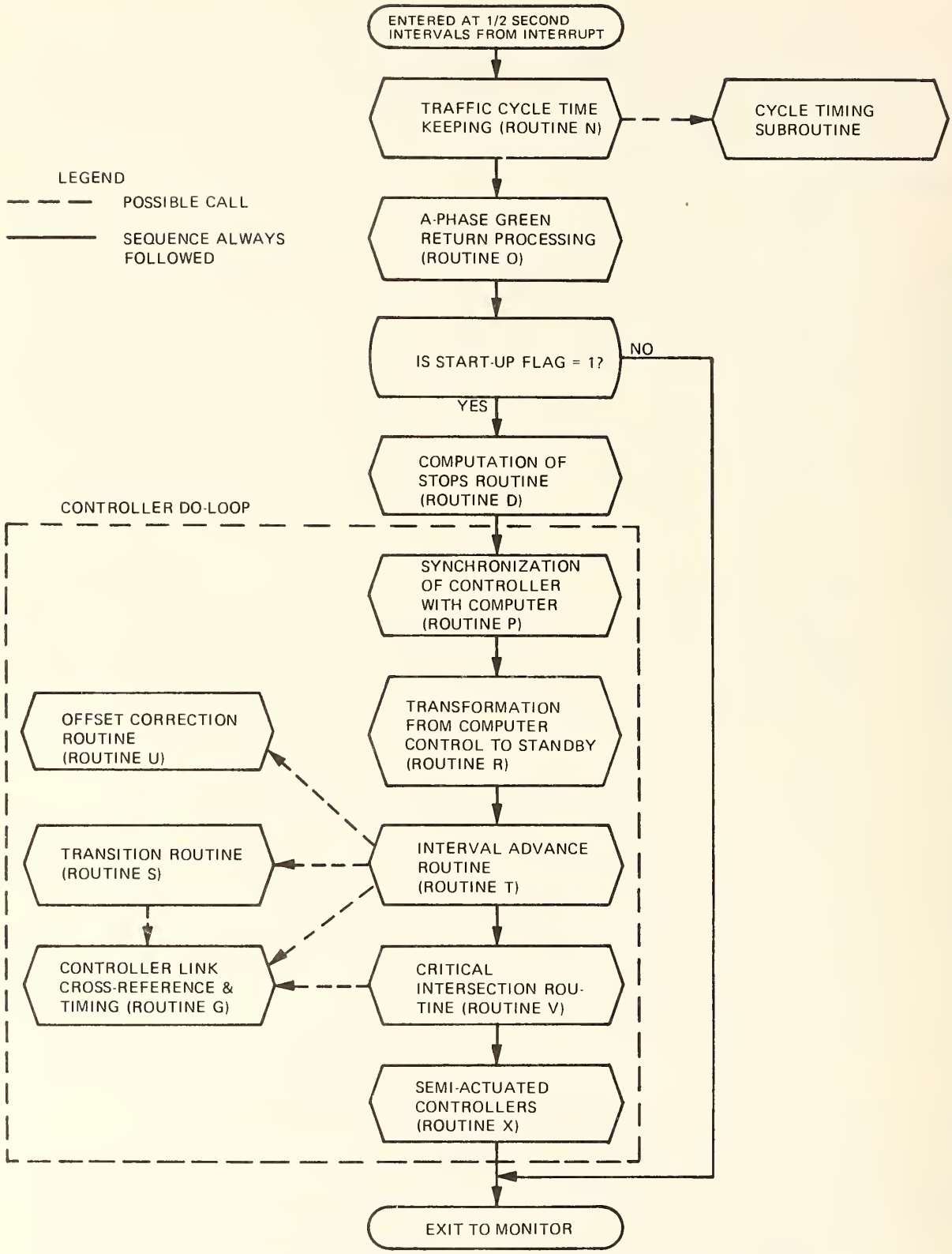


FIGURE 1.2. UTCS PRIORITY LEVEL TWO ROUTINES

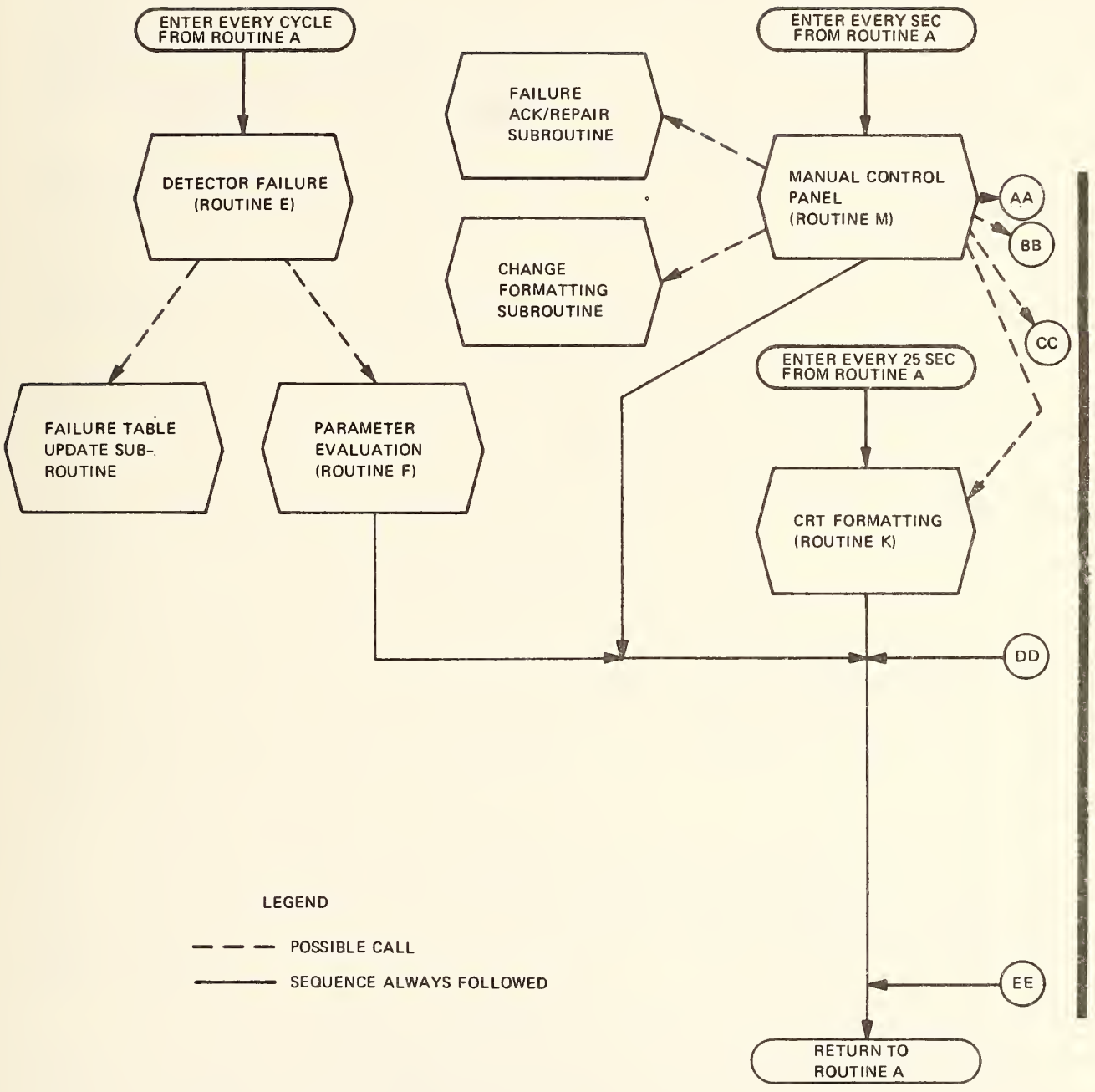


FIGURE 1.3. UTCS PRIORITY LEVEL THREE ROUTINES

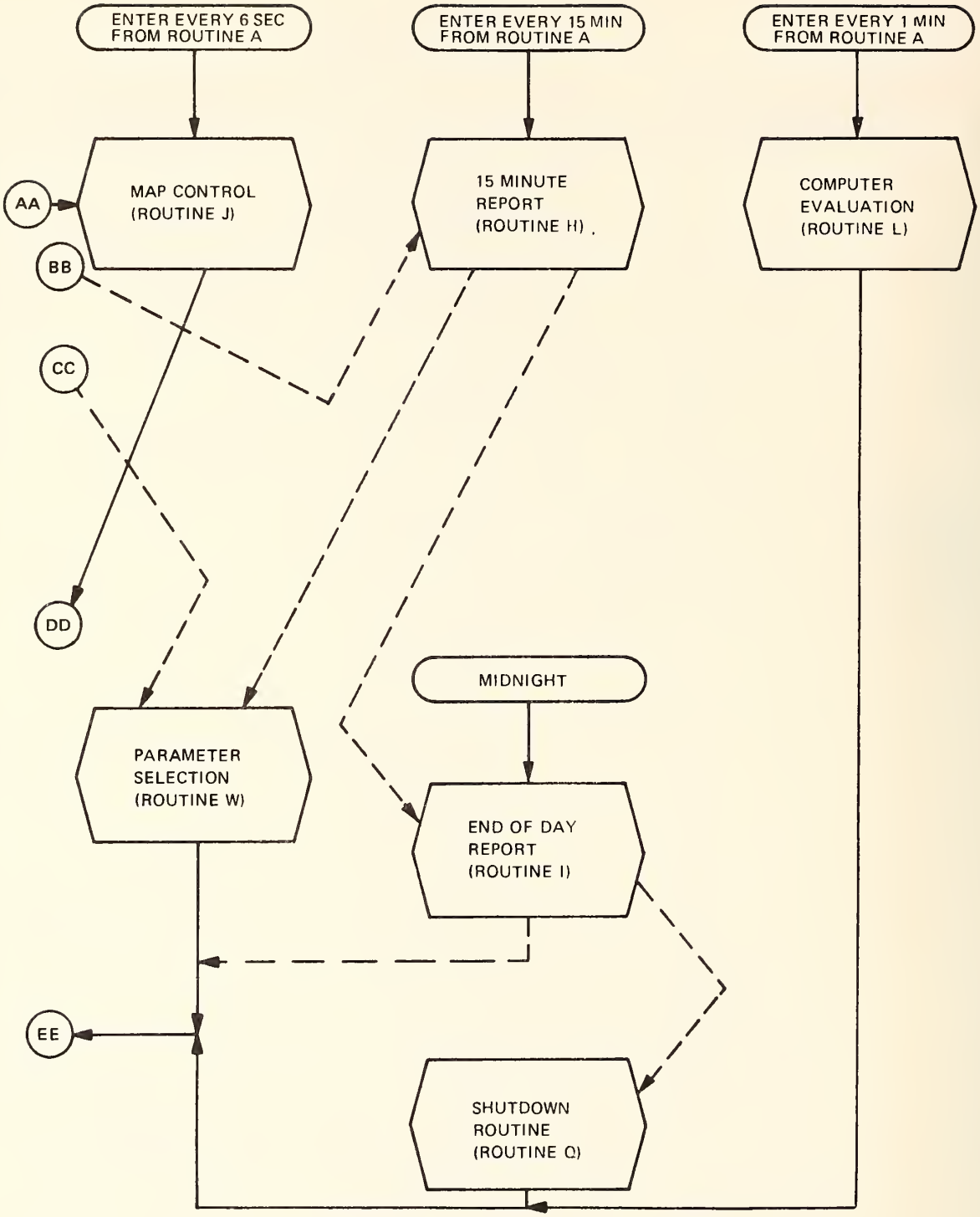


FIGURE 1.3. UTCS PRIORITY LEVEL THREE ROUTINES

As part of the start-up procedure, the start time for each of the cycles is synchronized with the corresponding cycle timing references from the District's (standby) system. A check is provided at the end of each cycle to determine whether this synchronization is being maintained.

A-Phase Green Return Processing, Routine O

This routine samples the A-Phase Green Return data read in by the Executive Routine. Two sets of flags are generated, based on this data, for use by other routines. One set is based on the presence of A-Phase Green for each controller; the other set denotes the start of A-Phase Green.

Synchronization of Controller with Computer, Routine P

This routine compares the A-Phase Green Return data with the computer's internal controller interval data for each controller to identify possible controller malfunctions. If the controller is found to be in error by one interval, an attempt is made to effect synchronization by either transmitting an extra advance pulse or inhibiting the next one due. If the controller is found to be in error by two or more intervals, the controller is placed into standby and designated as having failed.

Transformation from Computer Control to Standby, Routine R

This routine performs the required functions when it is desired to release a non-semi-actuated controller from computer control and place it into the standby mode. Controllers are placed in standby by resetting the computer HOLD output after 7.5 seconds of the A-Phase Green interval have elapsed.

Interval Advance, Routine T

The Interval Advance Routine generates, for each controller, the advance pulse data required to step the controller through its sequence of intervals. The advance pulse array generated by this routine is used by the Executive Routine to send the advance pulses to the controllers.

This routine also brings controllers under computer control from standby, when desired. In addition, when a transition from one set of controller intervals to another is desired as a result of either an operator action or a logical decision made by the computer, the operations required to identify the desired change and execute it are performed by this routine.

Offset Correction, Routine U

This routine compares the offset for each controller with the desired offset at the start of each controller cycle. If a discrepancy is found, its magnitude and sense are evaluated. The necessary adjustment is made by modification of the first controller interval. For large changes, several cycles are used.

Transition, Routine S

This routine computes the value of the variable controller intervals to provide a smooth transformation from one controller pattern to another. Split and safety intervals are maintained and cycle lengths are constrained within pre-defined limits. The Transition Routine is called whenever one of the following conditions exist: (1) the controller is being removed from standby and placed on line, or (2) a new pattern has been selected for the section to which this controller belongs.

Controller-Link Cross Reference and Timing, Routine G

This routine computes the duration of intervals in each controller cycle which are required for the computation of measures of effectiveness. The data are then ordered by links in a format consistent with the requirements of the routines generating the measures of effectiveness.

Critical Intersection, Routine V

This routine apportions the split between the critical phases of the controller cycle for those controllers that have been designated as Critical Intersection Controllers (CICs) in accordance with the vehicular demand on these phases as measured by their respective queue lengths and volumes. The split adjustment is made at the start of the controller cycle if all the required data are available and meet previously specified limits on magnitude. This routine also inhibits BPS extensions when various conditions unfavorable to BPS are present in UTCS.

Semi-Actuated Controller, Routine X

This routine performs the computations necessary to determine the start and maximum length of the B-Phase for each of the Semi-Actuated Controllers in the system. At the computed time, a yield pulse is transmitted to the controller. The decision as to whether or not to implement the B-Phase interval and, if so, the characteristics of the interval is made locally by the controller based on its pedestrian and vehicle sensor outputs. This routine also checks all semi-actuated controllers for malfunction, introduces operator selected offset changes, and puts them into and out of standby.

Computation of Stops, Routine D

This routine performs the timing and computations required to determine the number of vehicle stops occurring and the lengths of the vehicle queues on those links which are instrumented with two or more detectors. It also computes link delay. This routine also executes bus priority extensions when requested and makes the appropriate adjustments to the stop computations, the measure of effectiveness (MOE) timing, and the controller timing.

Priority Level 3

The Priority Level 3 routines provide the display and operator interface functions. Those data evaluation functions for which time is not critical are also performed by Priority Level 3 routines. The routines that comprise Level 3 are shown in Figure 1.3 in the sequence in which they may be entered. Each routine is called by the Level 3 portion of the Executive Routine and returns to the Level 3 portion of the Executive Routine when it is completed.

Manual Control Panel Processing, Routine M

The Manual Control Panel Processing Routine records the configuration of the controls set by the operator, evaluates the inputs for reasonableness and stores the data and flags required by other routines in responding to the requested operations. Included in the functions performed by this routine are the selection of data to be displayed on the illuminated street map, the selection of the CRT page to be displayed, and the selection of all system parameters and operating modes.

The Change Formatting Subroutine is entered from the Manual Control Panel Processing Routine, Routine M, whenever a system parameter or operating mode is changed by the operator.

Map Control and Data Formatting, Routine J

The Map Control and Data Formatting Routine controls the lamps on the illuminated street map display. The lamps are of two types; red and green lights which provide controller status information, and yellow lights which provide link parameter data. The type of information which is to be displayed is defined by the settings of the pertinent switches at the Traffic Control Panel.

CRT Control and Data Formatting, Routine K

The CRT Control and Data Formatting Routine causes the selected display (page) to be presented on the CRT device.

In addition, the CRT control and Data Formatting Routine includes two subroutines which are resident in the computer core memory: the CRT Failure Table Add Subroutine, which updates the controller and detector failure records when new failures are identified, and the CRT Failure Table Acknowledge and Repair Subroutine which updates or deletes elements of the failure table based on inputs from the traffic control panel.

Detector and Communications Failure Detection, Routine E

The Detector and Communications Failure Detection Routine identifies failures in the vehicle sensing function. The failures are classified in accordance with the symptoms noted as detector electronics, detector obstruction, or communications failures. When a failure is recorded, the operator is informed via the CRT Failure Table Add Subroutine, and suitable flags are set, preventing the use of information from the errant detector.

In addition to the failure identification functions performed, the raw link volume and occupancy counts are updated by this routine.

Link Volume Occupancy and Speed Evaluation, Routine F

This Routine, which is entered from the Detector and Communications Failure Detection Routine when the last detector on each link is sampled, computes link volume, occupancy, and average speed, and smoothes these values by combining them with past data. If a link is inactive, prestored typical volume and occupancy values are used for display purposes.

Fifteen Minute Performance and Status Report, Routine H

The Fifteen Minute Performance and Status Report Routine transmits system status, system performance and a record of operator commands to the line printer for printout at 15-minute intervals. In addition, this routine records the values of all the measures of effectiveness for each link on magnetic tape.

Controller Parameter Selection, Routine W

The Controller Parameter Selection Routine selects, for each controller in a section, the intervals appropriate to the operating mode of the section. A set of intervals and related bus priority parameters for all of the controllers in a section is called a pattern for that section. For sections in the traffic responsive mode, traffic data are matched against pre-stored histories at 15-minute intervals to determine whether or not a pattern change is required. For all sections, the controller patterns are changed if a mode or pattern change is requested by the operator. Section patterns, bus priority parameters,

and history data are stored in the fast access mass-storage device (disc) and read into the computer core memory as required.

Shut-Down and End of Day Report, Routines Q and I

The Shut-Down routine stores pertinent data on the fast-access mass-storage device at the conclusion of the day's operations. These data are thus available for read-in at a subsequent operating period. A report on data accumulated during the operating period is also provided.

Shut-down is effected by the operator by inserting System Shutdown at the control panel. The data storage and report writing functions are initiated by the Shut-Down routine after all the controllers in the system have been placed in the standby mode.

Computer Performance Evaluation, Routine L

The Computer Performance Evaluation routine tests memory access and instruction operation of the Central Computer. If a computer failure is noted, the controllers are placed in standby, an alarm lamp and buzzer are energized, and a "panic display" is sent to the CRT.

Other Routines

The only routine in this category is the Start Up routine.

Start-Up, Routine Y

The Start-Up routine is entered once at the beginning of system operations. The routine sets flags, initializes clock counts and sets all initial conditions required by other routines.

1.2 Organization of BPS CPU Functions.

The BPS Computer routines are organized in accordance with the frequency at which various functions are required to be performed. The BPS Executive Routine controls the sequence by which other BPS cyclical routines are performed in accordance with pre-defined assignments of priority and elapsed time. Functions that are performed 32 times per second are specified in routines that are assigned to Priority Level 1. Priority Level 2 routines are entered once per second.

The timing for the BPS Executive Routine is controlled by an interprocesser interrupt that is triggered by the UTCS Computer 32 times per second. This interrupt also maintains synchronism between the UTCS and BPS Systems. When the interrupt occurs, any routine in progress is suspended and control is given to the BPS Executive Routine which records on magnetic tape, Bus and Vehicle Detector data, Controller data, Control Panel data and Map data, if history recording had been requested by the operator. Irrespective of whether history recording is requested, each time the BPS Executive Routine is performed, that is, 32 times per second, the BPS Priority Level 1 routines are executed. At the completion of Level 1, the BPS Executive routine allows the Priority Level 2 routines to be resumed from the point at which they had been interrupted. When the one second mark is encountered, the Priority Level 2 routines are executed. If the Priority Level 2 routines are completed before Level 1 is scheduled to start again, the BPS Executive Routine places the system in an idle loop. It should be noted that the BPS Computer is not under the control of a monitor, as is the case with the UTCS Computer.

Priority Level 1

Priority Level 1 routines embody those functions that are directly associated with the measurement of bus traffic and executive control. The sequence of non-executvie functions performed in this level is illustrated by the flow chart in Figure 1.4.

Routine BA, BPS Executive

This routine maintains the timing for all time-dependent functions, direct the input and output of data, records history if requested and calls other routines in accordance with pre-defined timing and sequence requirements.

Routine BB, Bus Detector Data Input and Interpretation

This routine reads all the bus detector data once every 1/32 of a second. The detector data are processed to determine and label any detector communications channel failures. Each bus detected is then identified as to whether it is a "through" or "stopping" bus and whether it is at an upstream or a downstream detector. The "Once per Bus" Routine is then entered.

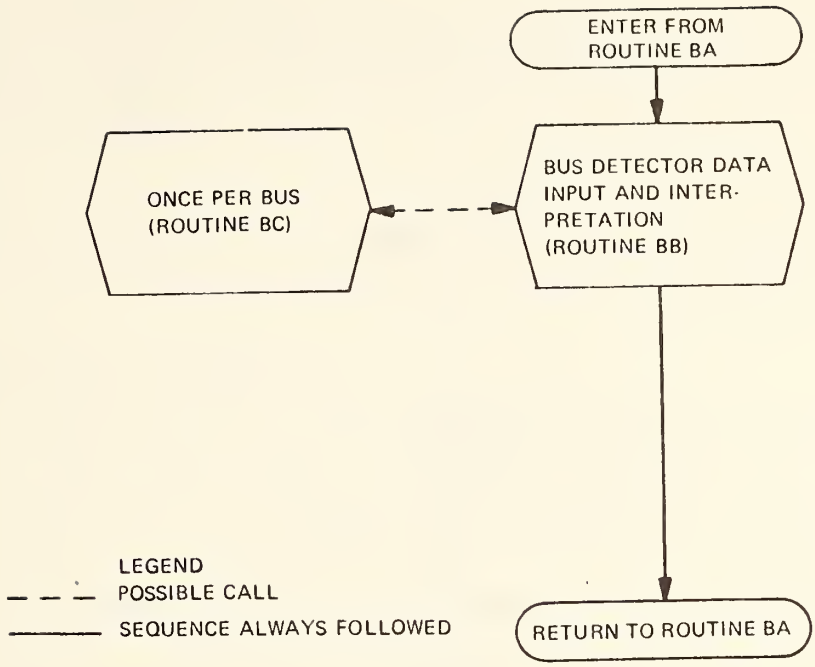


FIGURE 1.4. BPS NON-EXECUTIVE PRIORITY LEVEL ONE ROUTINES

Routine BC, Once Per Bus

This routine computes the bus zone occupancies for all through and stopping buses in each bus zone. This routine is entered each time a bus is detected by Routine BB. In addition, a second set of through and stopping occupancies are computed for those buses which enter or leave the bus zones during time intervals in which they might be helped by extensions. Tests are performed during the computations of the various bus zone occupancies to detect and correct errors which have occurred due to missed detections or improper use of the driver-controlled bus status switch. Detector malfunction is identified.

Priority Level 2

Priority Level 2 routines are primarily associated with the timing of bus arrivals by synchronizing to the UTCS controller commands and by the granting of bus priorities. BPS malfunction detection is also performed at this level. The relationship between the priority level two routines is depicted in Figure 1.5.

Routine BD, Bus Priority Link Timing

This routine performs the timing for all bus priority system action periods. It synchronizes the timing for each bus link to the controller intervals currently in use by UTCS and defines the time periods in which buses may be helped by an extension.

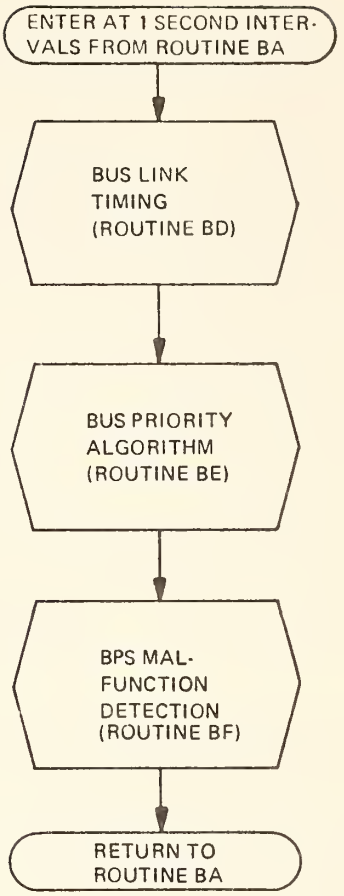


FIGURE 1.5. BPS PRIORITY LEVEL TWO ROUTINES

Routine BE, Bus Priority Algorithm

This routine computes the intersection gain for each bus zone one second prior to the start of amber for the zone, provided that bus priorities have not been inhibited for that zone. Bus priorities are permitted only if:

- The controller is under computer control and has been designated as a CIC.
- The CIC queue thresholds have not been exceeded.
- The controller is not in transition.
- The controller is not undergoing an offset correction.
- All bus detectors and UTCS queue detectors associated with the controller are on line.
- The intersections have been selected by the operator for bus priorities.
- There are no detectable errors in any bus zone associated with the controller.

When these conditions are met, the net reduction in passenger delay that the extension will provide is computed, and, if it exceeds a predetermined threshold, the extension is granted. When the extension is completed, the net reduction in passenger delay actually achieved is computed for MOE evaluation.

Routine BF, Malfunction Detection

This routine passes to Routine K, the number of failed detectors or communications at the time of failure. It then sets Routine K active.

Other Routines

Fifteen Minute Report, Manual Control Panel Processing, Shutdown, End-of-Day Report and Start Up are performed in the UTCS Computer for the Bus Priority System.

1.3 Data Processing Equipment

The UTCS/BPS Data Processing equipment shown in Figure 1.6, is composed of a dual processor system, each of which has access to core memory. The computer configuration is composed of two Xerox Data Systems (XDS) Sigma V computers and a core memory (used by both CPUs) of 65, 536 words, each of which is 32 bits long. In addition to core storage, peripheral storage is provided by Rapid Access Discs (RADs) and 7-track magnetic tape drives. Two RADs supplying 1.5 and 3 megabytes of storage are used to store the operating system program, the UTCS and BPS programs, traffic patterns and start-up parameters. Two tape drives are controlled by the UTCS CPU and may be used to bootstrap the operating system on to the RADs, to store BPS MOEs and UTCS MOEs. A third tape drive is controlled by the BPS CPU and is used to store raw vehicle and bus data. A line printer controlled by the UTCS CPU is used to provide hard copy records of the 15 minute and end of day reports. Two Hazeltine Model 2000 CRT units are used to provide UTCS and BPS system data that is requested by the operator. The requests are made from the control panel. The control panel is also used to select the modes of operation of the system and the type of map display desired. Additional peripheral units controlled by the UTCS CPU are 80 column card punch and card reader units. Each of the CPUs also has its own teletype (TTY) unit.

It should be noted that the Sigma V CPU normally accepts cards that have been keypunched with an EBCDIC character set. Some deck cards (Macro-Symbol, FORTRAN) punched with a BCD (Field Data) character set may also be accepted by using the FBCD conversion routine supplied with the operating system. However, all updates to the assembled program must be done using EBCDIC coded cards.

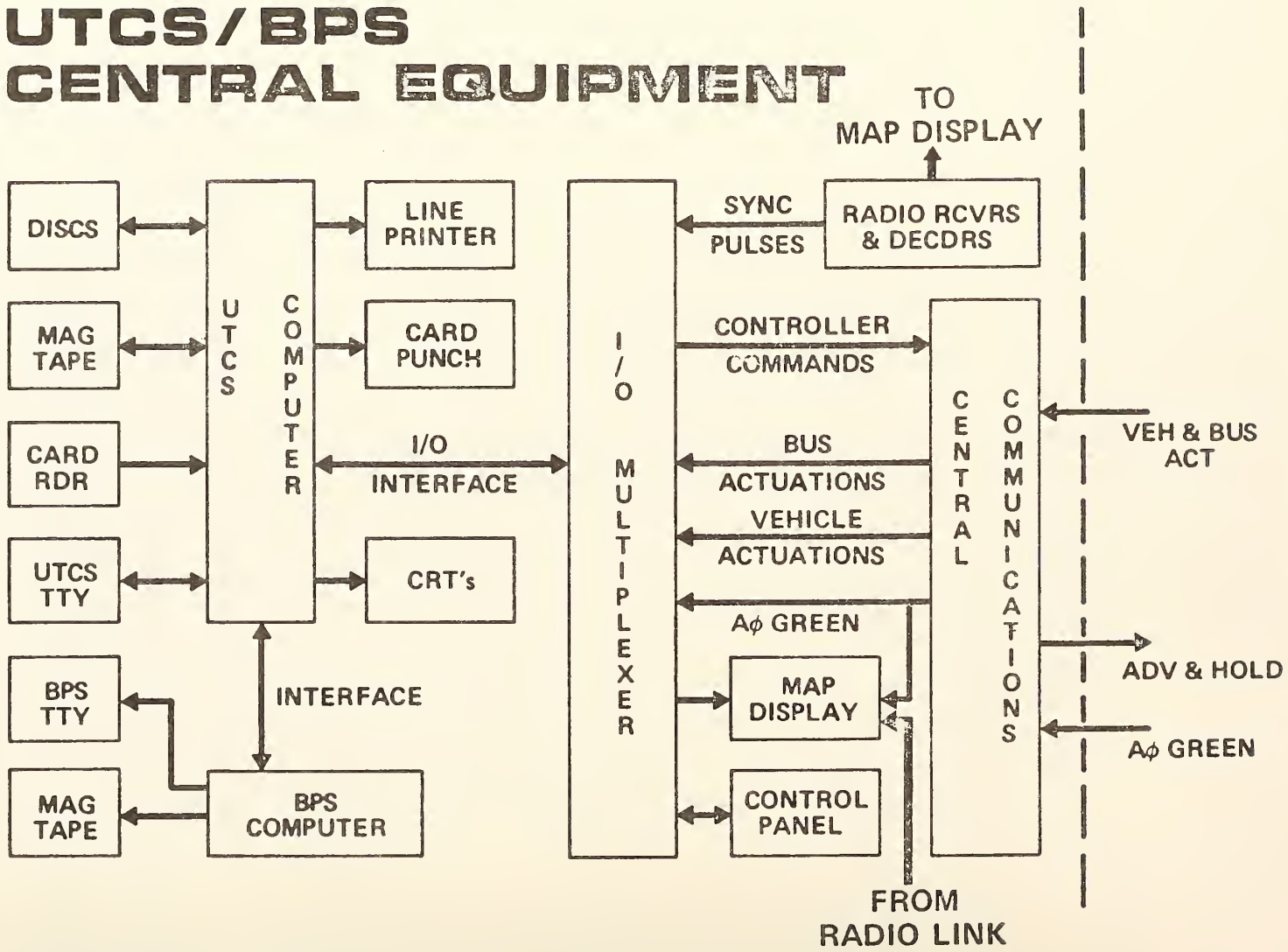


FIGURE 1.6. UTCS/BPS DATA PROCESSING EQUIPMENT

1.4 Software Operating System

The software operating system used in the UTCS CPU is the XDS Real-Time Batch Monitor (RBM), version C01. A Monitor is a program that supervises the processing, loading and execution of other programs. RBM provides for real-time foreground processing at its higher level of operation and batch processing at its lower level of operation. The real-time programs are the UTCS and BPS routines. The UTCS and BPS routines are controlled by their corresponding executive routines which react to external interrupts that are generated via clock pulses or are triggered by individual routines. It should also be noted that a modification to the standard XDS character oriented communications (COC) package of RBM was performed. This modification consisted of removing the unused EBCDIC to ASCII conversion table for the purpose of saving storage. Further details can be found in the RBM Reference Manual listed in Section 4.9.

1.5 Priority Interrupt System

Sixteen external interrupts are supplied with the system. Twelve of these are used for the UTCS CPU while the remaining four are used by the BPS CPU. A listing of the present external interrupt's tasks is contained in Table 1.1. In addition to the external interrupts, an internal clock pulse decrements a counter 8000 times per second. When the counter is decremented every 1/32 second to zero, the Counter Equals Zero interrupt in location X '5A' (where X signifies hexadecimal) is triggered, causing a short portion of the UTCS executive routine to set the counter to its initial value of 250 and trigger the interprocessor and UTCS Level 1 interrupts. Note that internal clock interrupt in location X '5A' has a higher priority than the external interrupts listed in Table 1.1.

The priority triggering structure of the UTCS and BPS CPUs is shown in Table 1.2. Every 1/32 second, the Counter Equals Zero internal clock interrupt triggers the UTCS Level 1 external interrupt and the UTCS Interprocessor interrupt which triggers the BPS Interprocessor interrupt in the BPS CPU. The UTCS Level 1 interrupt causes the UTCS executive routine to transfer the required data to and from the I/O Multiplexer and to initiate the processing of the detector inputs. When 1/2 second has elapsed, the UTCS Level 2 and Level 3 external interrupts are triggered by the UTCS Executive Routine. The Level 2 routines are primarily controller oriented. At the completion of Level 2, the 15 minute report routine is performed at Level 3 if the fifteen minute flag is set. At Level 3 the end of day report routine is also performed if the end of day flag is set. After completion of Level 3, the Level 4 external interrupt is triggered if there is a CRT request. After the Level 4 CRT routines are completed, the Monitor

allows the system to perform batch processing or idle until the next 1/32 second clock interrupt.

In the BPS CPU, the BPS Interprocessor interrupt triggers the BPS Level 1 external interrupt. This, in turn, causes the BPS Executive Routine to initiate the processing of the BPS detector inputs. When 1 second has elapsed, the BPS Level 2 external interrupt is triggered by the BPS Executive Routine. After the completion of the remaining BPS routines at Level 2, the BPS CPU stays in an idle loop until receipt of the next 1/32 second BPS Interprocessor interrupt.

Table 1.1

Σ5 Interrupt Structure
(External Group 2)

- UTCS (CPU 1)

Location	Function	
X '60'	Interprocessor	
61	Return Interprocessor (not used)	
62	Level 1 (1/32 second timing)	
63	Level 2 (1/2 second timing)	
64	Level 3 (other cyclical routine)	
65	Not used	
66	CRT Input (not used)	Used by
67	Output to CRT	Monitor
68	Level 4 (CRT output Routine)	
69	Not used	
6A	Not used	
6B	Monitor Control Task	

- BPS (CPU 2)

Location	Function
X '60'	Return interprocessor (Not used)
61	Interprocessor
62	Level 1 (1/32 second timing)
63	Level 2 (1 second timing)

Table 1.2

Priority Triggering Structure

Interrupt	Triggered by
UTCS Level 1	Counter Equals Zero (1/32 second)
UTCS Level 2	UTCS Executive Routine
UTCS Level 3	UTCS Executive Routine
UTCS Level 4	Routine K
Monitor Batch Mode	RBM
UTCS Interprocessor	Counter Equals Zero (1/32 second)
BPS Interprocessor	UTCS Interprocessor
BPS Level 1	BPS Interprocessor
BPS Level 2	BPS Executive Routine

*NOTE: End of BPS level 2 causes BPS CPU to transfer to an idle loop.

1.6 Input/Output

In the Sigma 5 system, the CPU executes instructions, the Multiplexer Input/Output Processor (MIOP) executes commands, and the I/O device executes orders. For example, the CPU may execute a start I/O (SIO) instruction to initiate an I/O operation. During the course of the operation, the MIOP fetches a command doubleword (command) fom the command list in core memory and stores it (except the order bits) in its own fast access memory. The command provides the MIOP with information needed to perform its functions; commands are, therefore, executed by the MIOP. The order bits of the command are transmitted to the device. The order defines the operation to be performed by the device; the I/O devices, therefore, execute orders.

For a description of I/O instructions, commands and orders see XDS Sigma 5 Computer Reference Manual listed in Section 4.9.

As indicated in Figure 1.6, the UTCS and BPS CPUs input/output (I/O) is comprised of peripheral unit data and data transferred by the I/O multiplexer. The peripheral units tied to the UTCS CPU are the two RADs, two magnetic tape drives, the card reader, the UTCS TTY, the line printer, the card punch and the two CRTs. The BPS CPU has a magnetic tape drive and the BPS TTY connected to it. A table of the peripheral unit software addresses is shown in Table 1.3. The table lists both the physical and logical

addresses for the UTCS peripheral units. The physical address is to be used when addressing the unit directly while the logic address is to be used when the calls are to be made through the monitor. Logical addresses do not apply to the BPS peripherals since the BPS CPU is not under the control of a monitor.

Table 1.3

Peripheral Unit Physical and Logical Addresses

Peripheral Unit	Physical Address	Logical Address
UTCS TTY	001	A01
Line Printer (LP)	002	A02
Card Reader (CR)	003	A03
Card Punch (CP)	004	A04
UTCS Tape No. x	0Ex	AEx
RAD 1 (3 m-byte)	0F0	AF0
RAD 2 (1.5 m-byte)	0F1	AF1
BPS Tape No. x	0Dx	--
BPS TTY	001	--

The remainder of the I/O is connected from the I/O multiplexer to the UTCS CPU. The inputs selected by the multiplexer include the synchronism pulses from radio-central, the bus actuations, the vehicle actuations, the A-Phase green returns and the control panel inputs. The multiplexer directs outputs comprised of controller commands, map data and control panel outputs.

The multiplexer configuration is composed of standard XDS I/O units as shown in Figure 1.7. The main chassis or multiplexer is a XDS Model 7929 unit. This unit contains Models 7969 and 7970 timing units, two Model 7930 cabinets and six Model 7931 cabinets. Each of the Model 7930 cabinets contain 12 Model 7951 input cards. The Model 7931 cabinets contain up to 16 cards which are composed of Model 7950 output cards, Model 7951 input cards or both types of cards. Each of the Model 7950 units has provisions for supplying 8 outputs while the Model 7951 units can accept 16 inputs. The UTCS CPU has access to 32 data points at a time.

A table indicating the multiplexer commands for selecting multiplexer data is shown in Table 1.4.

When inputting or outputting a word of data via the multiplexer, two consecutive words of buffer storage are required. The first word is the command and the second word contains the data. If for example, one wishes to read in all four words of the A-Phase

Green data from the multiplexer (G_1, G_2, G_3, and G_4) a buffer of 8 words must be provided. The 8 words are composed of 4 command words interleaved with 4 data words. This is one reason why some arrays in the glossary (Section 3) are listed as being interleaved. Another reason for interleaving data arrays is to save memory access time by loading two consecutive data words into registers with a single "load double word" instruction. For additional detail concerning the model 7929 order format and a description of the other XDS units used in the multiplexer refer to the XDS Sigma System Interface Units manual listed in Section 4.9.

Table 1.4

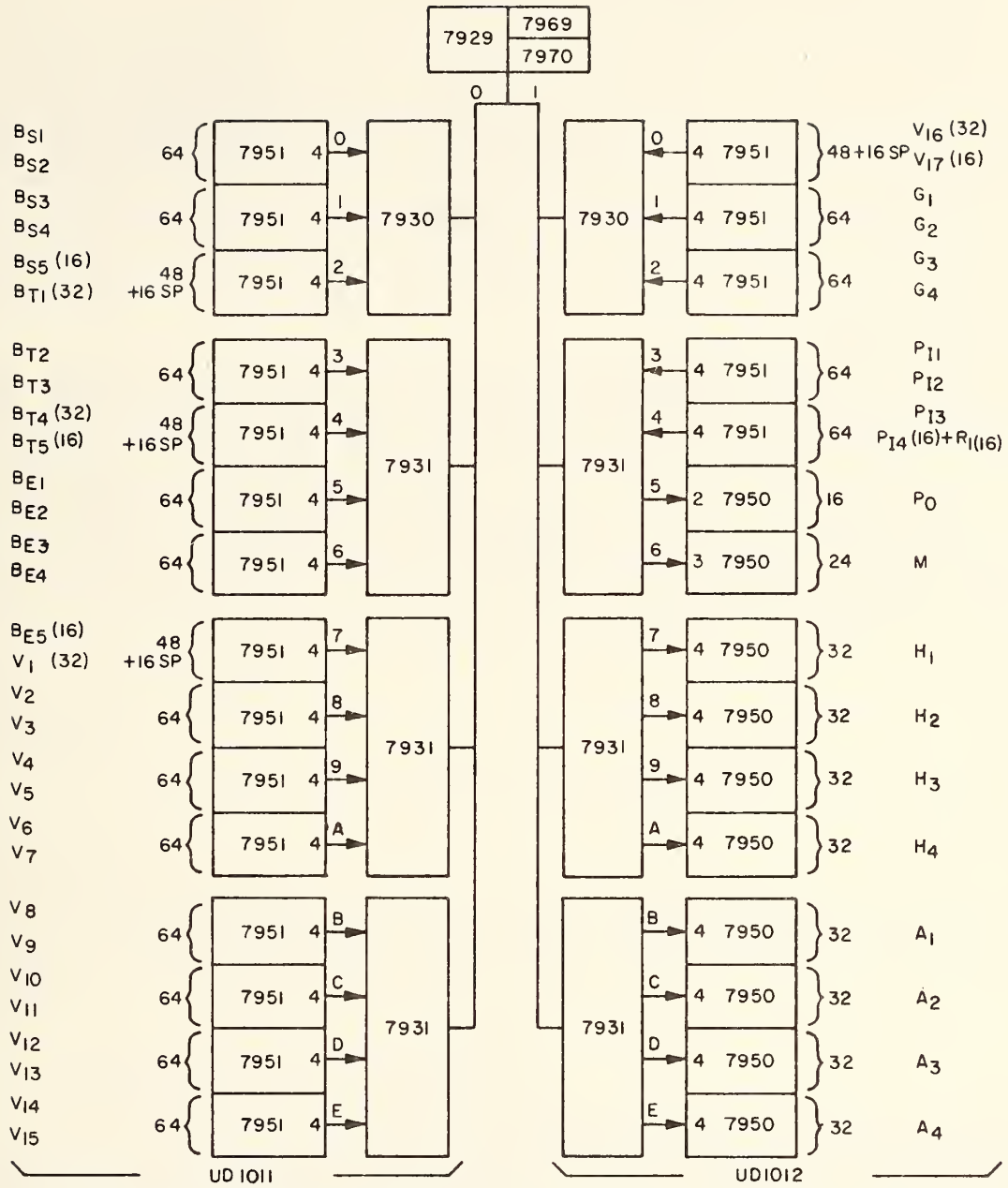
Multiplexer Commands (in Hexadecimal)

Data	Word Name	Bits 1-20	Bits 21-24	Bits 25-28	Bits 29-32
Bus Stop 1-32	B_{S1}	0080C	0	0	F
Bus Stop 33-64	B_{S2}	0080C	1	0	F
Bus Stop 65-96	B_{S3}	0080C	0	1	F
Bus Stop 97-128	B_{S4}	0080C	1	1	F
Bus Stop 129-144	B_{S5}	0080C	0	2	F
Bus Through 1-32	B_{T1}	0080C	1	2	F
Bus Through 33-64	B_{T2}	0080C	0	3	F
Bus Through 65-96	B_{T3}	0080C	1	3	F
Bus Through 97-128	B_{T4}	0080C	0	4	F
Bus Through 129-144	B_{T5}	0080C	1	4	F
Bus Error 1-32	B_{E1}	0080C	0	5	F
Bus Error 33-64	B_{E2}	0080C	1	5	F
Bus Error 65-96	B_{E3}	0080C	0	6	F
Bus Error 97-128	B_{E4}	0080C	1	6	F
Bus Error 129-144	B_{E5}	0080C	0	7	F
Vehicle Detector 1-32	V_1	0080C	1	7	F
Vehicle Detector 33-64	V_2	0080C	0	8	F
Vehicle Detector 65-96	V_3	0080C	1	8	F
Vehicle Detector 97-128	V_4	0080C	0	9	F
Vehicle Detector 129-160	V_5	0080C	1	9	F
Vehicle Detector 161-192	V_6	0080C	0	A	F
Vehicle Detector 193-224	V_7	0080C	1	A	F
Vehicle Detector 225-256	V_8	0080C	0	B	F

Table 1.4

Multiplexer Commands (in Hexadecimal) (Cont'd)

Data	Word Name	Bits 1-20	Bits 21-24	Bits 25-28	Bits 29-32
Vehicle Detector 257-288	V_9	0080C	1	B	F
Vehicle Detector 289-320	V_{10}	0080C	0	C	F
Vehicle Detector 321-352	V_{11}	0080C	1	C	F
Vehicle Detector 353-384	V_{12}	0080C	0	D	F
Vehicle Detector 385-416	V_{13}	0080C	1	D	F
Vehicle Detector 417-448	V_{14}	0080C	0	E	F
Vehicle Detector 449-480	V_{15}	0080C	1	E	F
Vehicle Detector 481-512	V_{16}	0080C	2	0	F
Vehicle Detector 513-528	V_{17}	0080C	3	0	F
A-Phase Green 1-32	G_1	0080C	2	1	F
A-Phase Green 33-64	G_2	0080C	3	1	F
A-Phase Green 65-96	G_3	0080C	2	2	F
A-Phase Green 97-128	G_4	0080C	3	2	F
Panel Input 1-32	P_{I1}	0080C	2	3	F
Panel Input 33-64	P_{I2}	0080C	3	3	F
Panel Input 65-96	P_{I3}	0080C	2	4	F
Panel Input 97-112	P_{I4}	0080C	3	4	F
Radio-Synch 113-128	R_I	0080C	3	4	F
Panel Output 1-16	P_O	0080C	2	5	F
Map 1-24	M	0080C	2	6	F
Hold 1-32	H_1	0080C	2	7	F
Hold 33-64	H_2	0080C	2	8	F
Hold 65-96	H_3	0080C	2	9	F
Hold 97-128	H_4	0080C	2	A	F
Advance 1-32	A_1	0080C	2	B	F
Advance 33-64	A_2	0080C	2	C	F
Advance 65-96	A_3	0080C	2	D	F
Advance 97-128	A_4	0080C	2	E	F



WORD	DESCRIPTION	WORD	DESCRIPTION
BS	BUS STOP	R_1	RADIO LINK
BT	BUS THROUGH	PO	CONTROL PANEL OUTPUT
BE	BUS ERROR	M	MAP ELECTRONICS
V	VEHICLE DETECTOR	H	HOLD
G	GREEN RETURN	A	ADVANCE
P	CONTROL PANEL	SP	SPARE

Figure 1.7 MUX Configuration

1.7 Entry and Working Storage for Pattern Changes

When the system changes patterns, new pattern data is transferred, by section, from the RAD to the core storage pattern array (PTN). The Controller Parameter Selection Routine, Routine W, reformats the PTN array data into entry storage arrays (the Level 2 interrupt is disabled during this process) and sets transition flags for all controllers in the section. Until the transition flags are set, data in the entry storage arrays has no effect upon the actual street patterns. This was done to prevent the Priority Level 2 controller routines from operating with incorrect entry data in the event that they interrupt Routine W, which is at Priority Level 3.

After the transition flags are set and the Priority Level 2 routines are scheduled, the appropriate controller routines compute working storage data from entry storage data for parameters that can be temporarily altered by the operator. These parameters include offset, interval durations and bus extensions. All other parameters do not require working storage. For example, working cycle length (differing from desired cycle length due only to transition cycles or bus extensions) is defined at all times as the sum of the interval durations.

and history data are stored on the Rapid Access Device (RAD) and read into the computer core memory as required.

Shut-Down and End of Day Report, Routines Q and I

The Shut-Down Routine stores pertinent data on the RAD at the conclusion of the day's operations. These data are thus available for read-in at a subsequent operating period. A report on data accumulated during the operating period is also provided.

Shut-down is effected by the operator by inserting System Shutdown at the control panel. The data storage and report writing functions are initiated by the Shut-Down Routine after all the controllers in the system have been placed in the standby mode.

Computer Performance Evaluation, Routine L

The Computer Performance Evaluation Routine tests the memory access and instruction operation of the Central Computer. If a computer failure is noted, the controllers are placed into standby, an alarm lamp and buzzer are energized, and a "panic display" is sent to the CRT.

Other Routines

The only routine in this category is the Start-Up Routine.

Start-Up, Routine Y

The Start-Up Routine is entered once at the beginning of system operations. The routine sets flags, initializes clock counts and sets all initial conditions required by other routines.

1.2 Organization of BPS CPU Functions.

The BPS Computer routines are organized in accordance with the frequency at which various functions are required to be performed. The BPS Executive Routine controls the sequence with pre-defined assignments of priority and elapsed time. Functions that are performed 32 times per second are specified in routines that are assigned to Priority Level 1. Priority Level 2 routines are entered once per second.

The timing for the BPS Executive Routine is controlled by an interprocesser interrupt that is triggered by the UTCS Computer 32 times per second. This interrupt also maintains synchronism between the UTCS and BPS Systems. When the interrupt occurs, any routine in progress is suspended and control is given to the BPS Executive Routine which records on magnetic tape, bus and vehicle detector data, controller data, control panel data and map data, if history recording had been requested by the operator. Irrespective of whether history recording is requested, each time the BPS Executive Routine is performed, that is, 32 times per second, the BPS Priority Level 1 routines are executed. At the completion of Level 1, the BPS Executive Routine allows the Priority Level 2 routines to be resumed from the point at which they had been interrupted. When the one second mark is encountered, the Priority Level 2 routines are executed. If the Priority Level 2 routines are completed before Level 1 is scheduled to start again, the BPS Executive Routine places the system in an idle loop. It should be noted that the BPS Computer is not under the control of a monitor, as is the case with the UTCS Computer.

Priority Level 1

Priority Level 1 routines embody those functions that are directly associated with the measurement of bus traffic and executive control. The sequence of non-executive functions performed in this level is illustrated by the flow chart in Figure 1.4.

Routine BA, BPS Executive

This routine maintains the timing for all time-dependent functions, directs the input and output of data, records history if requested and calls other routines in accordance with pre-defined timing and sequence requirements.

Routine BB, Bus Detector Data Input and Interpretation

This routine reads all the bus detector data once every 1/32 of a second. The detector data are processed to determine and label any detector communications channel failures. Each bus detected is then identified as to whether it is a "through" or "stopping" bus and whether it is at an "upstream" or a "downstream" detector. The "Once per Bus" Routine is then entered.

Routine BF, Malfunction Detection

This routine passes to Routine K, the number of bus detector or communication failures at the time of the failure. It then sets Routine K active.

Other Routines

Fifteen Minute Report, Manual Control Panel Processing, Shut-Down, End-of-Day Report and Start-Up are performed in the UTCS Computer for the Bus Priority System.

1.3 Data Processing Equipment

The UTCS/BPS Data Processing equipment shown in Figure 1.6, is composed of a dual processor system, each of which has access to core memory. The computer configuration is composed of two Xerox Data Systems (XDS) Sigma 5 computers and a core memory (used by both CPUs) of 65, 536 words, of 32 bits each. In addition to core storage, peripheral storage is provided by Rapid Access Devices (RADs) and 7-track magnetic tape drives. Two RADs supplying 1.5 and 3 megabytes of storage are used to store the operating system program, the UTCS and BPS programs, traffic patterns and start-up parameters. Three tape drives are controlled by either CPU. They may be used to bootstrap the operating system onto the RAD, to record BPS MOEs and UTCS MOEs, and to record raw vehicle and bus data. A line printer controlled by the UTCS CPU is used to provide hard copy records of the 15-minute and end of day reports. Two Hazeltine Model 2000 CRT units are used to provide the UTCS and BPS system data that is requested by the operator. The requests are made from the control panel. The control panel is also used to select the modes of operation of the system and the type of may display desired. Additional peripheral units controlled by the UTCS CPU are 80 column card punch and card reader units. Each of the CPUs also has its own teletype (TTY) unit.

It should be noted that a Sigma 5 CPU normally accepts cards that have been keypunched with an EBCDIC character set. Some card decks (Macro-Symbol, FORTRAN) punched with a Field Data character set may also be accepted by using the FBCD conversion routine supplied with the operating system. However, all updates to the assembled program must be done using EBCDIC coded cards.

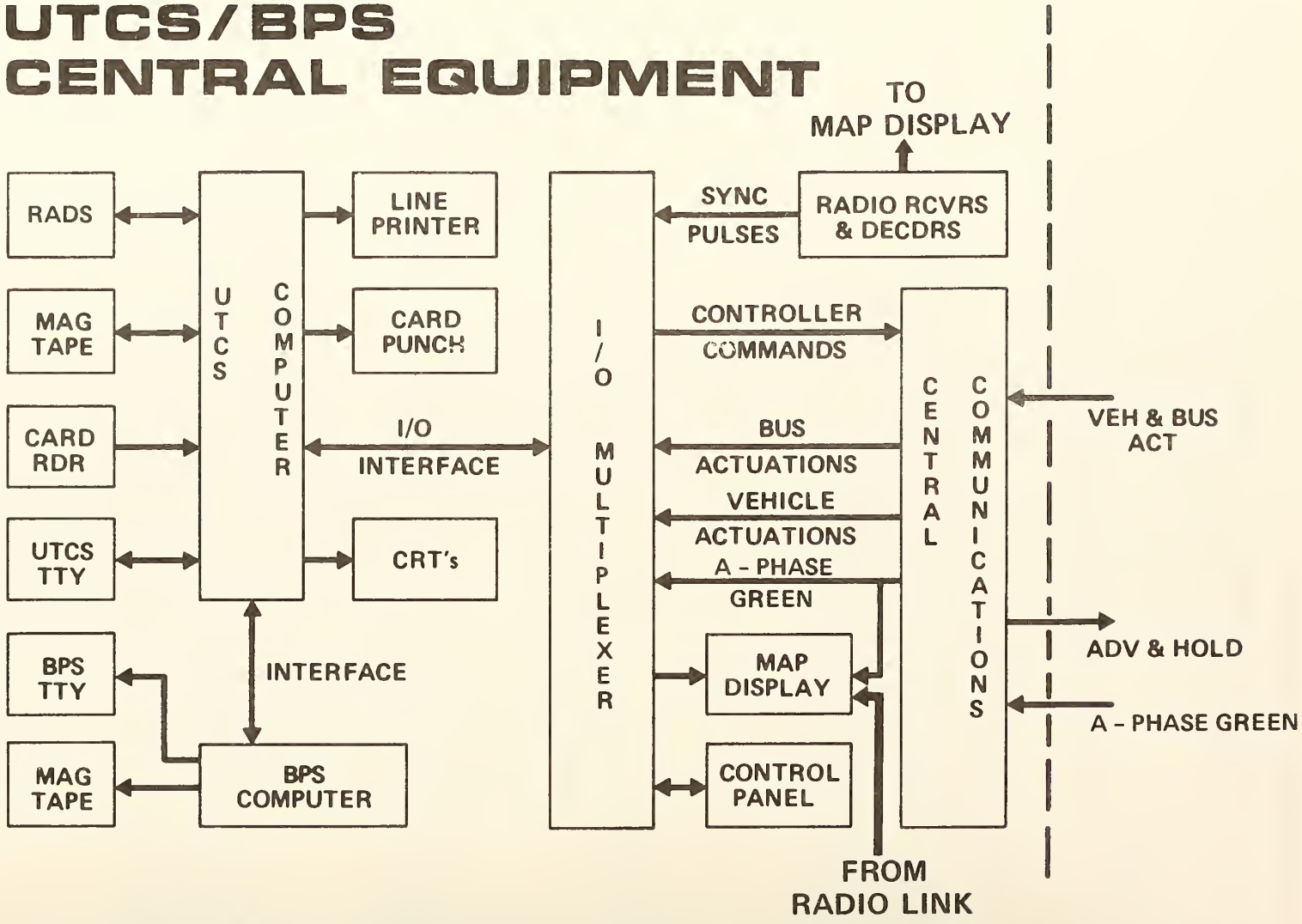


FIGURE 1.6. UTCS/BPS DATA PROCESSING EQUIPMENT

1.4 Software Operating System

The software operating system used in the UTCS CPU is the XDS Real-Time Batch Monitor (RBM). A Monitor is a program that supervises the processing, loading and execution of other programs. RBM provides for real-time foreground processing at its higher level of operation and batch processing at its lower level of operation. The real-time programs are the UTCS and BPS routines. The UTCS and BPS routines are controlled by their corresponding executive routines which react to external interrupts that are generated via clock pulses or are triggered by software commands. It should also be noted that a modification to the standard XDS character oriented communications (COC) package of RBM was performed. This modification consisted of removing the unused EBCDIC to ASCII conversion table for the purpose of saving storage. Further details can be found in the RBM Reference Manual listed in Section 4.10.

1.5 Priority Interrupt System

Sixteen external interrupts are supplied with the system. Twelve of these are used for the UTCS CPU while the remaining four are used by the BPS CPU. A listing of the present external interrupt's tasks is contained in Table 1.1. In addition to the external interrupts, an internal clock pulse decrements a counter 8000 times per second. When the counter is decremented every 1/32 second to zero, the Counter Equals Zero interrupt in location X '5A' (where X signifies hexadecimal) is triggered, causing a short portion of the UTCS Executive Routine to set the counter to its initial value of 250 and trigger the interprocessor and UTCS Level 1 interrupts. Note that internal clock interrupt in location X '5A' has a higher priority than the external interrupts listed in Table 1.1.

The priority triggering structure of the UTCS and BPS CPUs is shown in Table 1.2. Every 1/32 second, the Counter Equals Zero internal clock interrupt triggers the UTCS Level 1 external interrupt and the UTCS Interprocessor interrupt which triggers the BPS Interprocessor interrupt in the BPS CPU. The UTCS Level 1 interrupt causes the UTCS Executive Routine to transfer the required data to and from the I/O Multiplexer and to initiate the processing of the detector inputs. When 1/2 second has elapsed, the UTCS Level 2 and Level 3 external interrupts are triggered by the UTCS Executive Routine. The Level 2 routines are primarily controller oriented. At the completion of Level 2, the 15-Minute Report Routine is performed at Level 3 if the fifteen minute flag is set. At Level 3, the End of Day Report Routine is also performed if the end of day flag is set. After completion of Level 3, the Level 4 external interrupt is triggered if there is a CRT request. After the Level 4 CRT routines are completed, the Monitor

allows the system to perform batch processing or idle until the next 1/32 second clock interrupt.

In the BPS CPU, the BPS Interprocessor interrupt triggers the BPS Level 1 external interrupt. This, in turn, causes the BPS Executive Routine to initiate the processing of the BPS detector inputs. When 1 second has elapsed, the BPS Level 2 external interrupt is triggered by the BPS Executive Routine. After the completion of the remaining BPS routines at Level 2, the BPS CPU stays in an idle loop until receipt of the next 1/32 second BPS Interprocessor interrupt.

Table 1.1

Sigma 5 Interrupt Structure
(External Group 2)

- UTCS (CPU 1)

Location	Function	
X '60'	Interprocessor	
61	Return Interprocessor (not used)	
62	Level 1 (1/32 second timing)	
63	Level 2 (1/2 second timing)	
64	Level 3 (other cyclical routine)	
65	Not used	
66	CRT Input (not used)	Used by
67	Output to CRT	Monitor
68	Level 4 (CRT output Routine)	
69	Not used	
6A	Not used	
6B	Monitor Control Task	

- BPS (CPU 2)

Location	Function
X '60'	Return interprocessor (Not used)
61	Interprocessor
62	Level 1 (1/32 second timing)
63	Level 2 (1 second timing)

Table 1.2

Priority Triggering Structure

Interrupt	Triggered by
UTCS Level 1	Counter Equals Zero (1/32 second)
UTCS Level 2	UTCS Executive Routine
UTCS Level 3	UTCS Executive Routine
UTCS Level 4	Routine K
Monitor Batch Mode	RBM
UTCS Interprocessor	Counter Equals Zero (1/32 second)
BPS Interprocessor	UTCS Interprocessor
BPS Level 1	BPS Interprocessor
BPS Level 2	BPS Executive Routine*

*NOTE: End of BPS level 2 causes BPS CPU to transfer to an idle loop.

1.6 Input/Output

In the Sigma 5 system, the CPU executes instructions, the Multiplexer Input/Output Processor (MIOP) executes commands, and the I/O device executes orders. For example, the CPU may execute a start I/O (SIO) instruction to initiate an I/O operation. During the course of the operation, the MIOP fetches a command doubleword (command) from the command list in core memory and stores it (except the order bits) in its own fast access memory. The command provides the MIOP with information needed to perform its functions; commands are, therefore, executed by the MIOP. The order bits of the command are transmitted to the device. The order defines the operation to be performed by the device; the I/O devices, therefore, execute orders.

For a description of I/O instructions, commands and orders see XDS Sigma 5 Computer Reference Manual listed in Section 4.10 (Volume 2).

As indicated in Figure 1.6, the UTCS and BPS CPUs input/output (I/O) is comprised of peripheral unit data and data transferred via the I/O multiplexer. The peripheral units tied to the UTCS CPU are two RADs, two magnetic tape drives, card reader, UTCS TTY, line printer, card punch and two CRTs. The BPS CPU has a magnetic tape drive and the BPS TTY connected to it. A table of the peripheral unit software addresses is shown in Table 1.3. The table lists both the physical and logical

addresses for the UTCS peripheral units. The physical address is to be used when addressing the unit directly while the logical address is to be used when the calls are to be made through the monitor. Logical addresses do not apply to the BPS peripherals since the BPS CPU is not under the control of a monitor.

Table 1.3

Peripheral Unit Physical and Logical Addresses

Peripheral Unit	Physical Address	Logical Address
UTCS TTY	001	A01
Line Printer (LP)	002	A02
Card Reader (CR)	003	A03
Card Punch (CP)	004	A04
UTCS Tape No. x	0Ex	AEx
RAD 1 (3 m-byte)	0F0	AF0
RAD 2 (1.5 m-byte)	0F1	AF1
BPS Tape No. x	0Dx	--
BPS TTY	001	--

The remainder of the I/O is connected from the I/O multiplexer to the UTCS CPU. The inputs selected by the multiplexer include synchronism pulses from radio-central, bus actuations, vehicle actuations, A-Phase Green Returns and control panel inputs. The multiplexer directs outputs comprised of controller commands, map data and control panel outputs.

The multiplexer configuration is composed of standard XDS I/O units as shown in Figure 1.7. The main chassis or multiplexer is a XDS Model 7929 unit. This unit contains Models 7969 and 7970 timing units, two Model 7930 cabinets and six Model 7931 cabinets. Each of the Model 7930 cabinets contain 12 Model 7951 input cards. The Model 7931 cabinets contain up to 16 cards which are composed of Model 7950 output cards, Model 7951 input cards or both types of cards. Each of the Model 7950 units has provisions for supplying 8 outputs while the Model 7951 units can accept 16 inputs. The UTCS CPU has access to 32 data points at a time.

A table indicating the multiplexer commands for selecting multiplexer data is shown in Table 1.4.

When inputting or outputting a word of data via the multiplexer, two consecutive words of buffer storage are required. The first word is the command and the second word contains the data. If for example, one wishes to read in all four words of the A-Phase

2. Programming Specifications

This section contains the programming specifications for all the UTCS and BPS routines. Each specification is composed of 5 sections describing the purpose, method, repetition rate, cross reference and flow charts. In addition, a glossary of the symbols used by the routine is contained in Section 3. There are 26 UTCS routines and 6 BPS routines which are specified in Sections 2.1 through 2.32. The present size (in 32 bit words) of each of the routines assembled is listed in Table 2.1 and their timing requirements are listed in Table 2.2. A current memory map indicating the starting location of each of these relocatable packages is contained in the latest computer listings. Note that assembled routine "BPS" contains routines BA, BB, BC, BD, BE and BF. Also routines KFMT and CRTOUT are subroutines called by Routine K. All routines were coded in the Macro-Symbol Assembly language.

Table 2.1

Size of Assembled Routines

Routine	Size (Words)
BPS	4797
A	1547
A1	44
B	92
C	361
D	605
E	216
F	94
G	78
H	4117
I	863
J	1044
K	1638
KFMT	87
CRTOUT	71
L	456
M	1292
N	102
O	58
P	82

Table 2.1

Size of Assembled Routines (cont'd)

Routine	Size (Words)
Q	102
R	64
S	207
T	249
U	66
V	370
W	364
X	102
Y	19467*

*Routine Y contains all data arrays and reserve areas

Table 2.2

UTCS/BPS Timing Requirements

Routine	Program Timing		
	(msec)	(msec/sec)	Priority level
A	0.16	5.1 +RBM*	1
B	1.4	45	1
C	0.46	103	1
D	64/20	84	2
E	30	Negligible	3
F	0.25	Negligible	3
G	0.5	1	2
H (Includes BPS)	300	0.33	3
I (Includes BPS)	400	Not Cyclical	3
J	31.5	Negligible	3
K (Includes BPS)	15	Not Cyclical	3
L	0.5	1	3
M (Includes BPS)	2	Not Cyclical	3
N	0.38	0.76	2

*RBM Timing estimated to be 10 msec/sec.

Table 2.2

UTCS/BPS Timing Requirements (cont'd)

Routine	Program Timing (msec)	Program Timing (msec/sec)	Priority level
O	0.33	0.66	2
P	8	16	2
Q (Includes BPS)	NRT**	Not Cyclical	3
R	8	16	2
S	1.5	3	2
T	6	12	2
U	0.05	0.1	2
V	2	4	2
W	45	0.05	3
X	0.5	1	2
Y (Includes BPS)	NRT**	Not Cyclical	None
BA	0.25	30	1
BB	0.6	19	1
BC	0.2	6.4	2
BD	20	20	2
BE	20	20	2
BF	1	1	2
BJ	0.5	0.5	2

**Non Real Time

2.1 Routine A (UTCS Executive) Specification

2.1.1 Purpose

The purpose of the UTCS Executive Routine is to control the sequence by which other routines are performed in accordance with pre-defined assignments of priority and elapsed time. In addition, the UTCS Executive Routine performs all multiplexer (MUX) I/O and triggers an inter-processor interrupt for the BPS CPU (CPU2).

2.1.2 Method

The UTCS Executive Routine is composed of an Executive Initialization Loop (Figure 2.1.5.1), Interprocessor Interrupt and Counter Pulse 3 Clock Tasks (Figure 2.1.5.2), a Main Loop (Figure 2.1.5.3), a Level 3 Loop (Figure 2.1.5.9) and an End Action Loop (Figure 2.1.5.8). It also schedules the Level 2 Executive, Routine A1, which controls the sequencing of all Priority Level 2 routines.

The Executive Initialization Loop is entered directly from Routine Y after it has completed its required start-up tasks. The loop sets up the priority structure of the program and allows real time processing. The loop connects tasks directly or centrally to interrupts. By connecting tasks directly, the monitor is bypassed and the user must save the environment. When tasks are connected centrally, the monitor will save the environment at the expenses of slower reaction time than that of direct connection. It should be noted that the internal clock interrupt (location X' 5A') has a higher priority than those of the external interrupts whose priority order is listed in Table 1.1.

When the 1/32 second mark occurs, the internal clock interrupt causes the monitor to transfer control to the Counter Pulse 3 clock task. This task resets the clock counter value to 250 (an internal clock pulse decrements this counter 8000 times per second resulting in a clock interrupt every 1/32 second), triggers the Interprocessor Interrupt (location X' 60') and Priority Level 1 interrupt (location X' 62'), releases the internal clock interrupt (location X' 5A') and exits to the monitor.

The monitor then transfers control to the interprocessor interrupt task which simply releases the Interprocessor Interrupt (location X' 60') so it may be triggered in the future, and returns control to the monitor. The monitor then transfers control to the Main Loop of the UTCS Executive Routine.

The Main loop updates the real time clock (RTC), sets half-second and one second flags, and decrements several scheduler clocks once per second. When a scheduler clock has counted down to zero, its corresponding Priority Level 3 routine is scheduled by setting its activity bit in the appropriate word in the Master Activity Scan Table (MAST). The next task is to decrement the Detect Buffer Pointer (DBP) and perform all multiplexer I/O. The detector Buffer Pointer is used to point to the vehicle detector array (P1, P2, P3 or P4) that is to be filled for use in the detector processing algorithm used by Routine B. After multiplexer I/O is performed, the Priority Level 1 routines (Routines B and C) are performed; if a half-second mark is encountered, the Priority Level 2 interrupt (location X'63') is triggered and the Priority Level 3 interrupt (location X'64') is triggered. Then the Priority 1 Level interrupt (location X'62') is released, and control is returned to the monitor.

If the Priority Level 2 interrupt is the highest interrupt active, control is given by the monitor to the Level 2 Executive, Routine A1. If the Priority Level 3 interrupt is the highest interrupt active, control is given by the monitor to the Level 3 loop. The Level 3 loop (Figure 2.1.5.9) controls the execution of the level 3 routines, whose order of priority is routine M, J, K, E, H, W, Q, I and L. Upon entry, the Level 3 loop scans the Master Activity Scan Table (MAST) from top to bottom for a word having an activity bit (A) present and a Service bit (S) absent. If no word can be found, the Priority Level 3 interrupt (location X' 64') is released and control is returned to the monitor. If a word is found, the "A" bit is reset and the control bit (C) is set in MAST, and the corresponding Priority Level 3 routine is executed. The last step in this routine is to reset its "C" bit is MAST and return control to the Level 3 loop which scans MAST from the top of the table again. If a routine suspends itself while waiting for I/O completion, it sets its "S" bit and returns control to top of the Level 3 loop for another scan of MAST. Upon completion of I/O operation, control is eventually returned to the routine via the End Action Task and the Level 3 loop. Note that if a routine is scheduled (that is, its "A" bit is set in MAST), while waiting for I/O service (that is, its "S" bit is set in MAST), it is not given control until the completion of I/O operation. The only Priority Level 3 routines that may wait for I/O servicing are Routines H, I and W.

The Level 1 Executive is also responsible for the scheduling of the computer evaluation routines for both CPUs. Once per minute a flag (WMINF) is set to inform the BPS CPU to start its evaluation. Upon completion of its evaluation, the BPS routine (Routine BJ) clears WMINF and schedules Routine L in the UTCS CPU. If WMINF has not been cleared by the next minute mark, the Level 1 Exec schedules Routine L and a SINGLE COMPUTER mode of evaluation is imposed by setting CPFLG=1.

2.1.3 Repetition Rate

The clock interrupt causes this routine to be entered every 1/32 second.

2.1.4 Cross Reference

The routine controls all other UTCS routines.

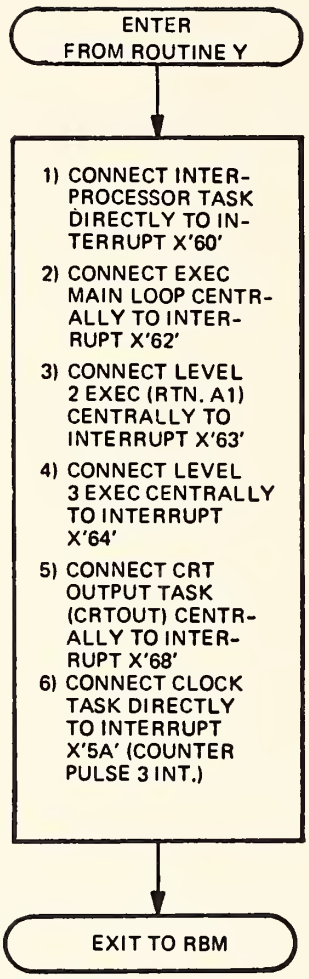


FIGURE 2.1.5.1. ROUTINE A SPECIFICATION
(EXECUTIVE INITIALIZATION LOOP)

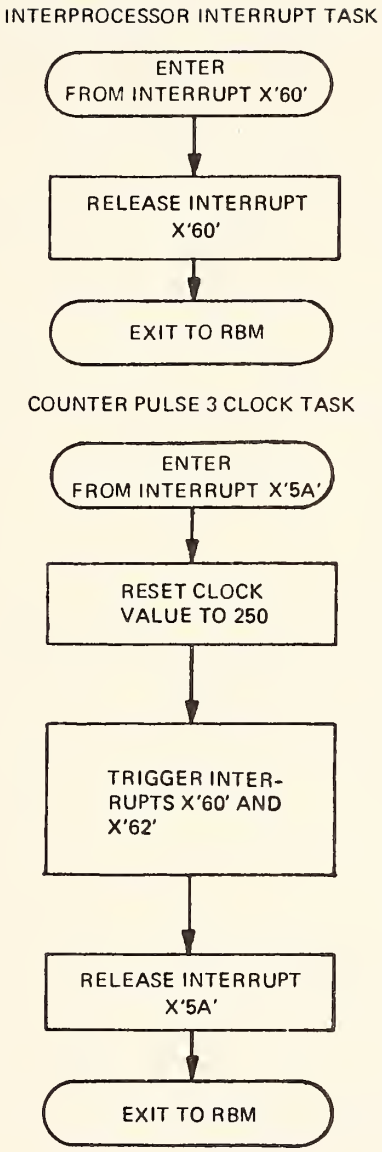


FIGURE 2.1.5.2. ROUTINE A SPECIFICATION (INTERPROCESSOR INTERRUPT TASK, COUNTER PULSE 3 CLOCK TASK)

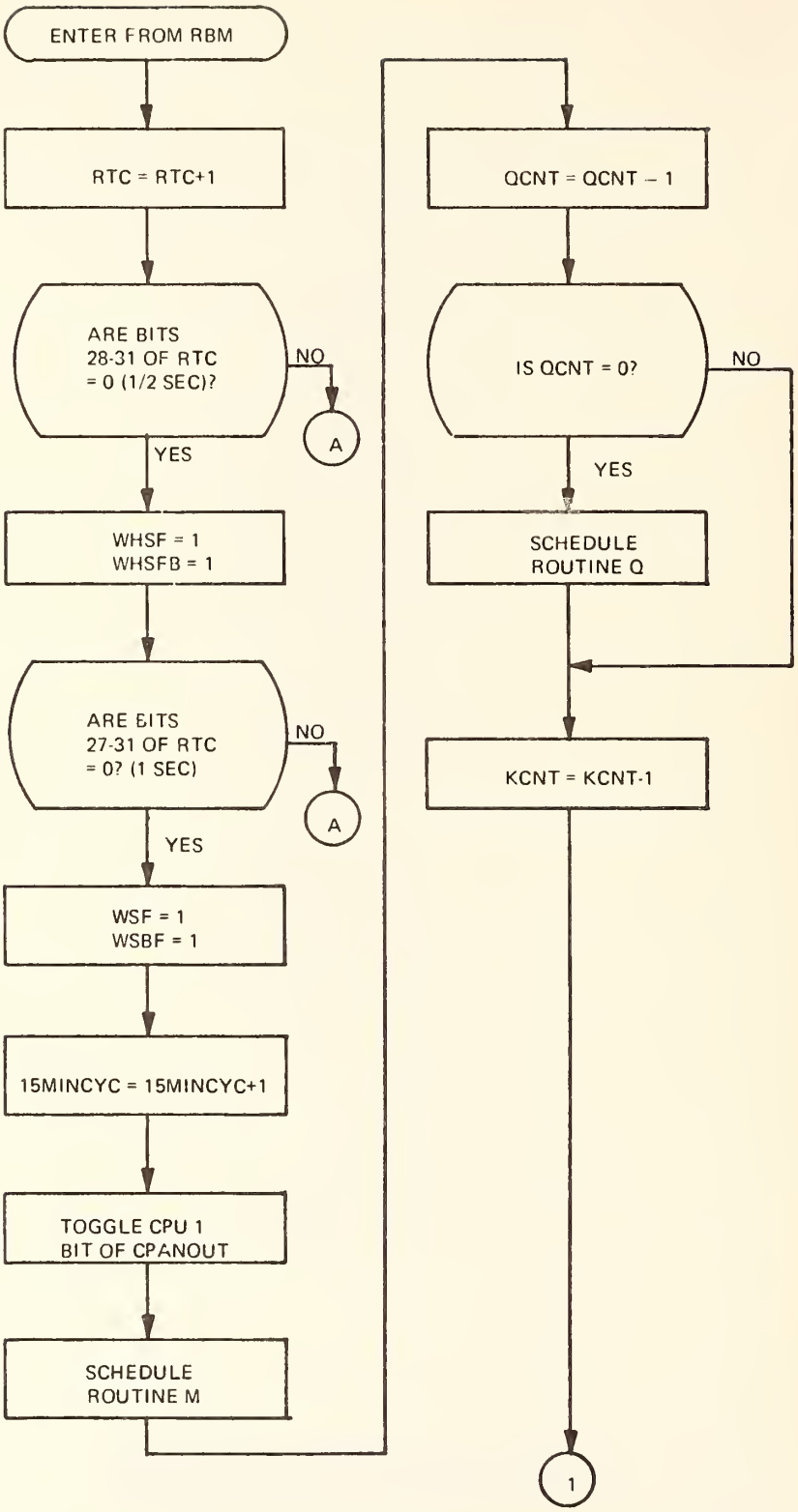


FIGURE 2.1.5.3. ROUTINE A SPECIFICATION (MAIN LOOP)

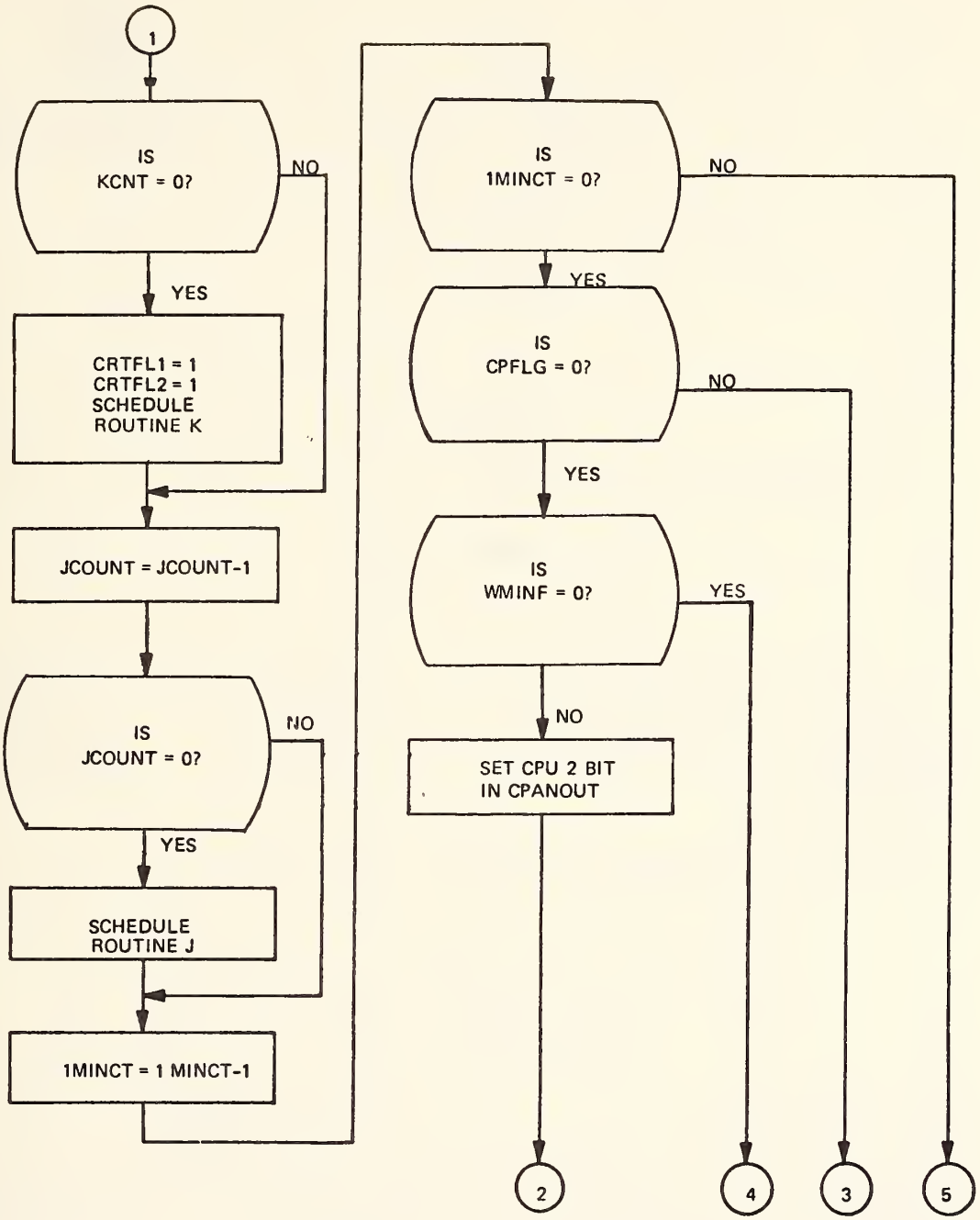


FIGURE 2.1.5.4. ROUTINE A SPECIFICATION
(MAIN LOOP)

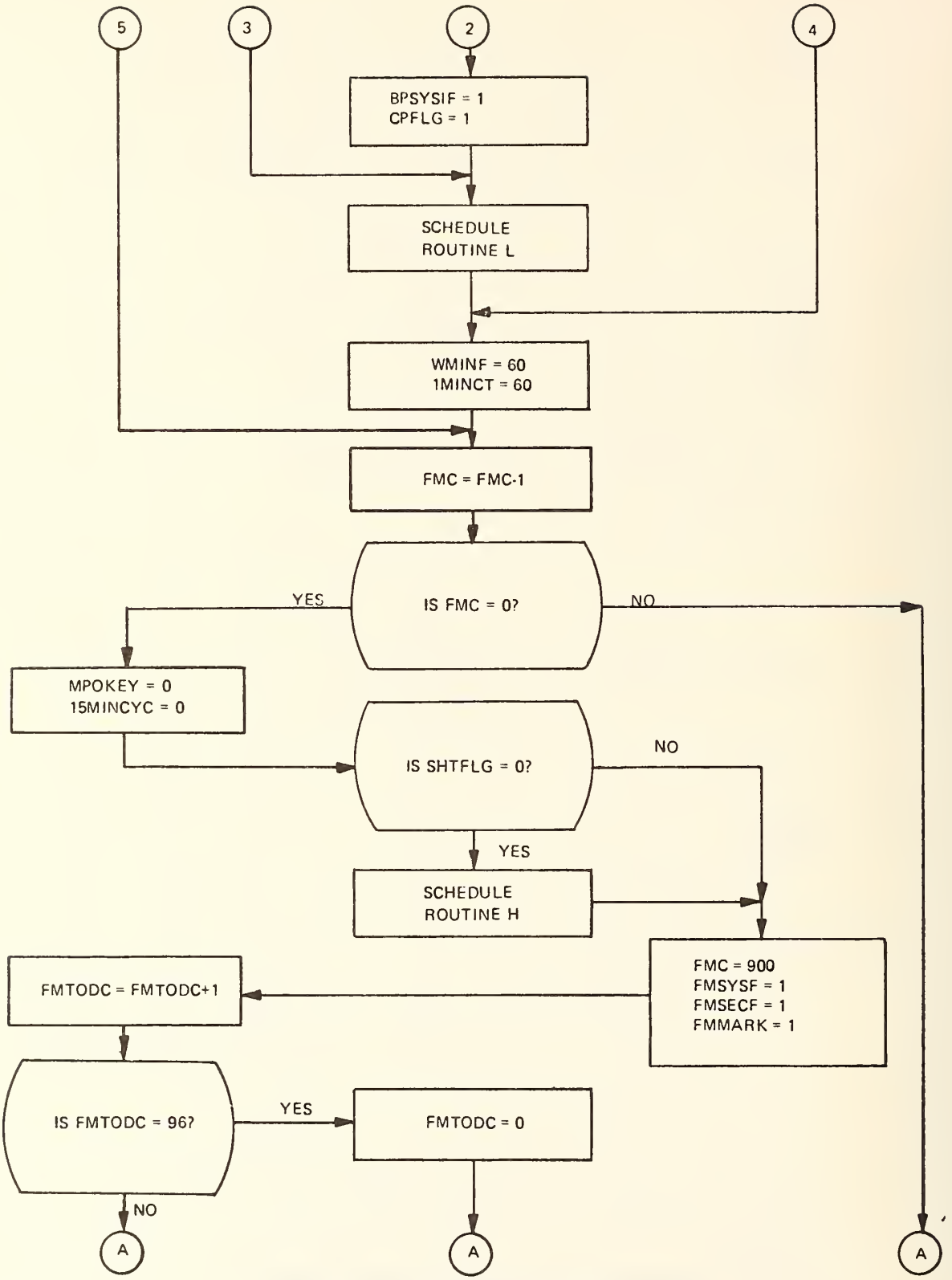


FIGURE 2.1.5.5. ROUTINE A SPECIFICATION
(MAIN LOOP)

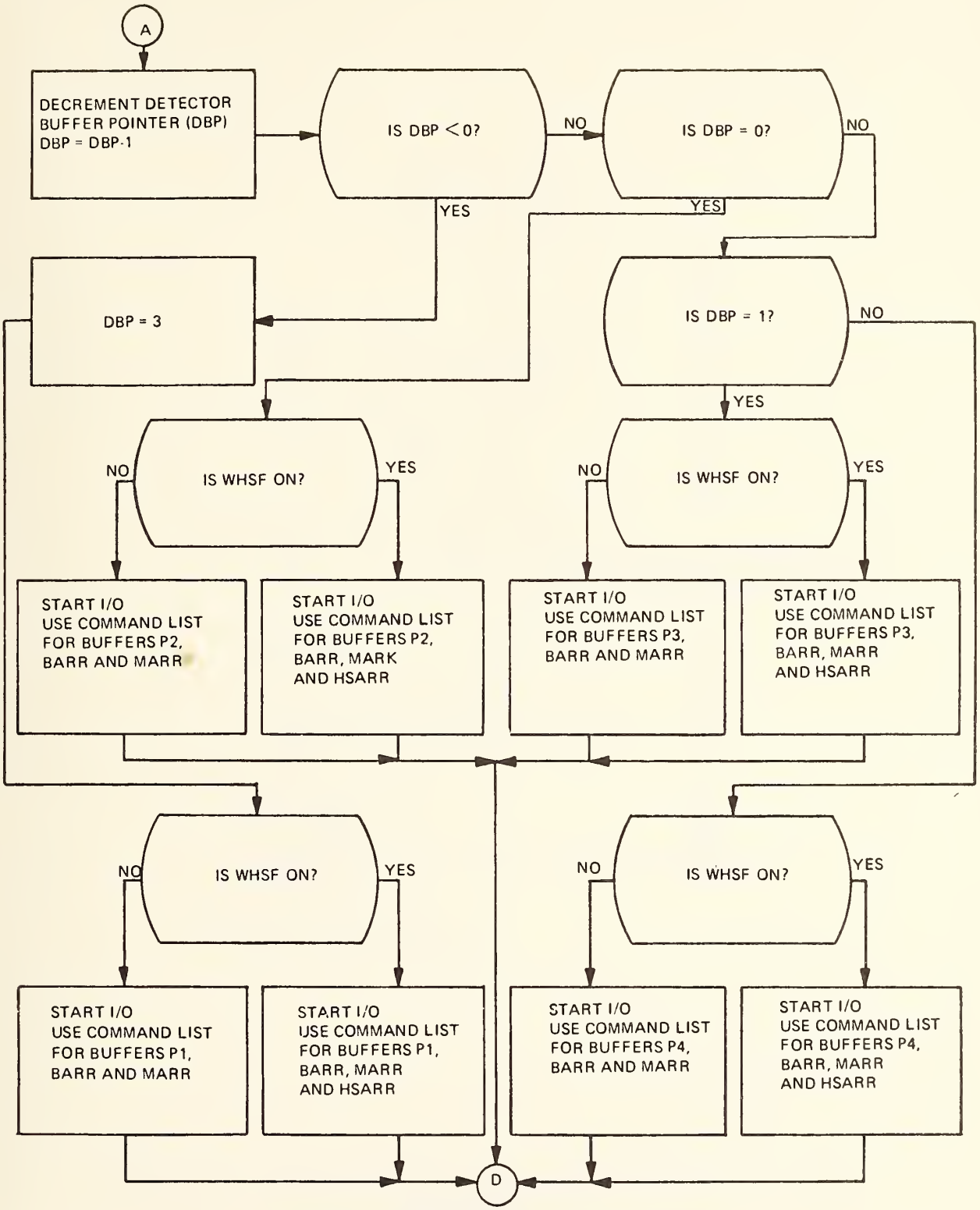


FIGURE 2.1.5.6. ROUTINE A SPECIFICATION
(MAIN LOOP)

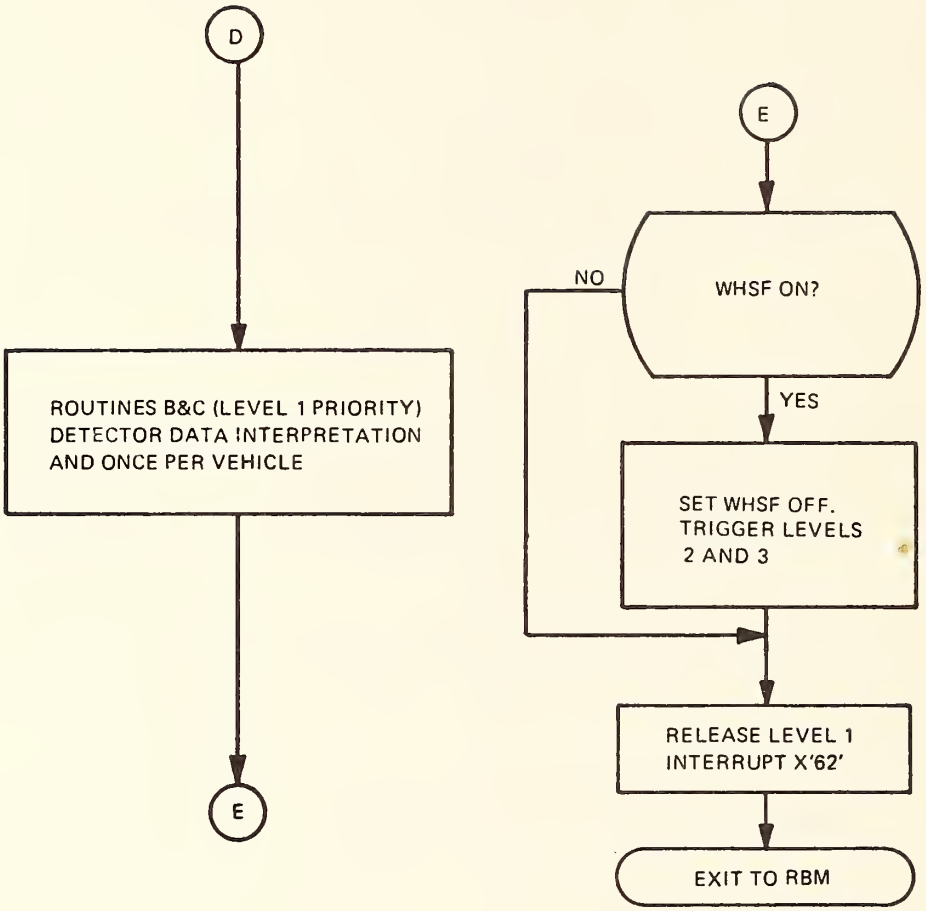
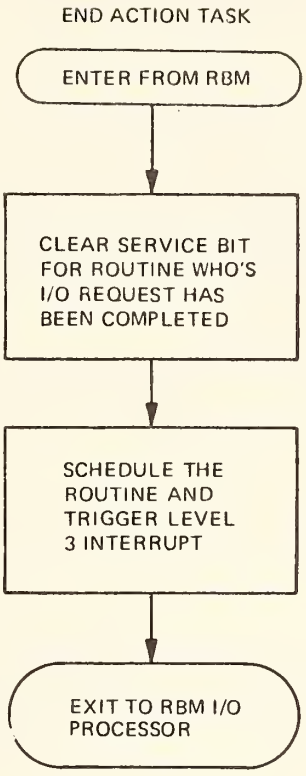


FIGURE 2.1.5.7. ROUTINE A SPECIFICATION
(MAIN LOOP)



AT PRESENT, ONLY THE FOLLOWING LEVEL 3 ROUTINES REQUEST END ACTION:

1) RTN. H
2) RTN. I
3) RTN. W

FIGURE 2.1.5.8. ROUTINE A SPECIFICATION (END ACTION TASK)

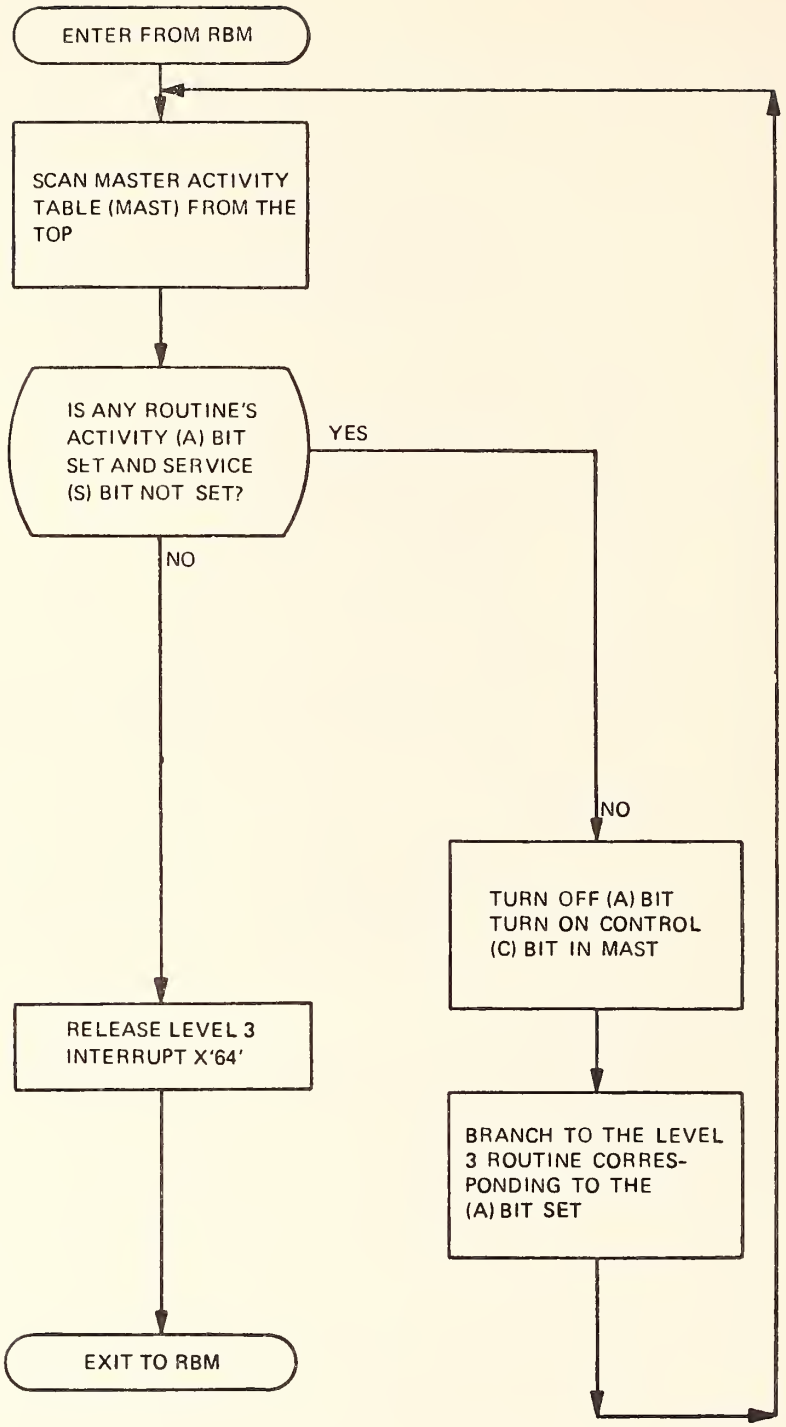


FIGURE 2.1.5.9. ROUTINE A SPECIFICATION
(LEVEL 3 LOOP)

2.2 Routine A1 (Level 2 Executive) Specification

2.2.1 Purpose

This routine will control the execution of the controller do-loop by scheduling the routines in the loop when their functions are required.

2.2.2 Method

The Level 2 Executive Routine decides whether a Priority Level 2 routine is to be entered. If system parameters and/or flags indicate that the routine is required, it is scheduled, otherwise it is not entered for that pass through the loop. The loop is executed completely 2NCWRD (currently 4) times. During each pass, a scheduled routine handles 32 controllers.

The Level 2 Executive routine also supplies common inputs to the routines of the loop, such as the do-loop index (I) and the byte index base (K).

2.2.3 Repetition Rate

This routine is entered every 1/2 sec.

2.2.4 Cross Reference

This routine represents the control routine for Level 2 and calls Routines D, N, P, R, T, V, and X. It is entered from RBM via the Level 2 interrupt and exits to RBM.

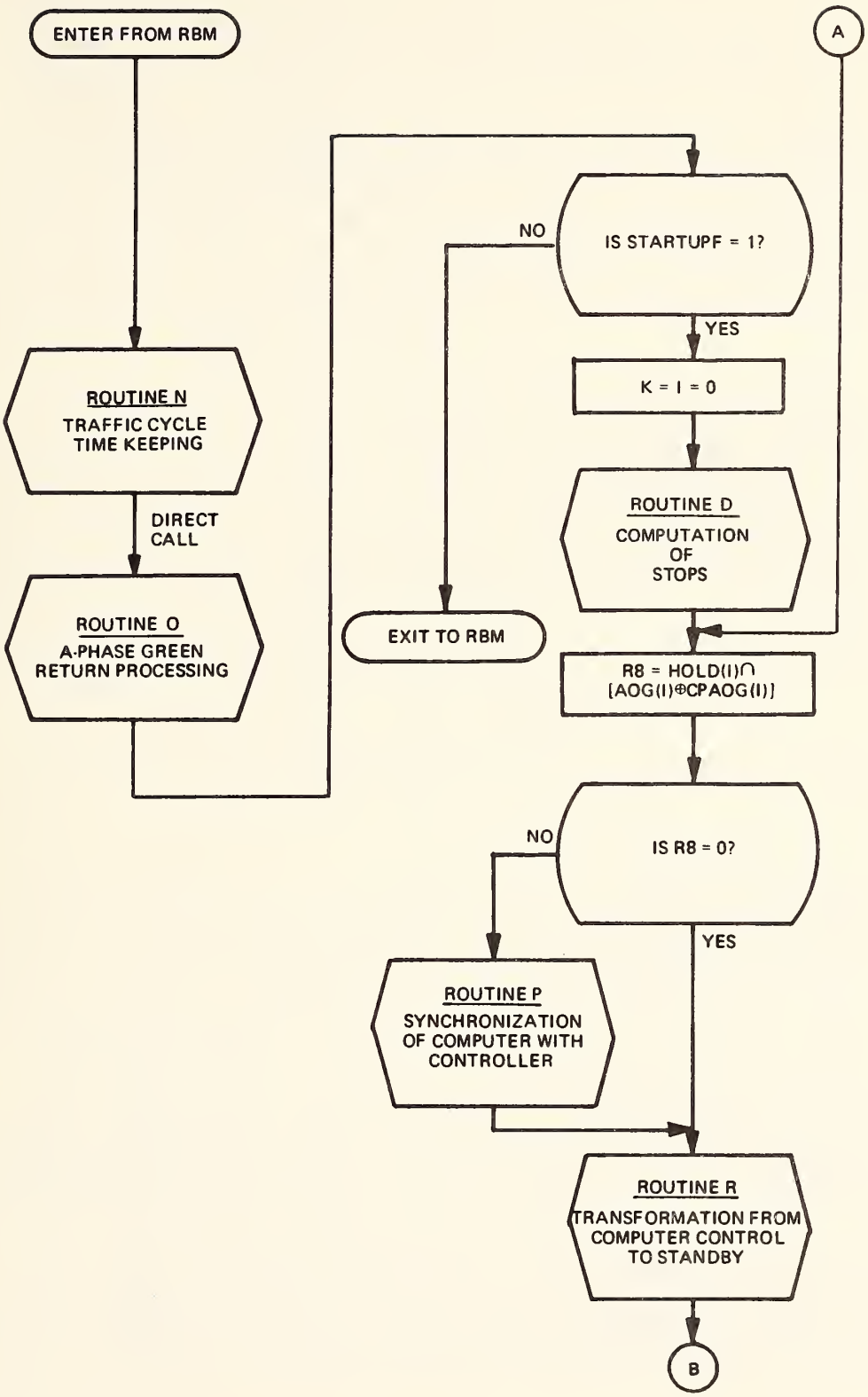


FIGURE 2.2.5.1. ROUTINE A1 FLOW CHART

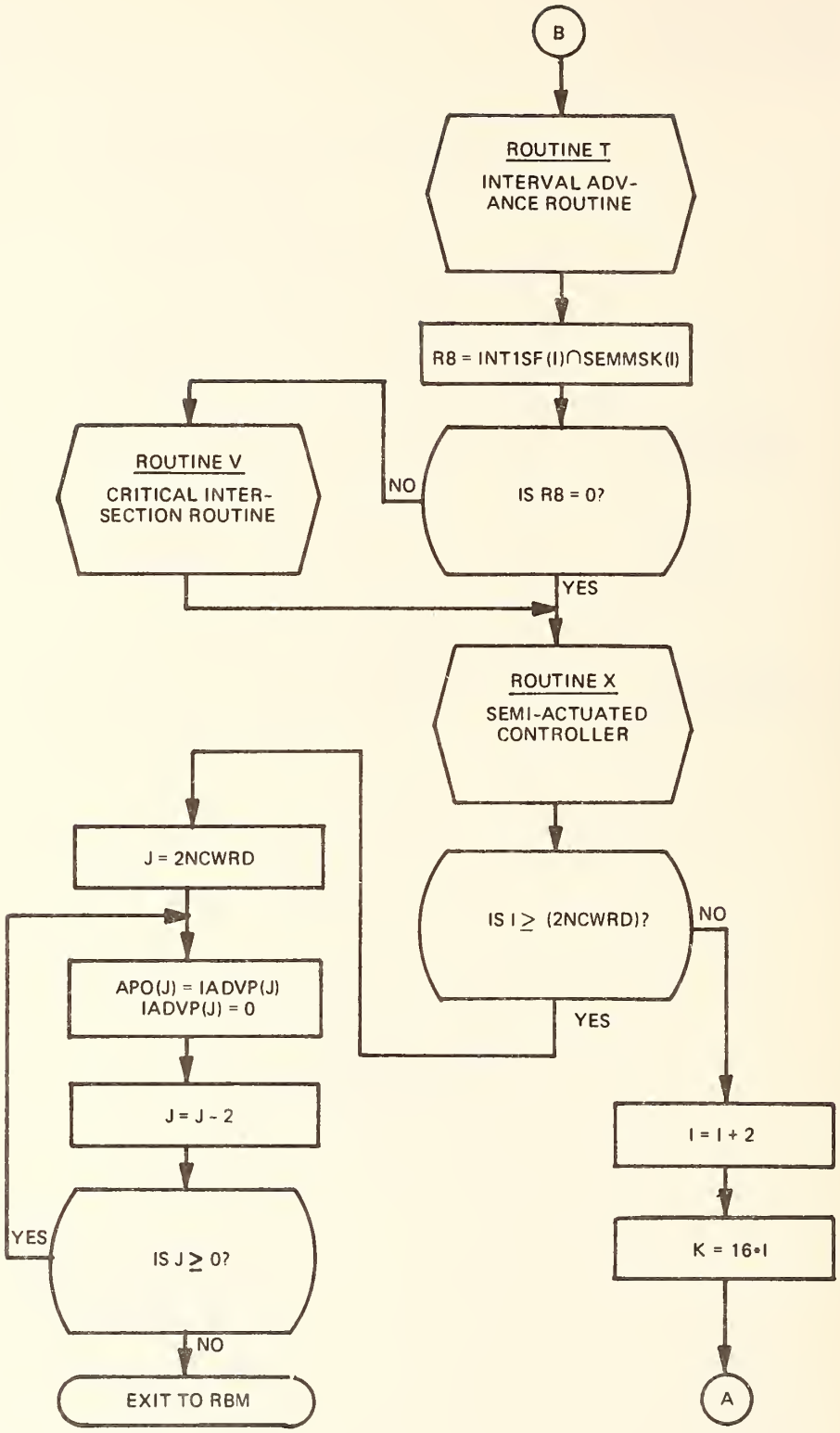


FIGURE 2.2.5.1. ROUTINE A1 FLOW CHART

2.3 Routine B (Detector Data Input and Interpretation) Specification

2.3.1 Purpose

The purpose of Routine B is to examine the vehicle detector arrays for an indication of vehicle presence. From this indication, the routine records the start time and duration (presence) of each vehicle passage. Whenever an end of vehicle is sensed, the Once per Vehicle Routine, Routine C, is performed. Changes in detector states are ignored if the state does not remain stable for at least 2 sampling times (1/16 second).

2.3.2 Method

This routine is entered every 1/32 seconds from the Executive Routine, Routine A. All detector data is stored by the Executive Routine in an array of packed words, one bit per detector. This routine will unpack the detector words and identify those detectors that have changed state since the last pass through this routine. Those detectors that have had a change in state are checked to determine whether the change indicates the beginning of a vehicle or the end of one. In order to reduce the effect of spurious pulses, logic is used to indicate a "change of state" only when the input presence indications have maintained the same state for at least two scan periods.

Each time an end of vehicle is identified, the routine computes the total time that the vehicle spent in the particular detectors field of sensitivity; that is, the presence in seconds.

When an end of vehicle pulse is processed, this routine enters the Once per Vehicle Routine, Routine C. After Routine C is completed, control is returned to this routine and the next detector indicating a change in state is processed. After all detectors have been examined, and all those needing processing have been processed, control is returned to the Executive Routine.

The technique used in Routine B is a word oriented quadruple buffer scheme. Three buffers are required to determine if changes in detector states remain stable for 2 sampling times. The fourth buffer is provided to allow new data to be inputted from the MUX while the other three buffers are being processed.

Upon entry, the routine initializes counters and examines the Detector Buffer Pointer (DBP) to determine which three buffers are to be processed. The first step is to determine if two changes of state have occurred in the past 2 samples for a particular bit

(detector) in the Ith word. If two changes of state have occurred (indicating a spike or a gap), the change in this particular bit is ignored by complementing the respective bit in the previous (middle) data word and W. W is the exclusive OR (denoted by the symbol $\oplus$) of the previous data word and data word two samples ago, and indicates bit positions in which the previous changes of state lie.

Irrespective of whether two changes of state have occurred or not, W is tested to determine if at least one bit has changed state. If there is at least one bit with a change, indicated by a logical "one", each of the 4 bytes that comprise W are examined to see if they contain any "ones". If a particular byte X is not zero, the detectors corresponding to the non-zero bits of X are isolated. If TSTART(K) is positive, the change in state of the Kth detector represents the beginning of a vehicle presence and the present real time is stored in TSTART(K) with a negative sign. If TSTART(K) is negative, the change in state of the Kth detector represents the end of vehicle presence, hence the pulse duration TT is computed, the present real time is stored in TSTART(K) with a positive sign, and the Once per Vehicle routine, Routine C, is performed. After all the detectors with changed states in byte X have been processed, the remaining bytes in W are examined. After all 4 bytes in W have been examined and processed, when required, the next word from the three vehicle detector buffers is analyzed. When the entire buffer has been analyzed, the routine is exited.

2.3.3 Repetition Rate

This routine is entered every 1/32 second from the Executive Routine, Routine A.

2.3.4 Cross Reference

This routine is called by the Executive Routine every 1/32 second and returns to that routine.

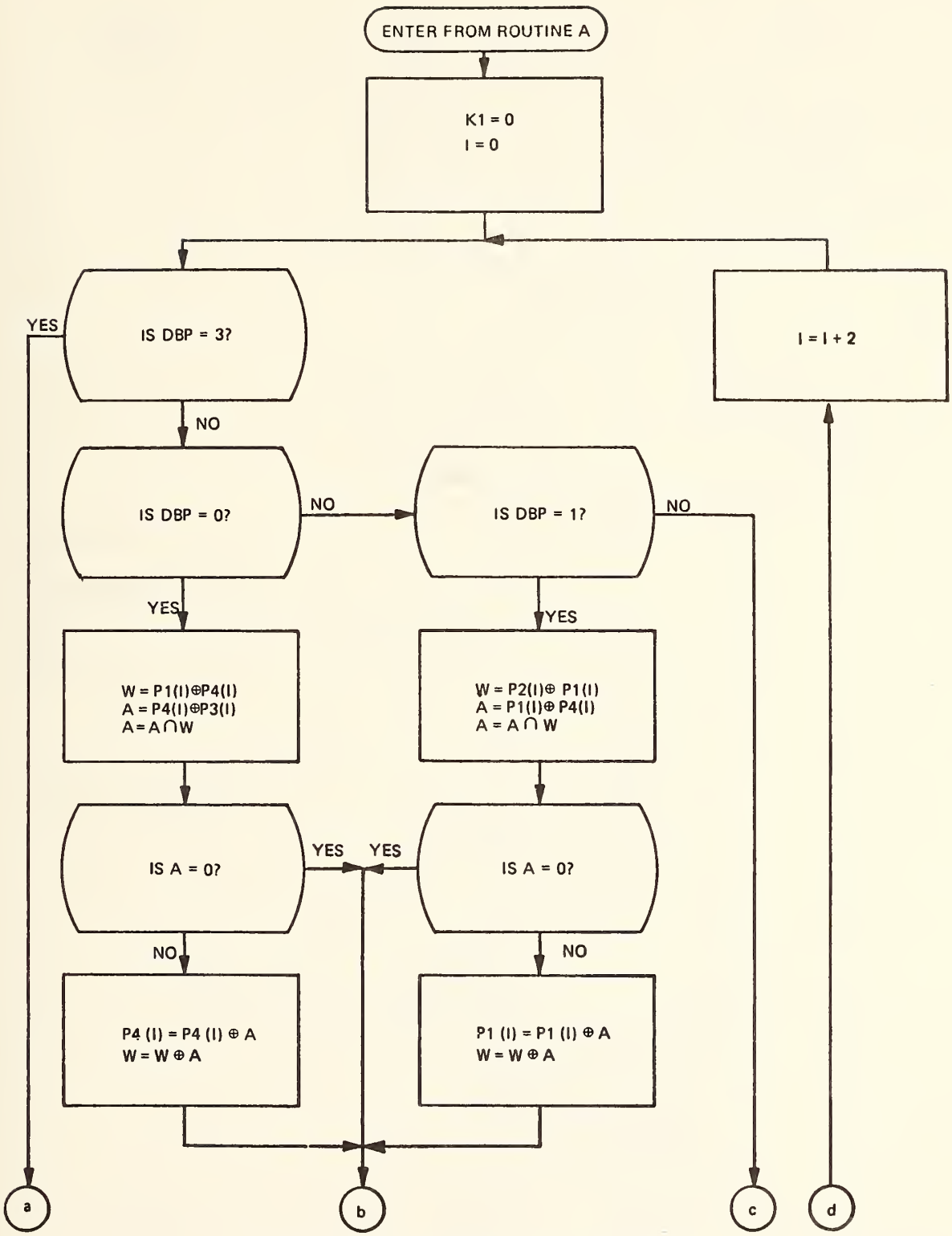


FIGURE 2.3.5.1. ROUTINE B SPECIFICATION

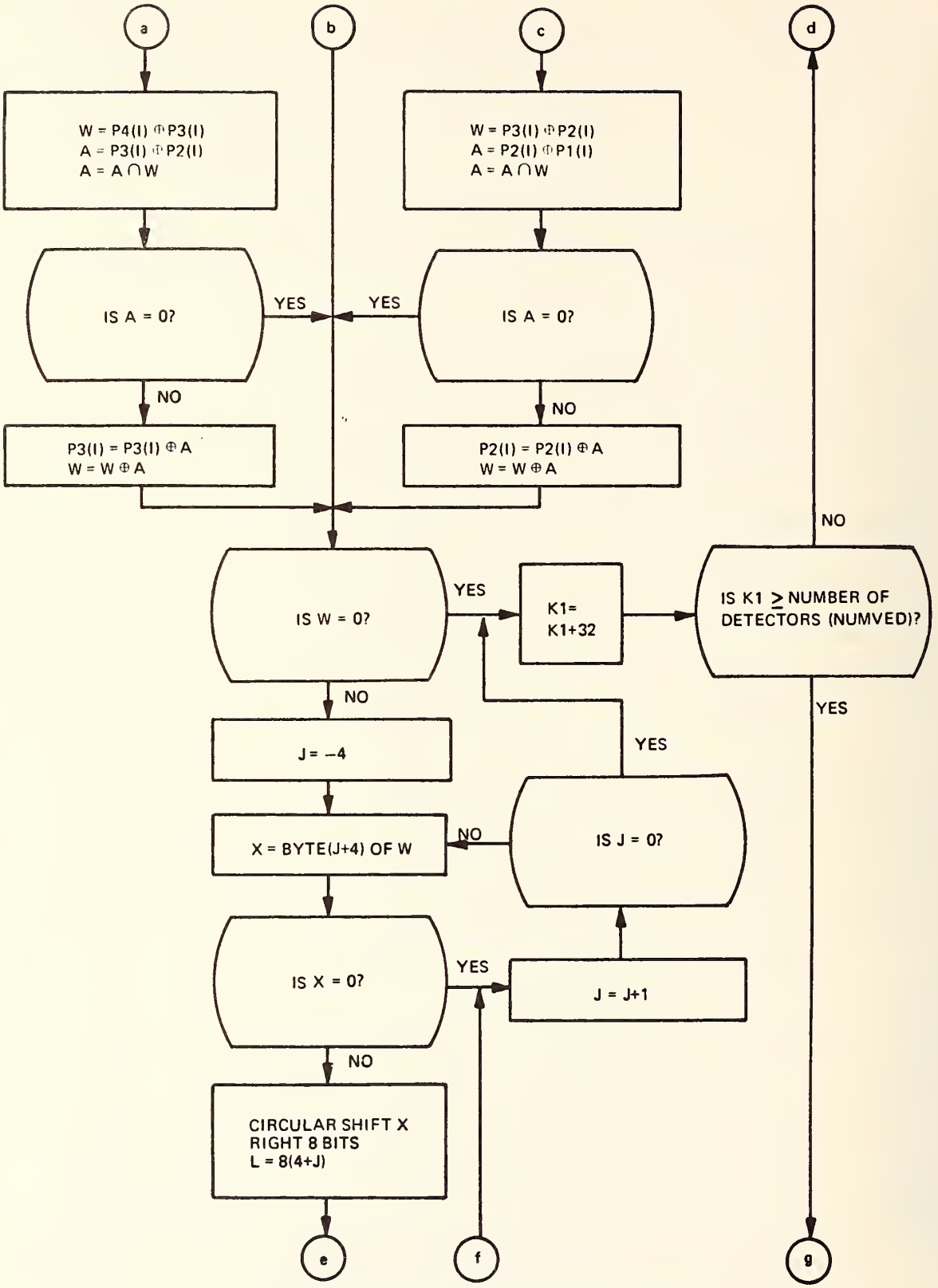


FIGURE 2.3.5.2. ROUTINE B SPECIFICATION

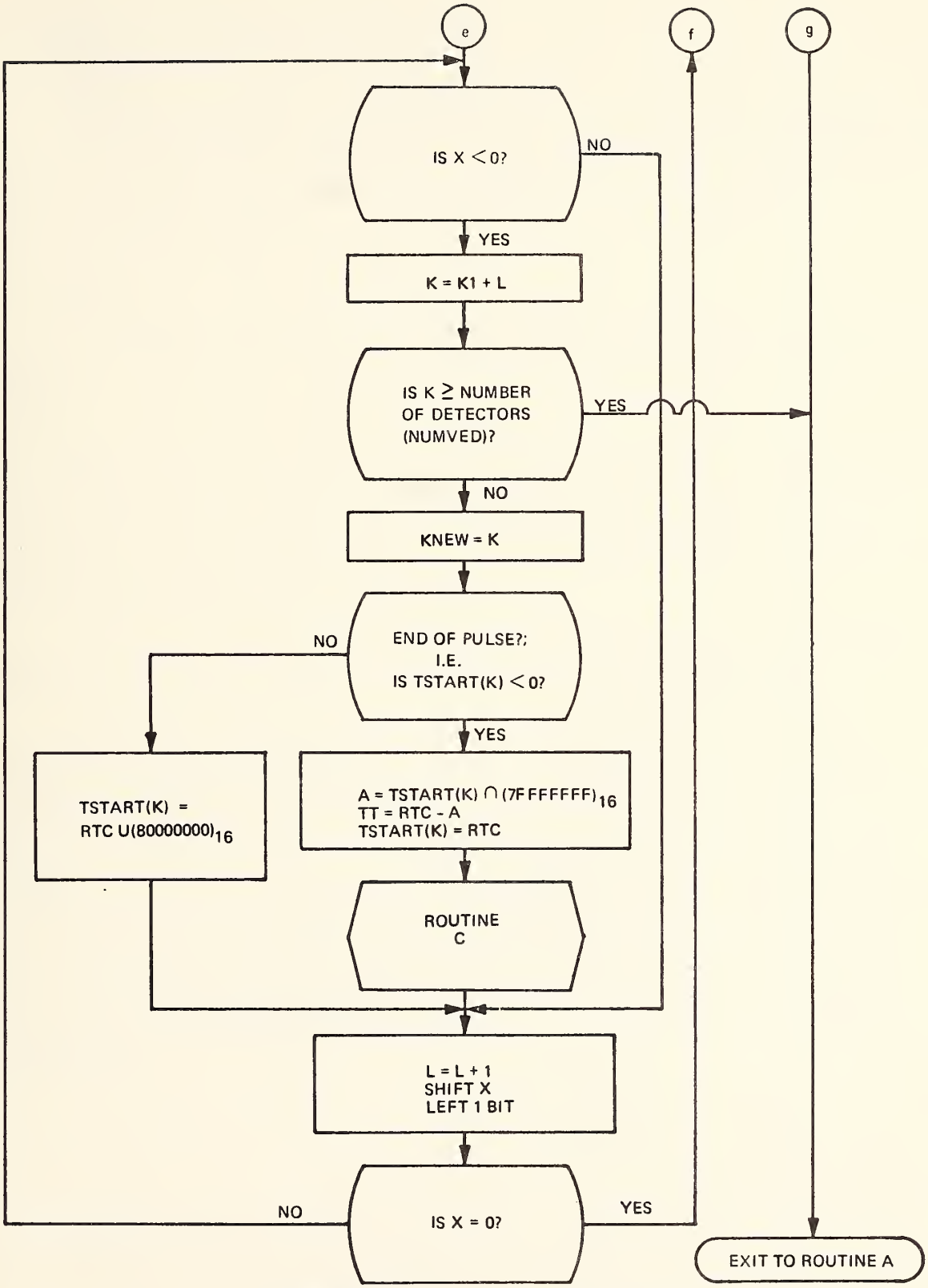


FIGURE 2.3.5.3. ROUTINE B SPECIFICATION

2.4 Routine C (Once per Vehicle) Specification

2.4.1 Purpose

The purpose of Routine C is to accumulate raw car counts, raw occupancy and raw speed, corrected for bias, for each detector; to update smoothed zone count; to set flags for timing the computation of stops; and to update smoothed vehicle pulse width for each upstream queue detector crossing.

2.4.2 Method

The technique used in Routine C is detector oriented. Whenever an end of vehicle is sensed in Routine B, Routine C is entered, and upon completion, control is returned to Routine B.

After the Detector Obstruction Flag, DOF(K), has been reset, the link number J corresponding to detector number K is determined. If there is a defective detector on this link, the routine is exited. Otherwise, the corrected pulse length, TTC, the raw occupancy, RAWOCC, and raw speed, RAWSP, are computed for this detector. If detector K is the only detector on link J, the routine is exited.

If the detector presently being processed is one of a set used to determine link zone count, this routine will update the smoothed value of zone count as follows:

The detector is referenced with respect to link and position on the link and, therefore, the zone(s) within its influence. (The i-1st zone is defined as that section of the link between the ith and the i-1st detectors.) If the appropriate stop flags are set, an estimate of zone count will be computed (table look up) based on the vehicle pulse width information. The estimate is then smoothed by weighted past values. The stop flags are set and reset in Computation of Stops, Routine D, and indicate those vehicles which will join the existing queue and those vehicles which will join the existing queue if a BPS extension is granted. In addition, each sensed vehicle is added or subtracted from the appropriate zone count accordingly, as the vehicle enters or leaves the particular zone or zones indicated.

In addition, the vehicle pulse width measured at the 2nd or 3rd detector in each link (so instrumented) is filtered. These filtered values are used by the Computation of the Stops Routine, routine D, in estimating the queue for the associated link.

Upon completing the processing of the present detector the routine exits to the Detector Data Input and Interpretation Routine, Routine B.

2.4.3 Repetition Rate

This routine is asynchronous. It is entered once per vehicle per detector, i.e., each time a detector senses the end of a vehicle.

2.4.4 Cross Reference

This routine is called by Routine B and returns to that routine.

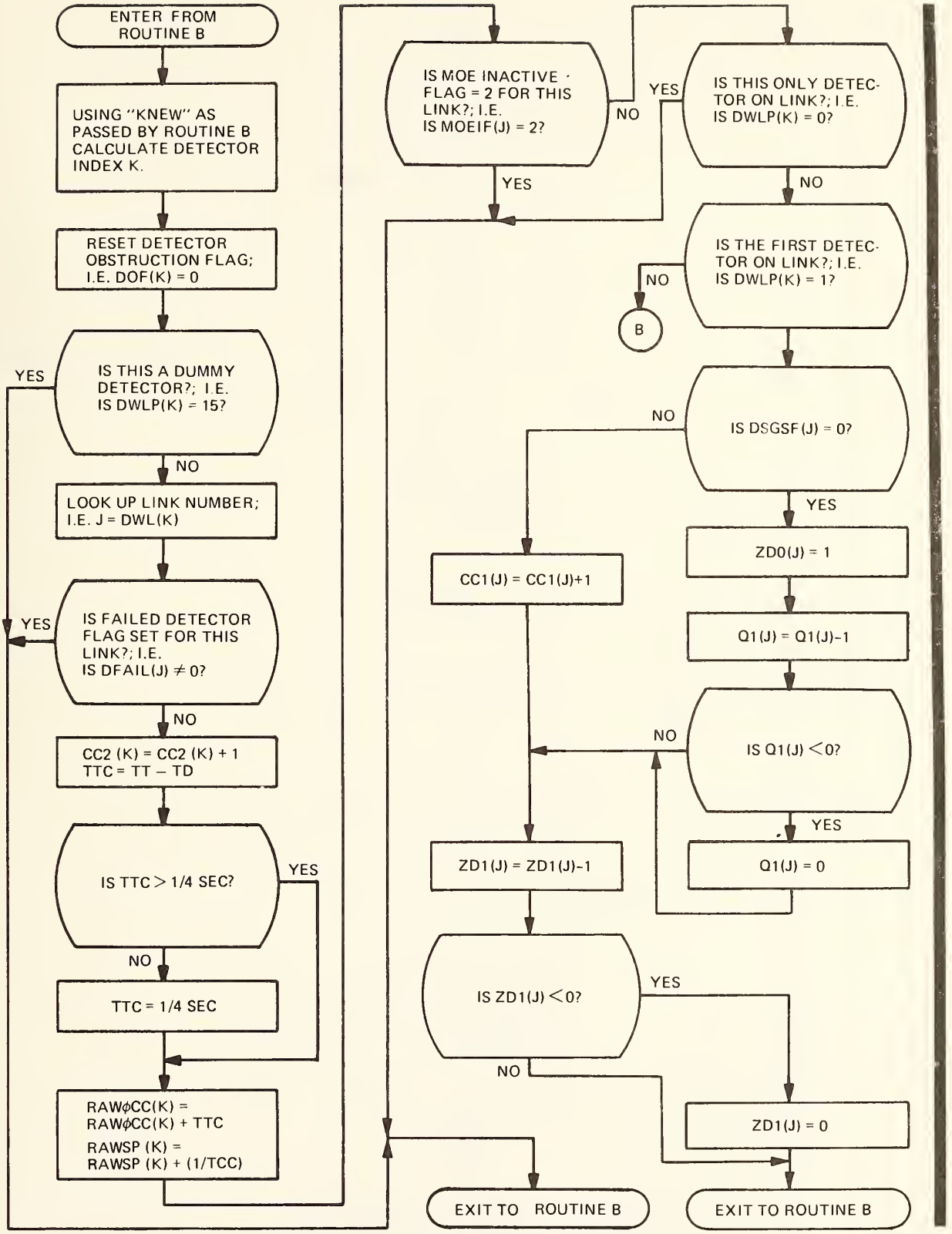


FIGURE 2.4.5.1. ROUTINE C FLOW CHART

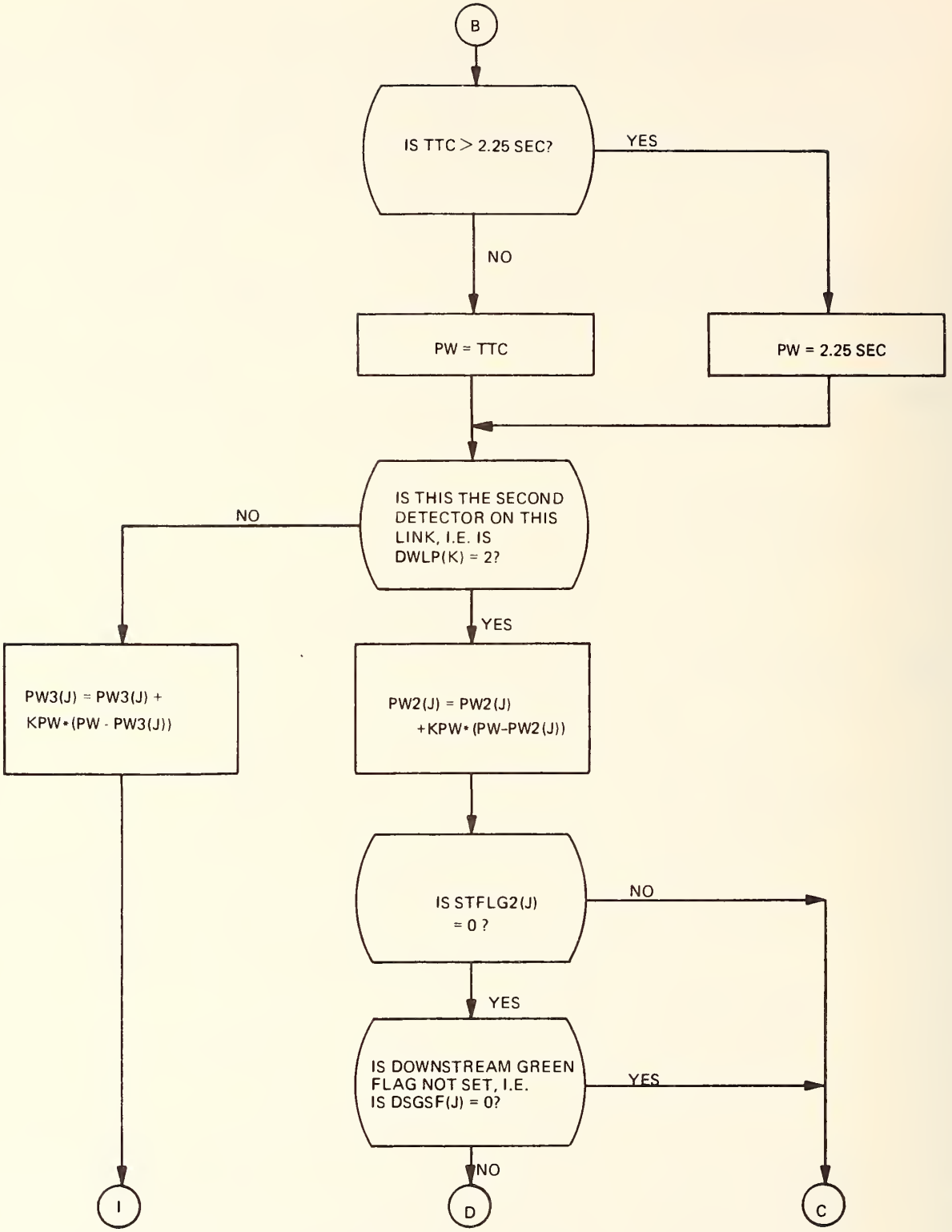


FIGURE 2.4.5.2. ROUTINE C FLOW CHART

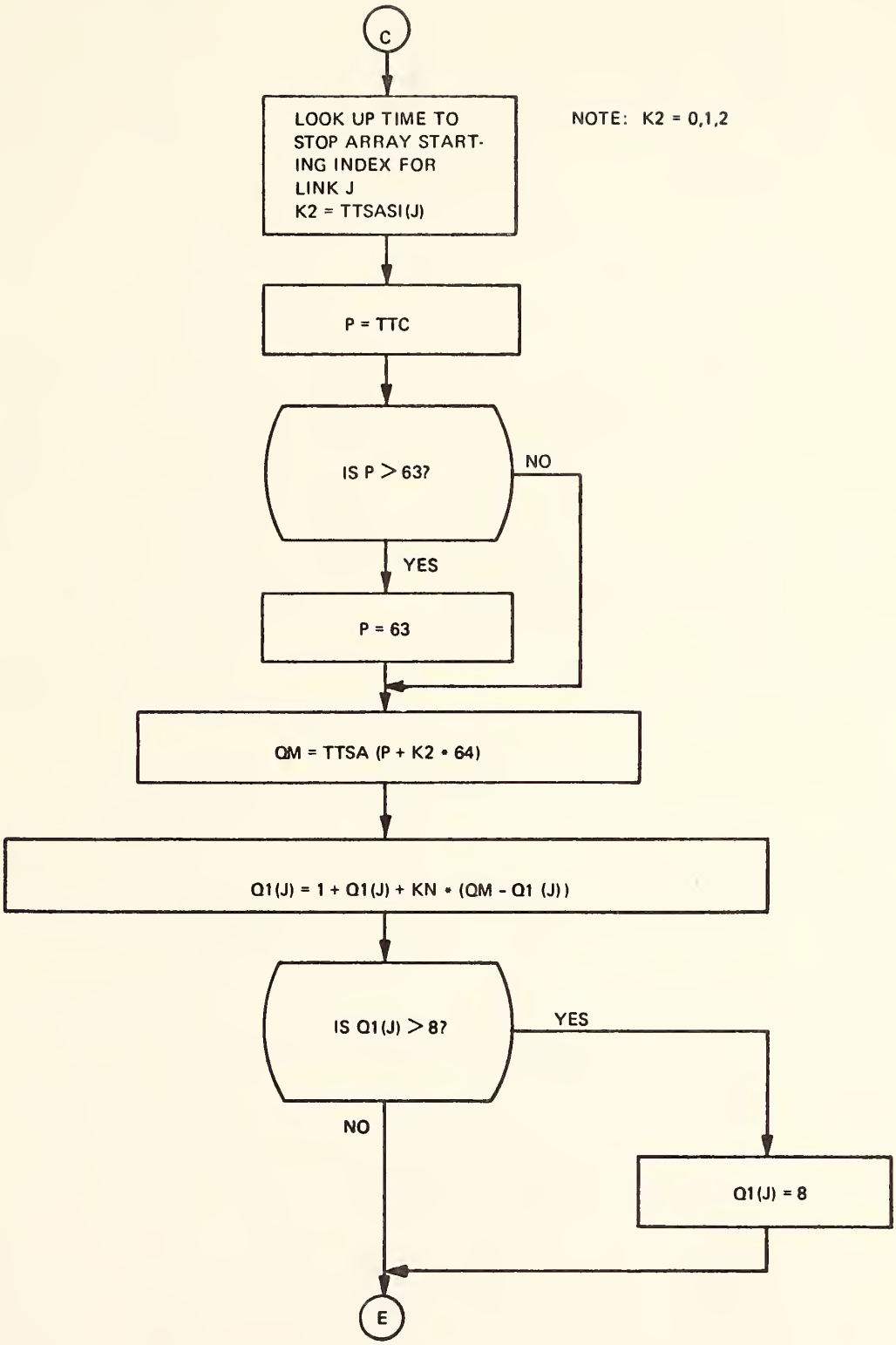


FIGURE 2.4.5.3. ROUTINE C SPECIFICATION

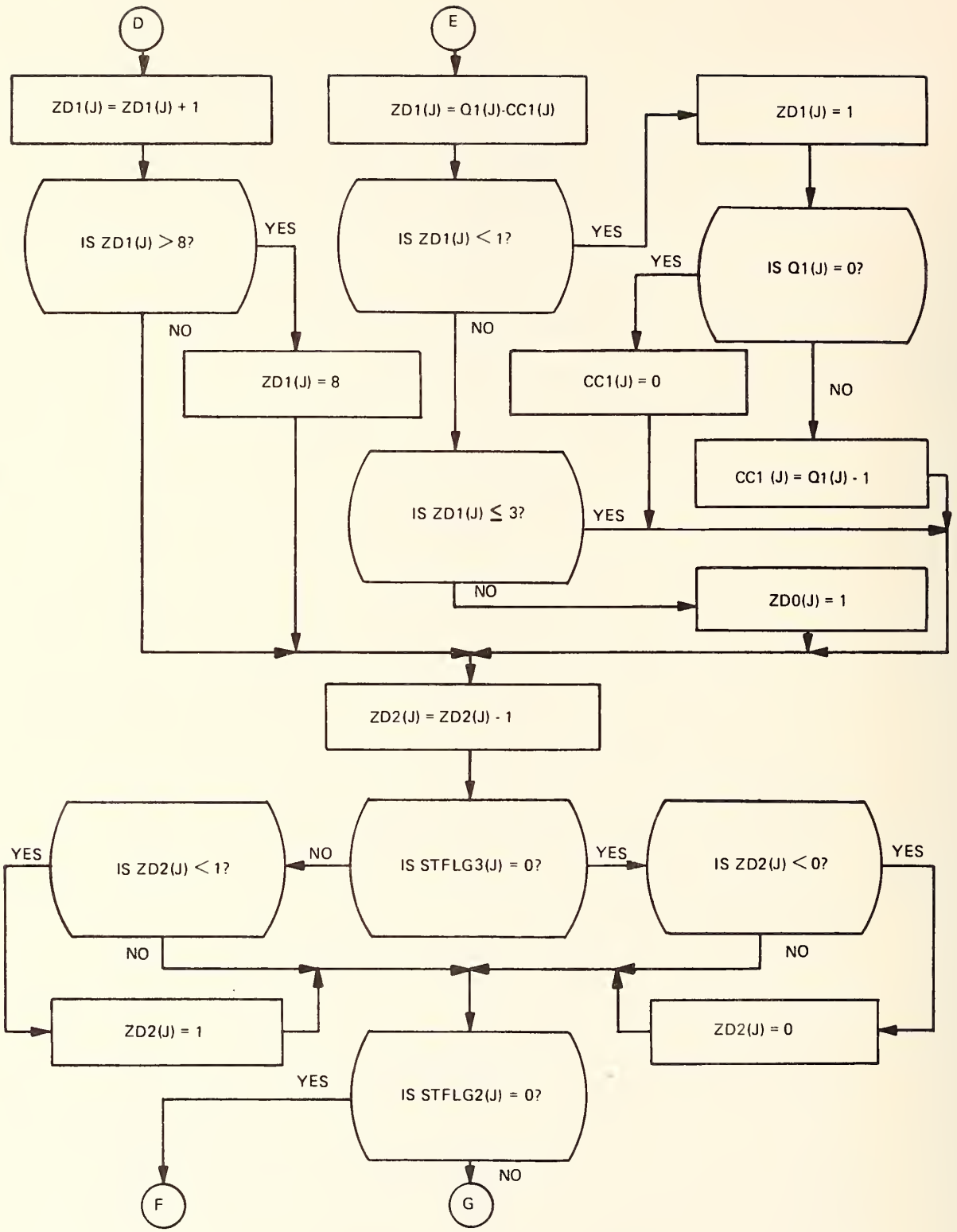


FIGURE 2.4.5.4. ROUTINE C FLOW CHART

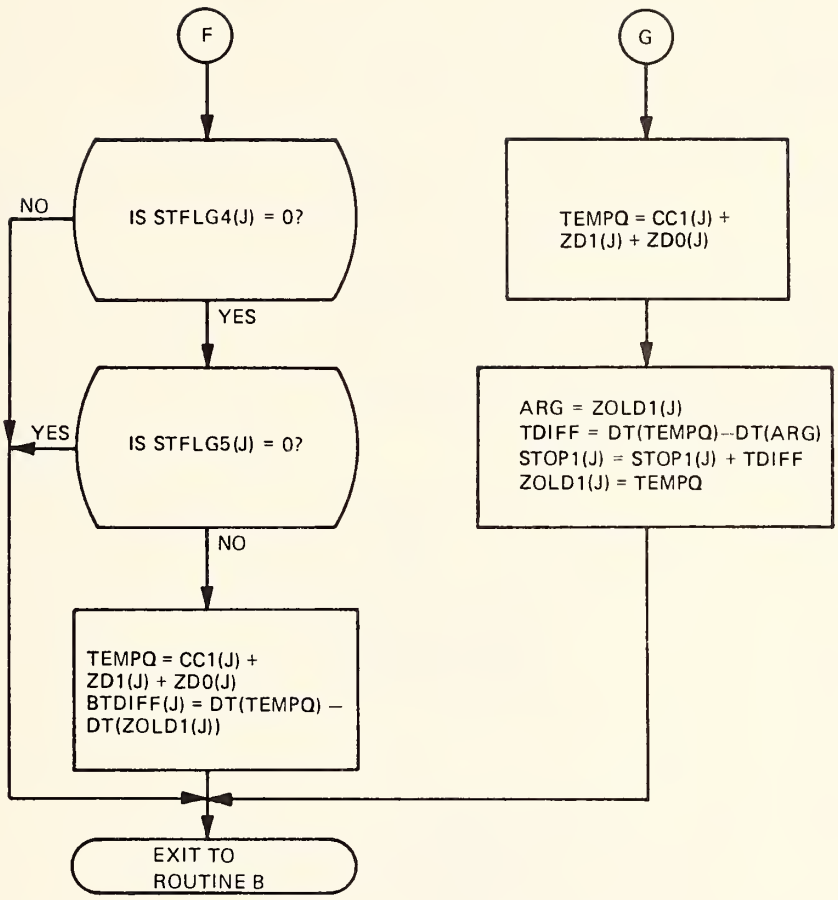


FIGURE 2.4.5.5. ROUTINE C FLOW CHART

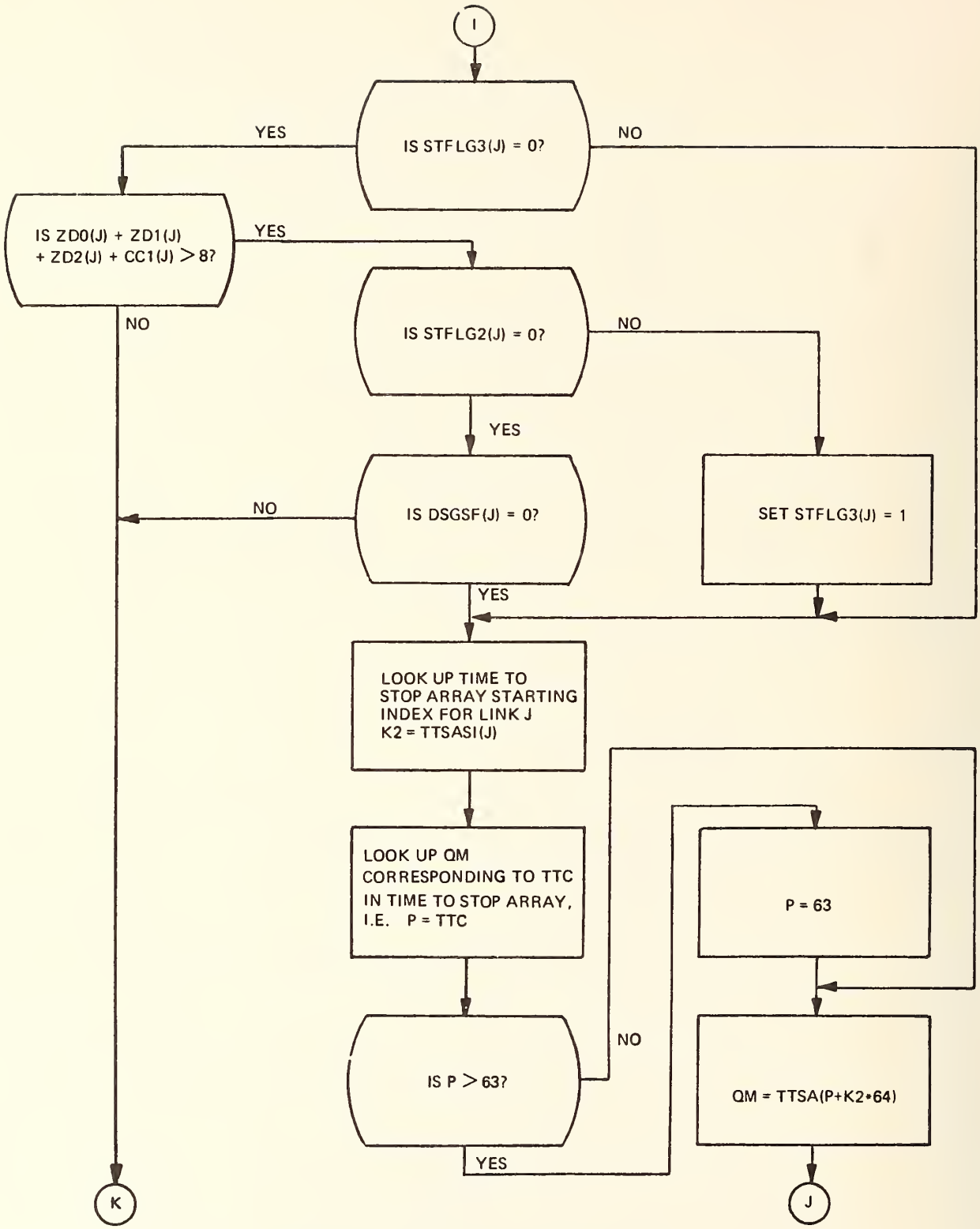


FIGURE 2.4.5.6. ROUTINE C SPECIFICATION

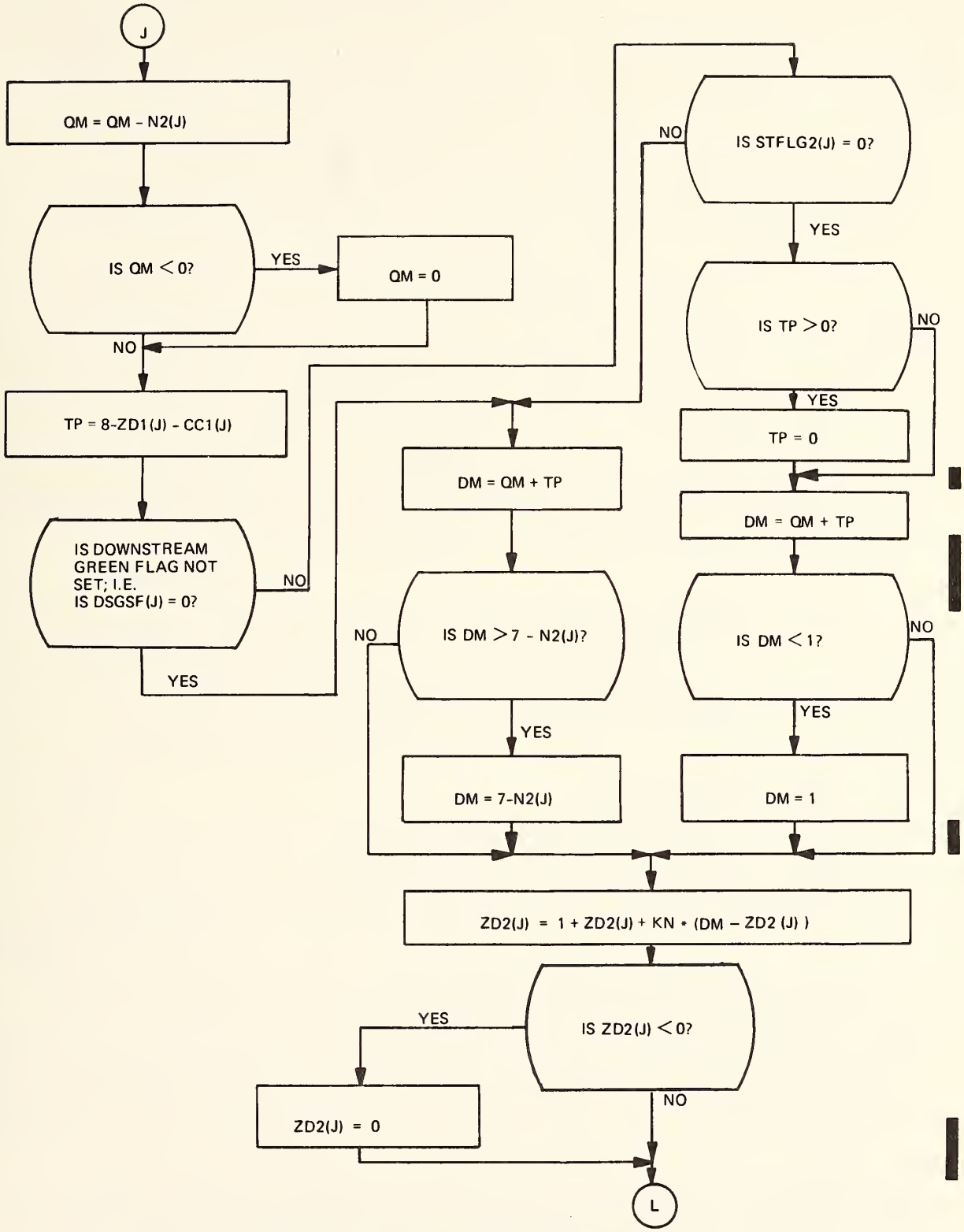


FIGURE 2.4.5.7. ROUTINE C FLOW CHART

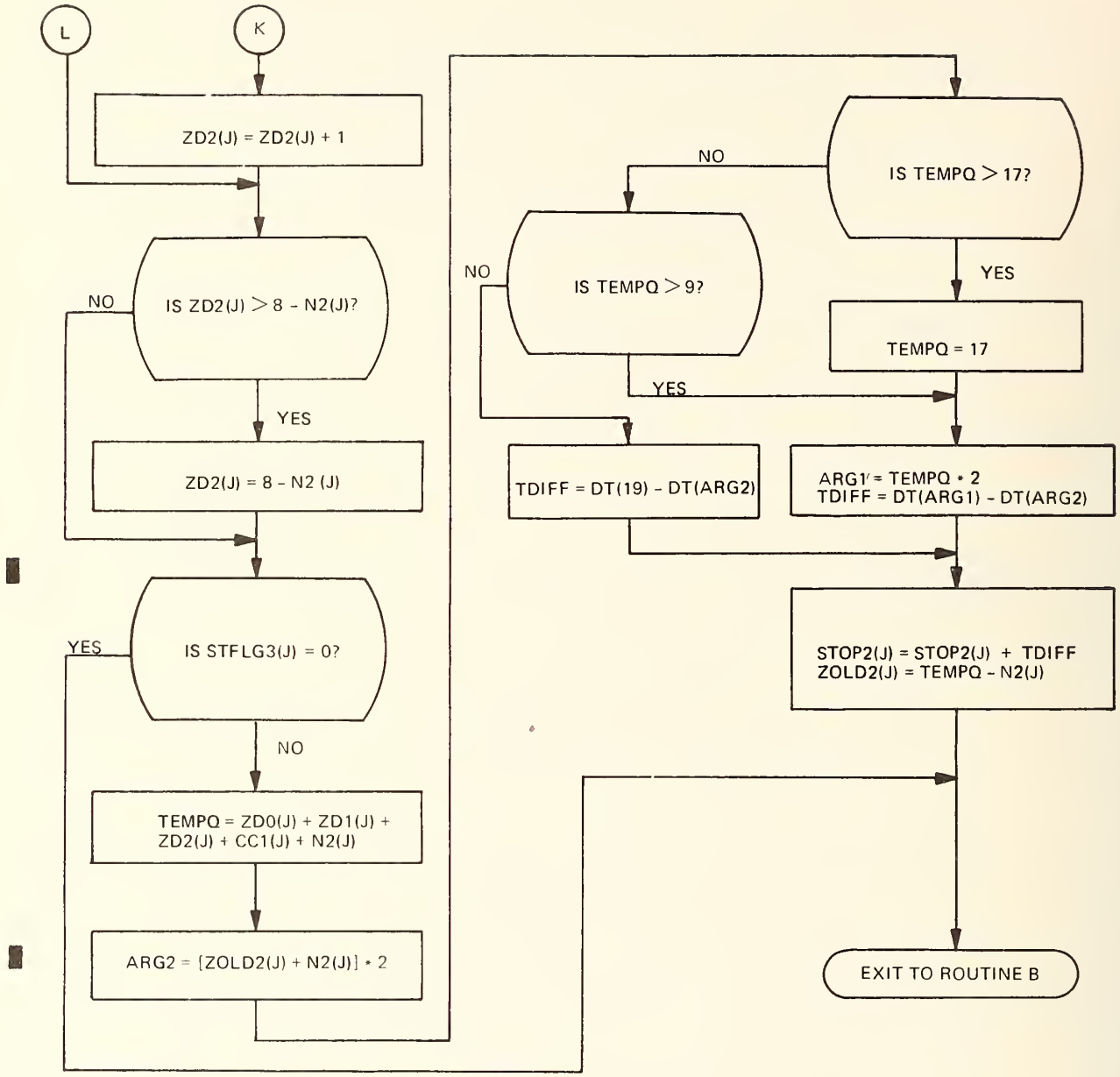


FIGURE 2.4.5.8. ROUTINE C FLOW CHART

2.5 Routine D (Computation of Stops) Specification

2.5.1 Purpose

This routine will perform the following functions:

a) Initialize and update the stops clocks.

b) Compute the number of stops per link for each link, once per cycle, when indicated by the stops clock.

c) Set up the stop flags to govern the computations of various measures of effectiveness.

d) Sample and smooth queue, once per cycle, at the start of the link green phase.

e) Update the 15-minute smoothed queue and numter of stops accumulation.

f) Compute link delay.

g) Grant bus priorities and perform the computations required to adjust the stop flags which govern the various MOE's, the stop clocks, and the appropriate controller interval.

h) Sample and smooth the count of vehicles out of the link once per controller cycle at start of the red phase for each instrumented link.

i) Sample and smooth stopped queue once per cycle at the start of the green phase for each instrumented link.

2.5.2 Method

This routine is called every 1/2 second by the Executive Routine. There are two major branches to the routine. Each branch is traversed on alternate passes through the routine. One branch processes all MOE 1 parameters while the other processes all MOE 2 parameters. *

The first branch is entered on odd "1/2 second clock" counts and each link stop clock** is decremented by one second and tested. For those clocks that have been counted down to zero, appropriate adjustments are made to Stop Flag 2 (STPFLG 2), Stop Flag 3 (STEPFLG 3), and Stop Flag 5 (STPFLG 5). These flags are defined in the Glossary.

---

* Appendix 4.7.8 describes the function and the calculation of MOE 1 and MOE 2 periods.

** Appendix 4.7.6 describes the stops calculation algorithm and the action of the stop clocks in this algorithm.

The bus priority extension flag for each link is tested. If an extension flag has changed to the "one" state, then the appropriate stop flags are set, the stop clock is adjusted to reflect the extension, the extension is granted by adjusting the appropriate controller "count down register" and the period reduction flags are set to reduce the subsequent MOE 1 and 2 periods and controller interval. The number of stops on this link are then computed when the stop clock has been counted down to zero, or the downstream signal is green, or the current downstream green interval has ended.

After all stop clocks have been decremented, the list of controllers is scanned for all MOE controllers* that are on line. For those MOE and CIC controllers which are on line, the MOE 1 periods for each controller, as computed in the Controller-Link Cross Reference and Timing Routine, Routine G, are loaded into the appropriate MOE 1 clocks and these clocks are then counted down to zero. At the end of each MOE 1 period, the "downstream green flags" are set or reset for the links associated with the controller MOE 1 clock being processed, and the "count of vehicles" out of the links during the present cycle are smoothed (summed with exponentially weighted past values). If the MOE 1 Period Reduction Flag is set, the next MOE 1 period is reduced by the length of the working Bus Priority extension in use.

In addition, the stopped queue is computed for the associated links which have started a green period and the "QVOK" Flag is set to indicate the validity of the smoothed data. The QVOK Flag, the smoothed value of count of the vehicles out of the link during the current cycle and the stopped queue estimate are used by the "Critical Intersection Routine", Routine V.

The second branch of this routine is entered on the even "1/2 second clock" counts. As done for MOE 1 clocks in the odd half-second branch, the MOE 2 clocks are processed for each on-line MOE Controller. The MOE 2 periods, as computed in Routine G, are loaded into the appropriate MOE 2 period clocks and each clock is decremented by one second each time this branch is entered. When an MOE 2 clock becomes zero, Stop Flags 2, 3, and 4 are set for the associated links. If the MOE 2 Period Reduction Flag is set, the next MOE 2 is reduced by the length of the working Bus Priority extension in use.

---

* MOE controllers are all controllers having multi-detector links. All CIC controllers are necessarily MOE controllers. However other controllers which are incapable of CIC action due to insufficient instrumentation or other causes are also included in this category.

In addition, the "Stops Clock" corresponding to the green link is reinitialized, and if the present queue is greater than 9 cars, Bus Priorities are inhibited at that intersection.

2.5.3 Repetition Rate

This routine is entered once every 1/2 second from the Level 2 Executive Routine, Routine A1.

2.5.4 Cross Reference

This routine is called by the Level 2 Executive Routine, Routine A1, and returns to that routine.

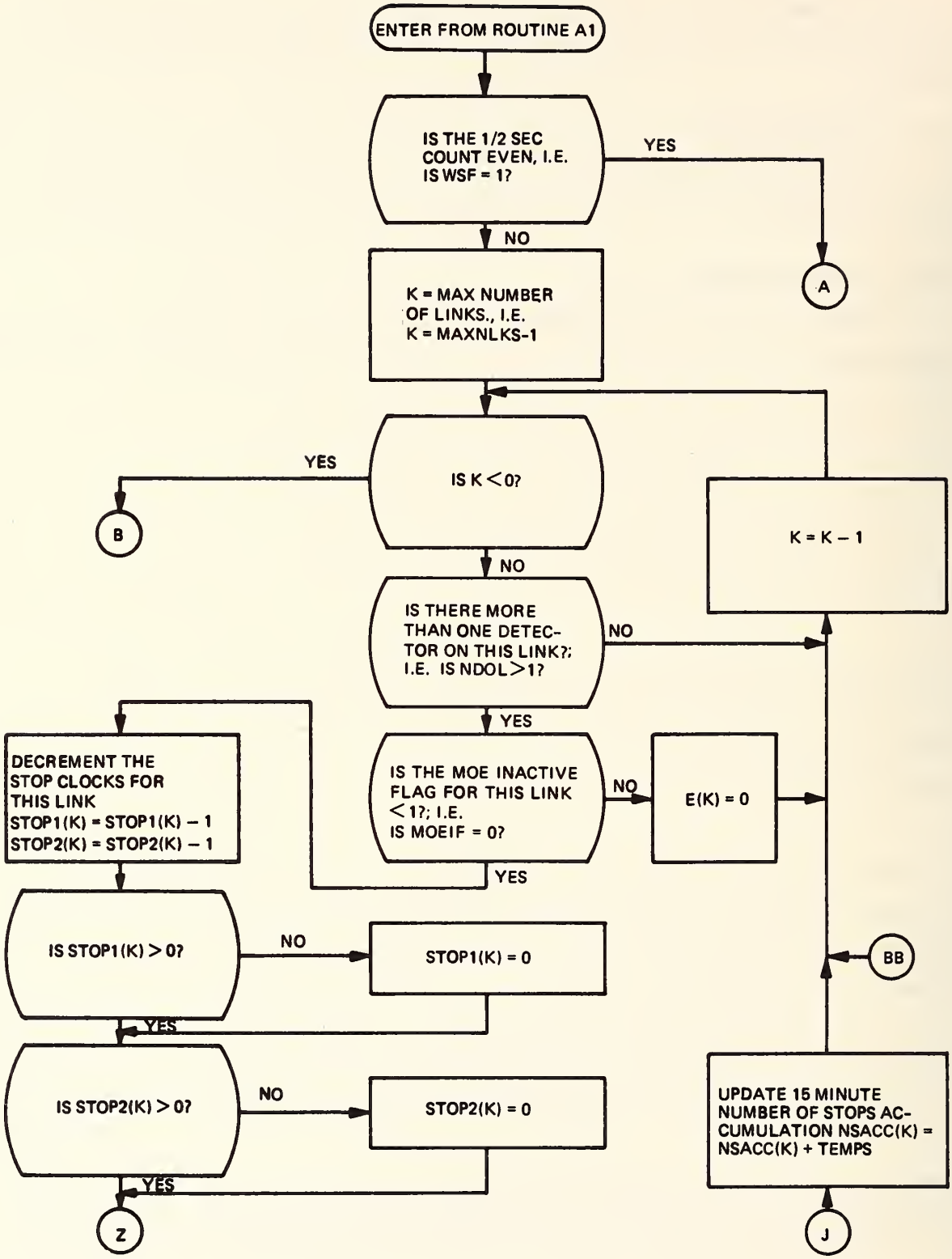


FIGURE 2.5.5.1. ROUTINE D FLOW CHART

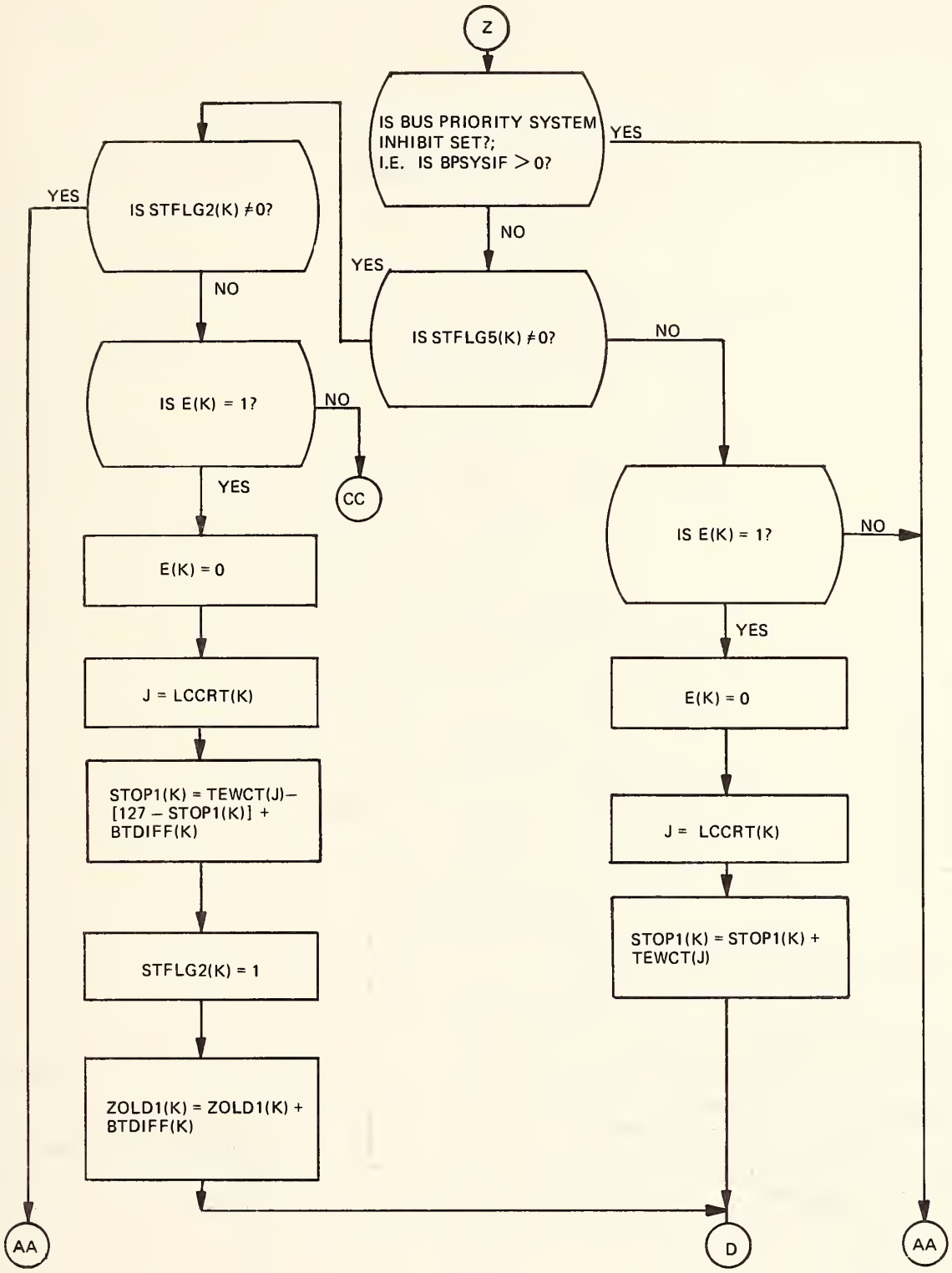


FIGURE 2.5.5.2. ROUTINE D FLOW CHART

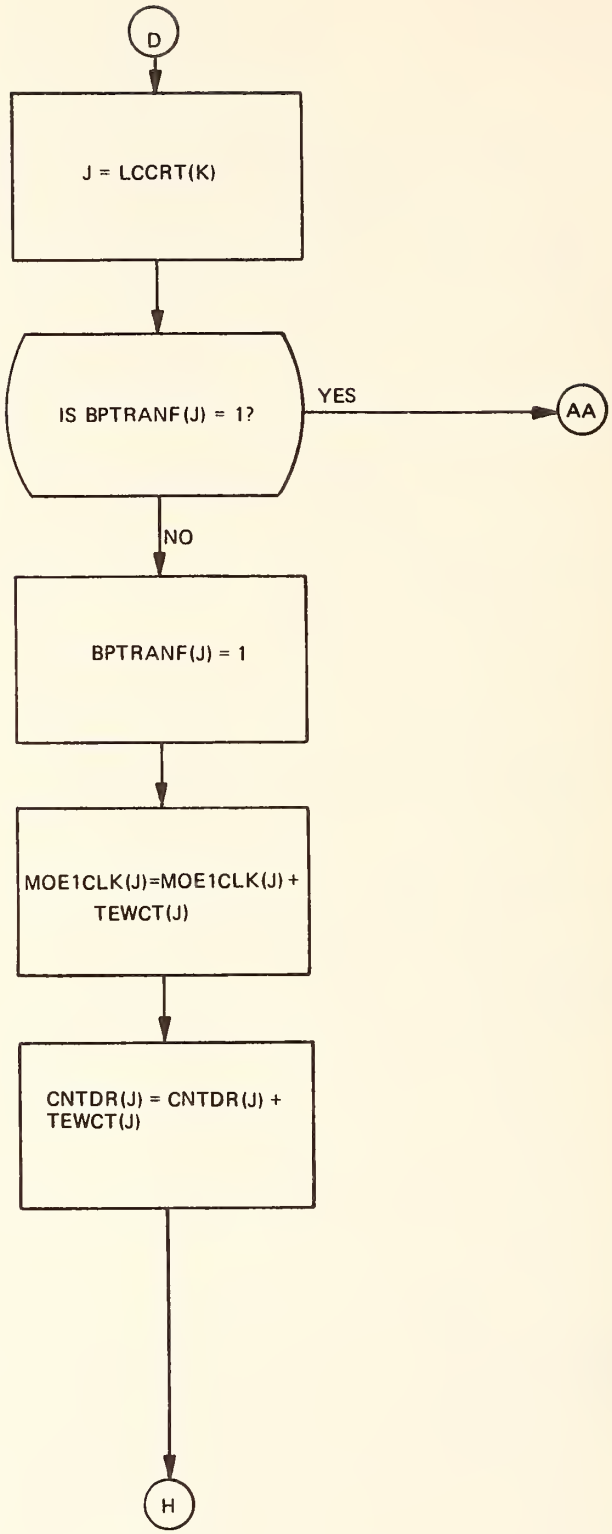


FIGURE 2.5.5.3. ROUTINE D FLOW CHART

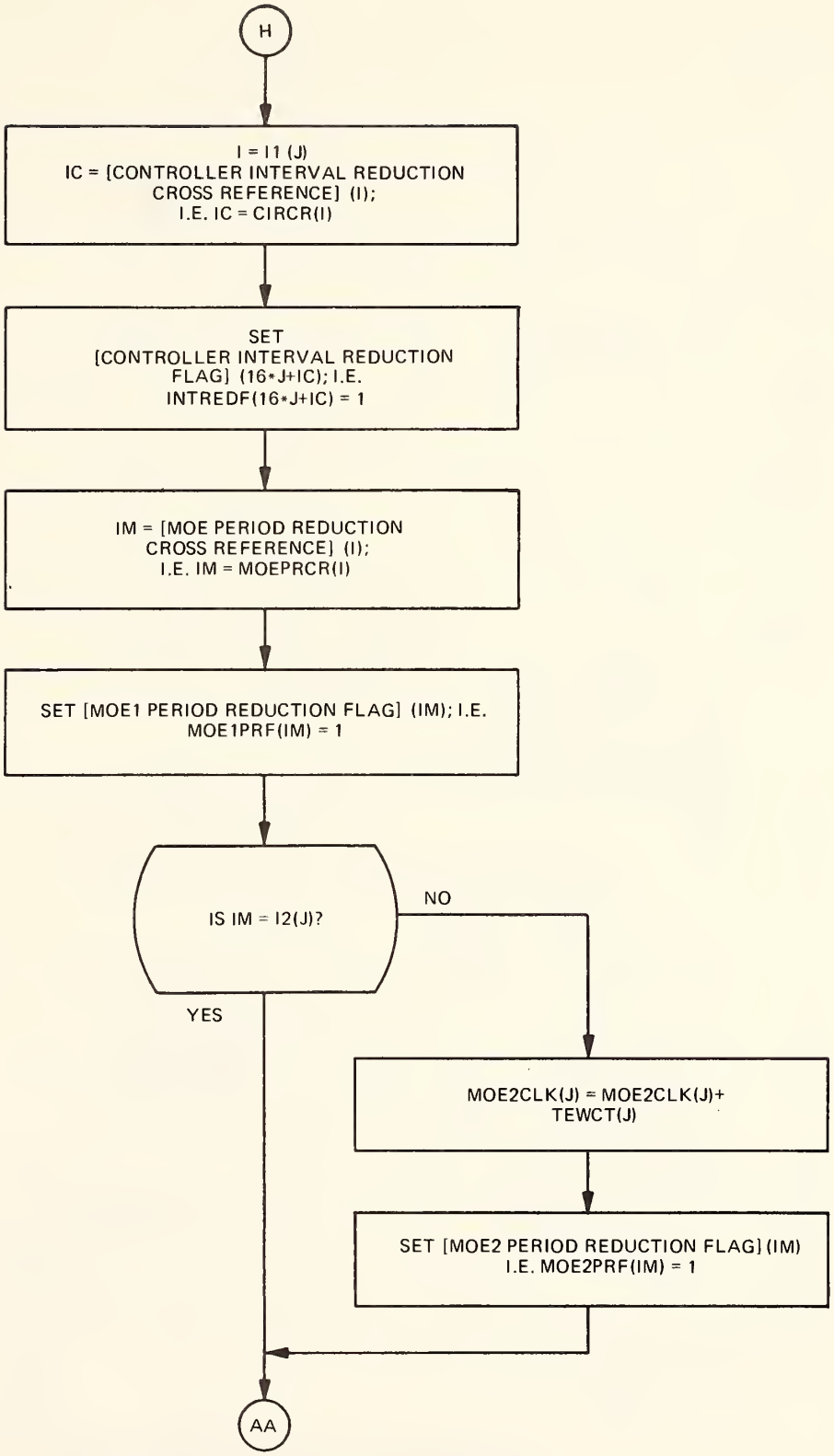


FIGURE 2.5.5.4. ROUTINE D FLOW CHART

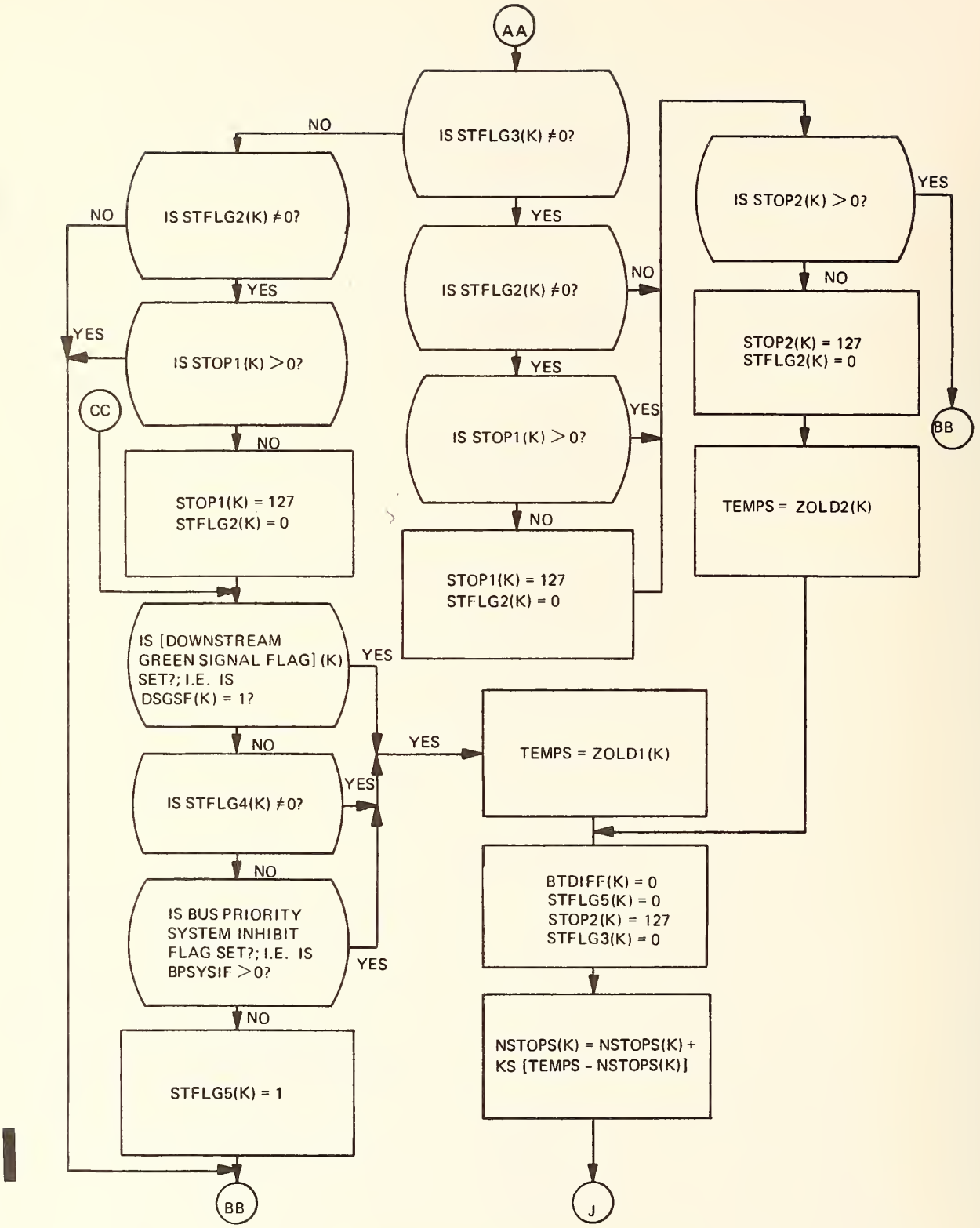


FIGURE 2.5.5.5. ROUTINE D FLOW CHART

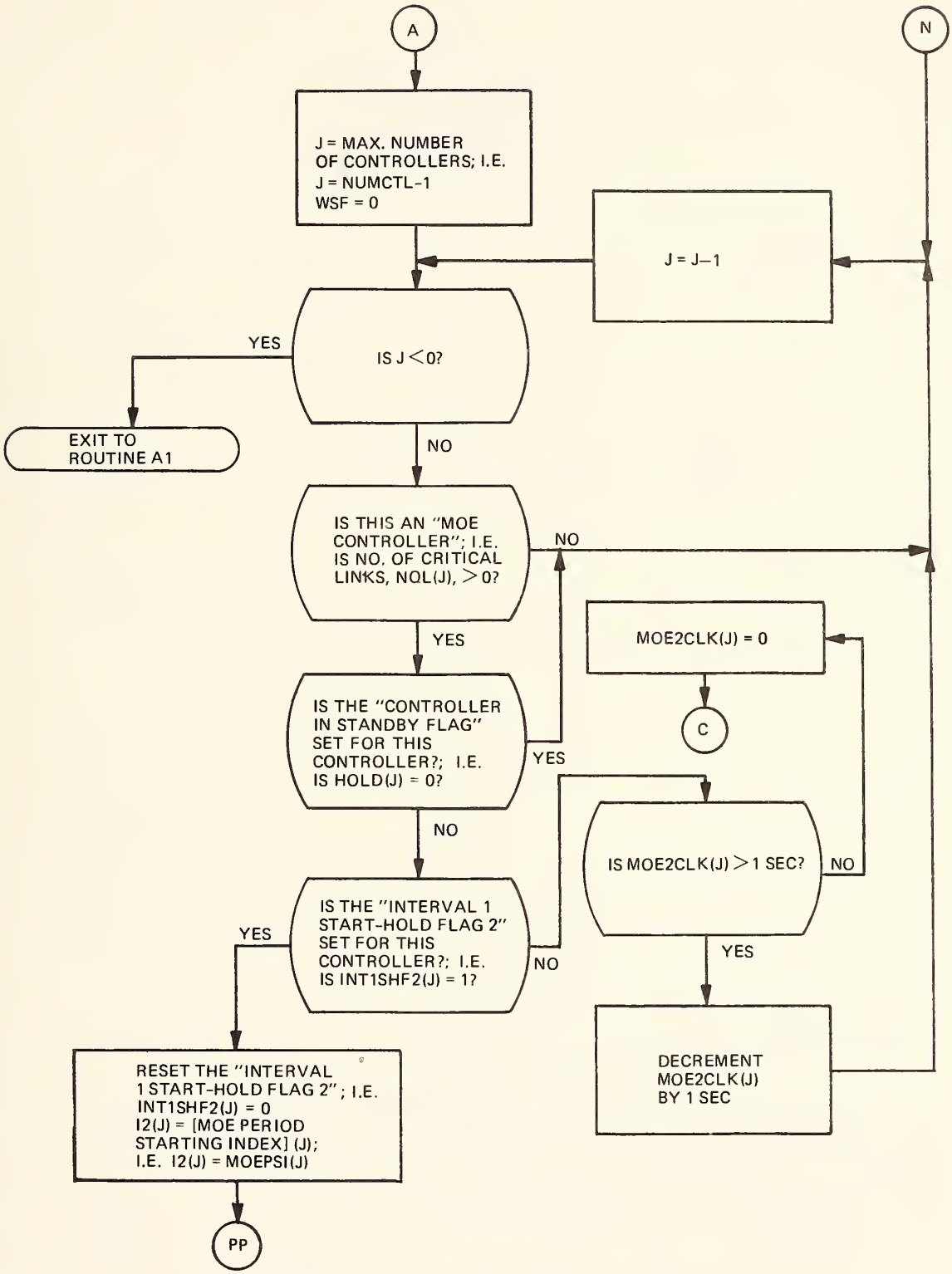


FIGURE 2.5.5.6. ROUTINE D FLOW CHART

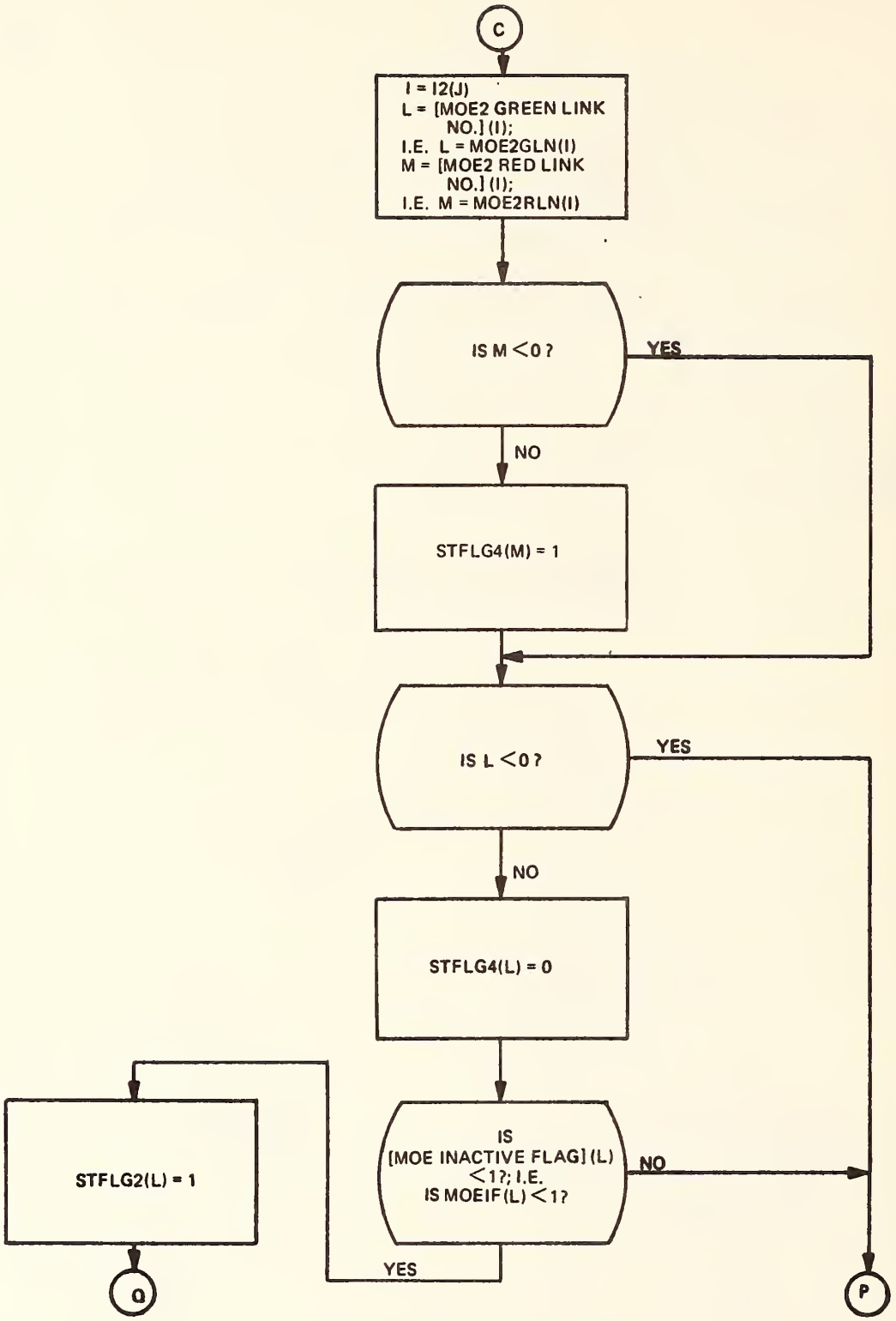


FIGURE 2.5.5.7. ROUTINE D FLOW CHART

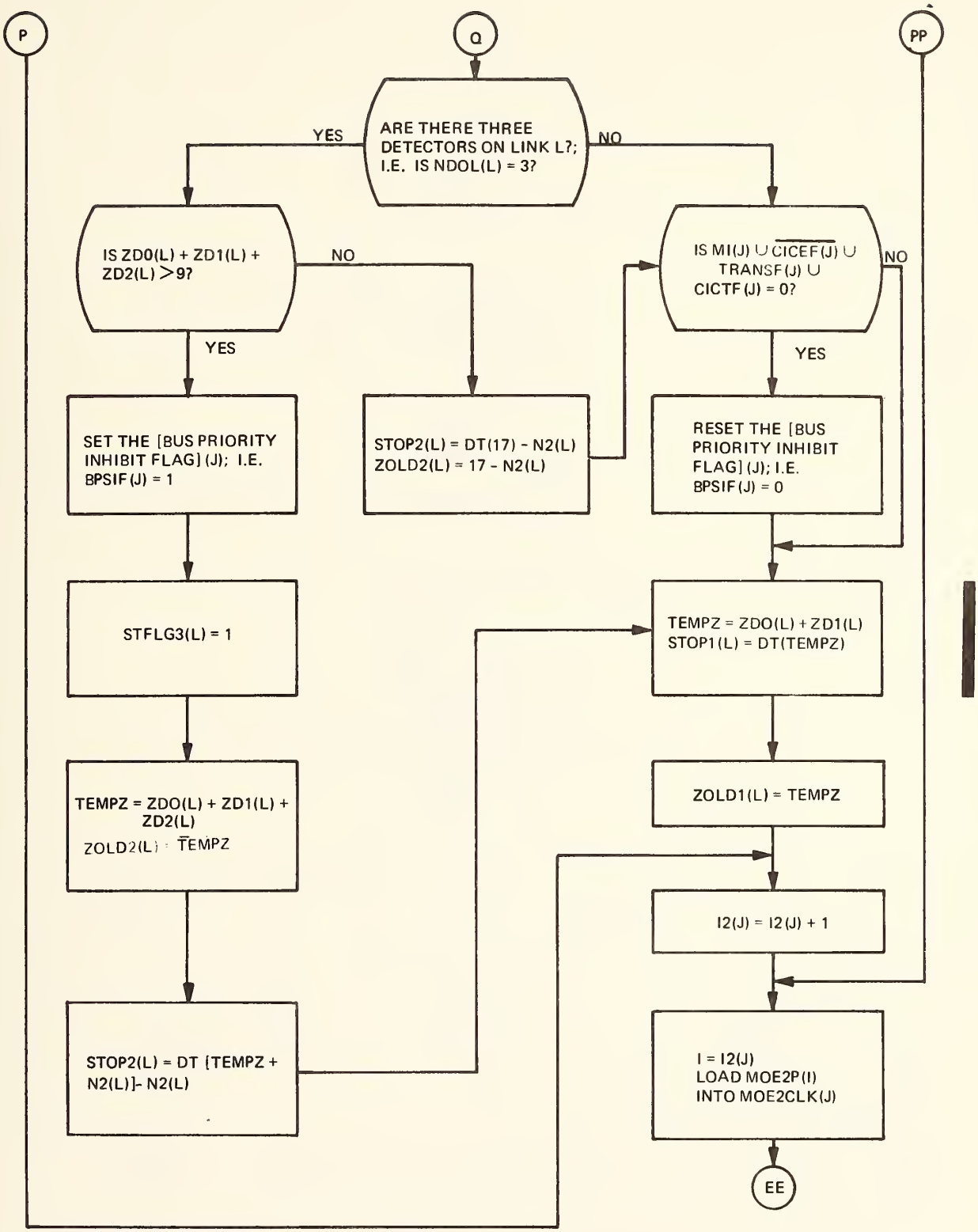


FIGURE 2.5.5.8. ROUTINE D FLOW CHART

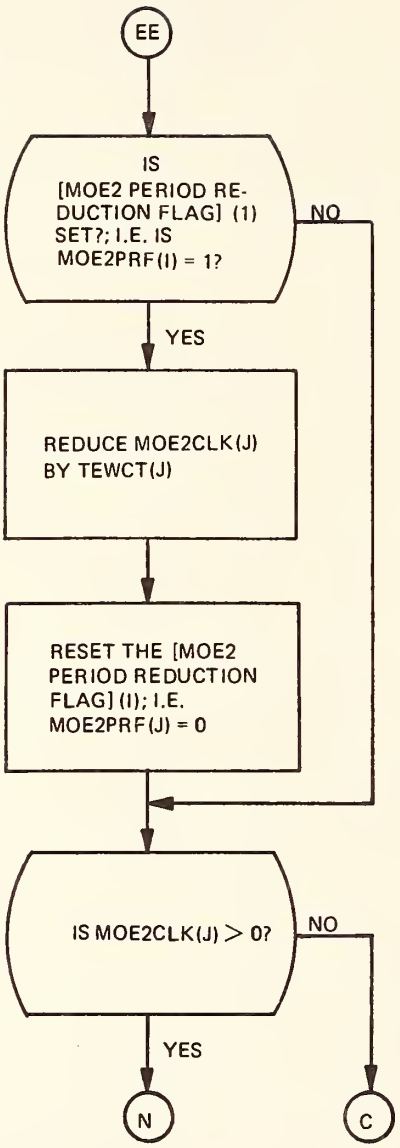


FIGURE 2.5.5.9. ROUTINE D FLOW CHART

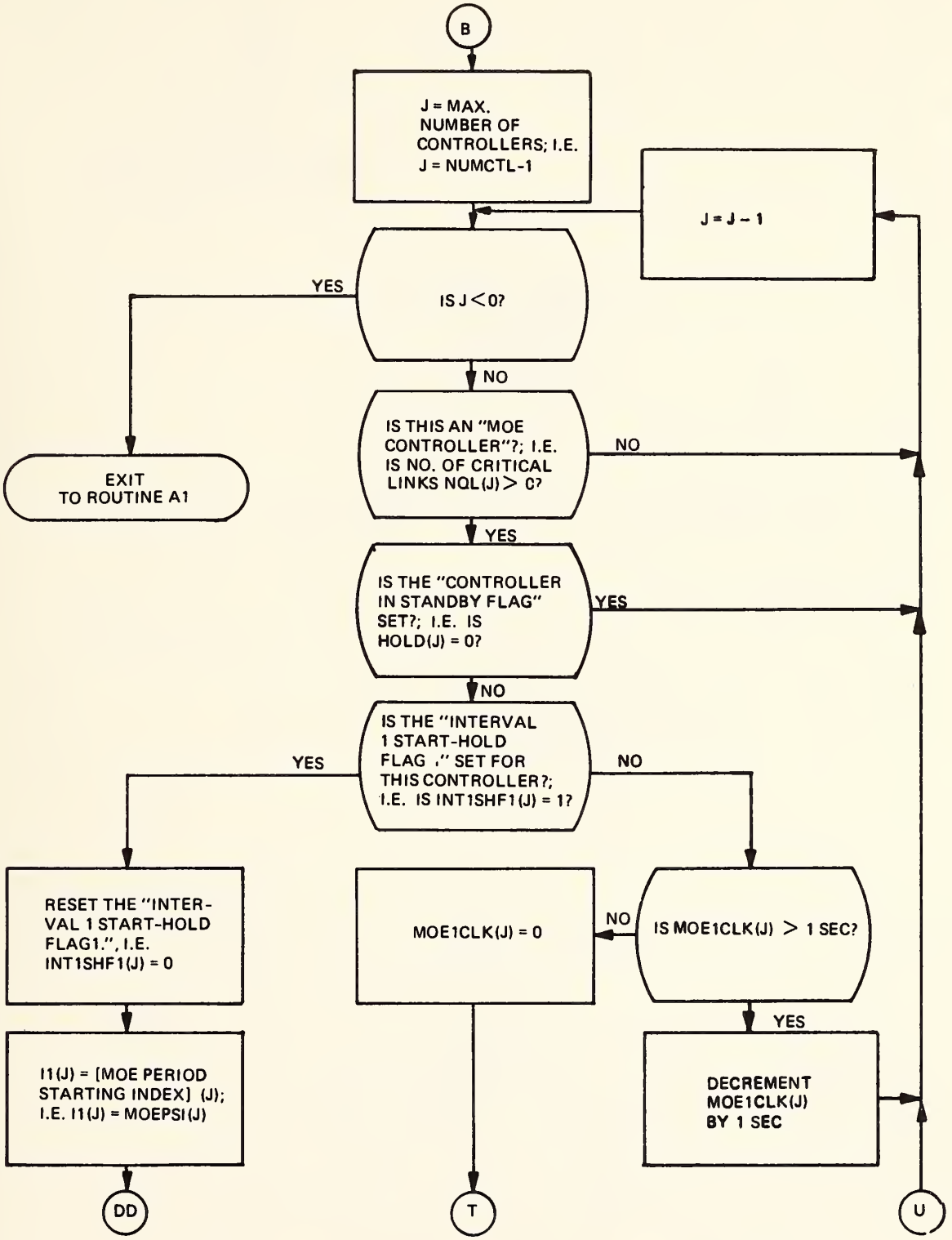


FIGURE 2.5.5.10. ROUTINE D FLOW CHART

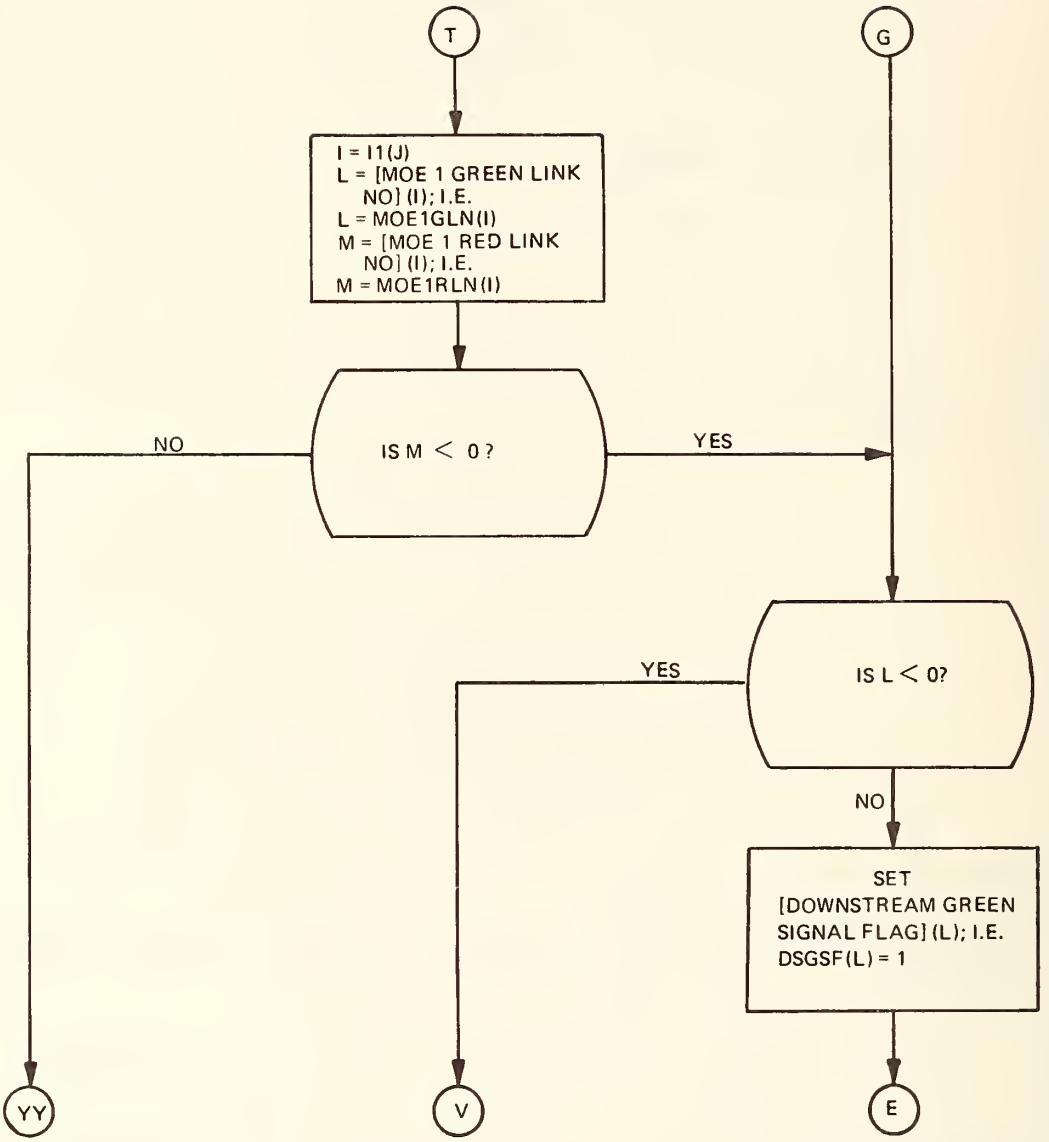


FIGURE 2.5.5.11. ROUTINE D FLOW CHART

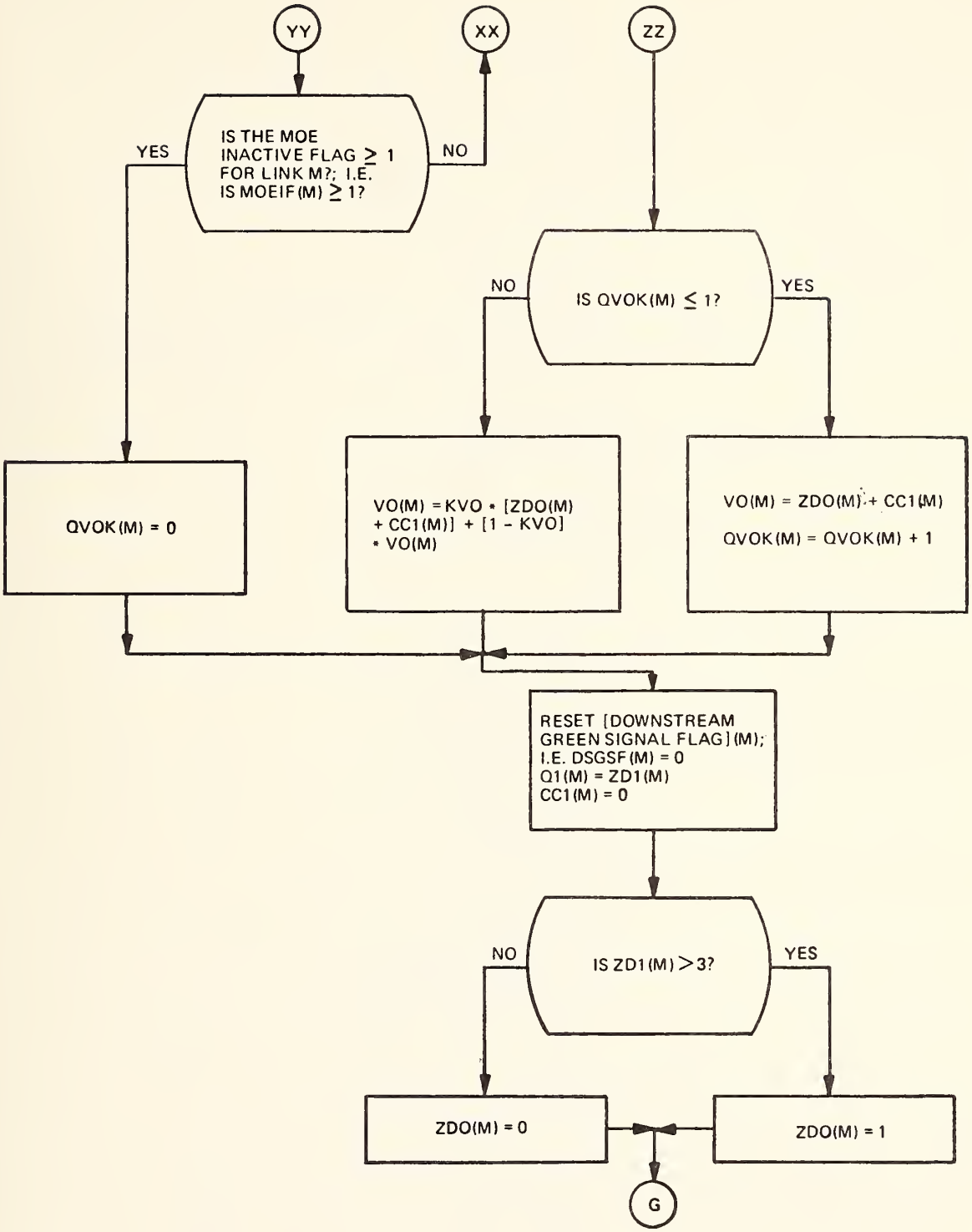


FIGURE 2.5.5.12. ROUTINE D SPECIFICATION

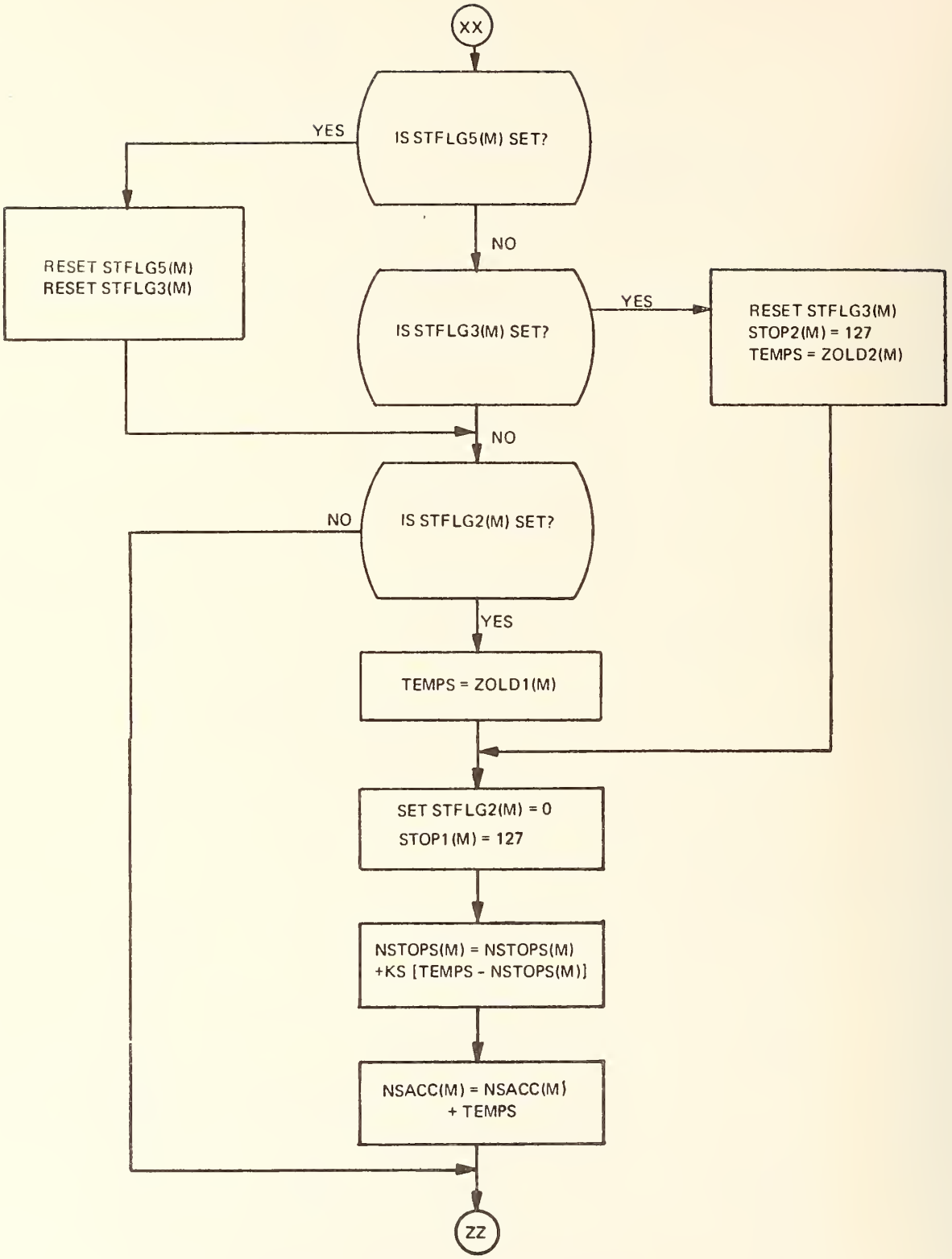


FIGURE 2.5.5.13. ROUTINE D SPECIFICATION

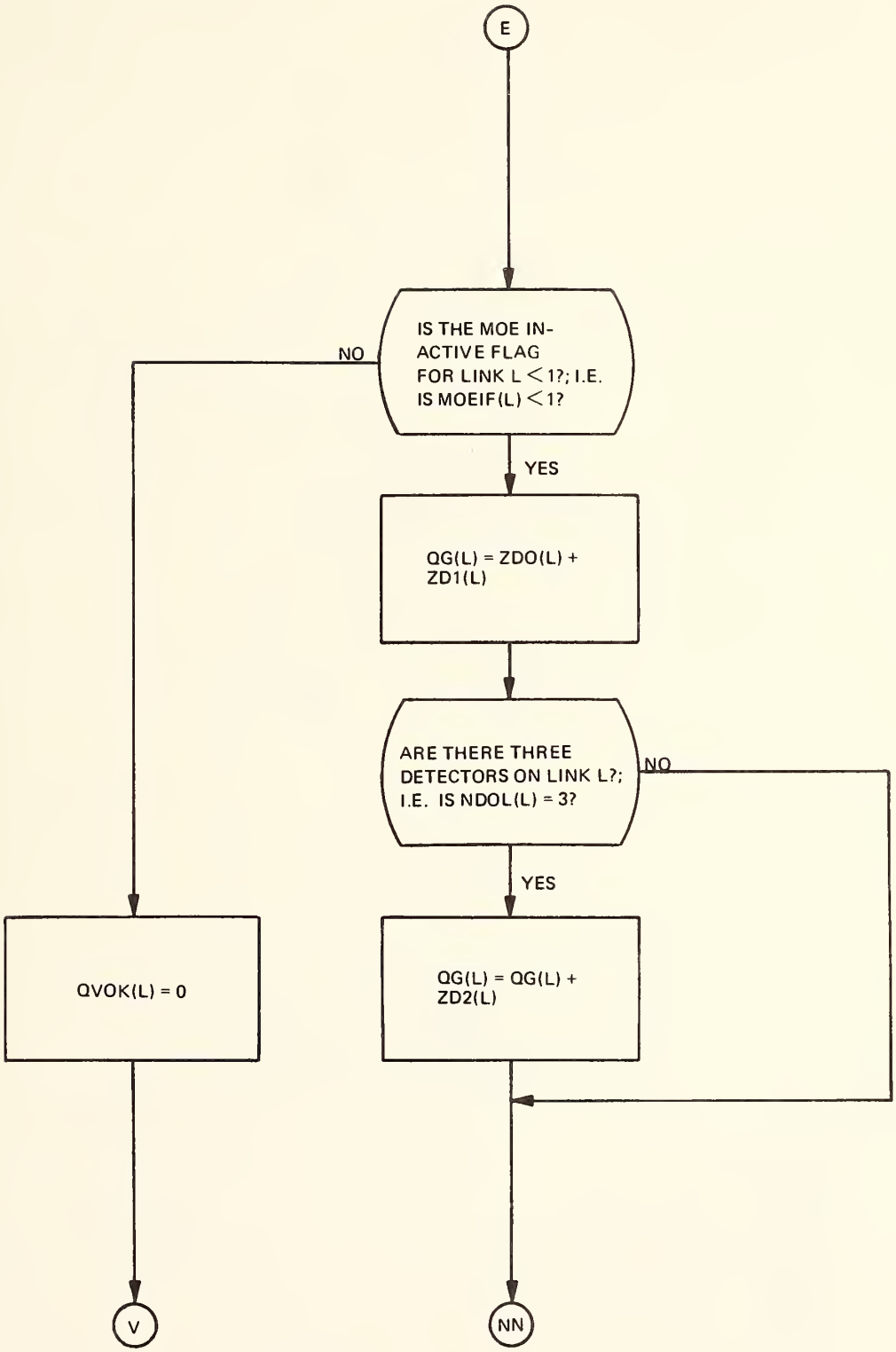


FIGURE 2.5.5.14. ROUTINE D FLOW CHART

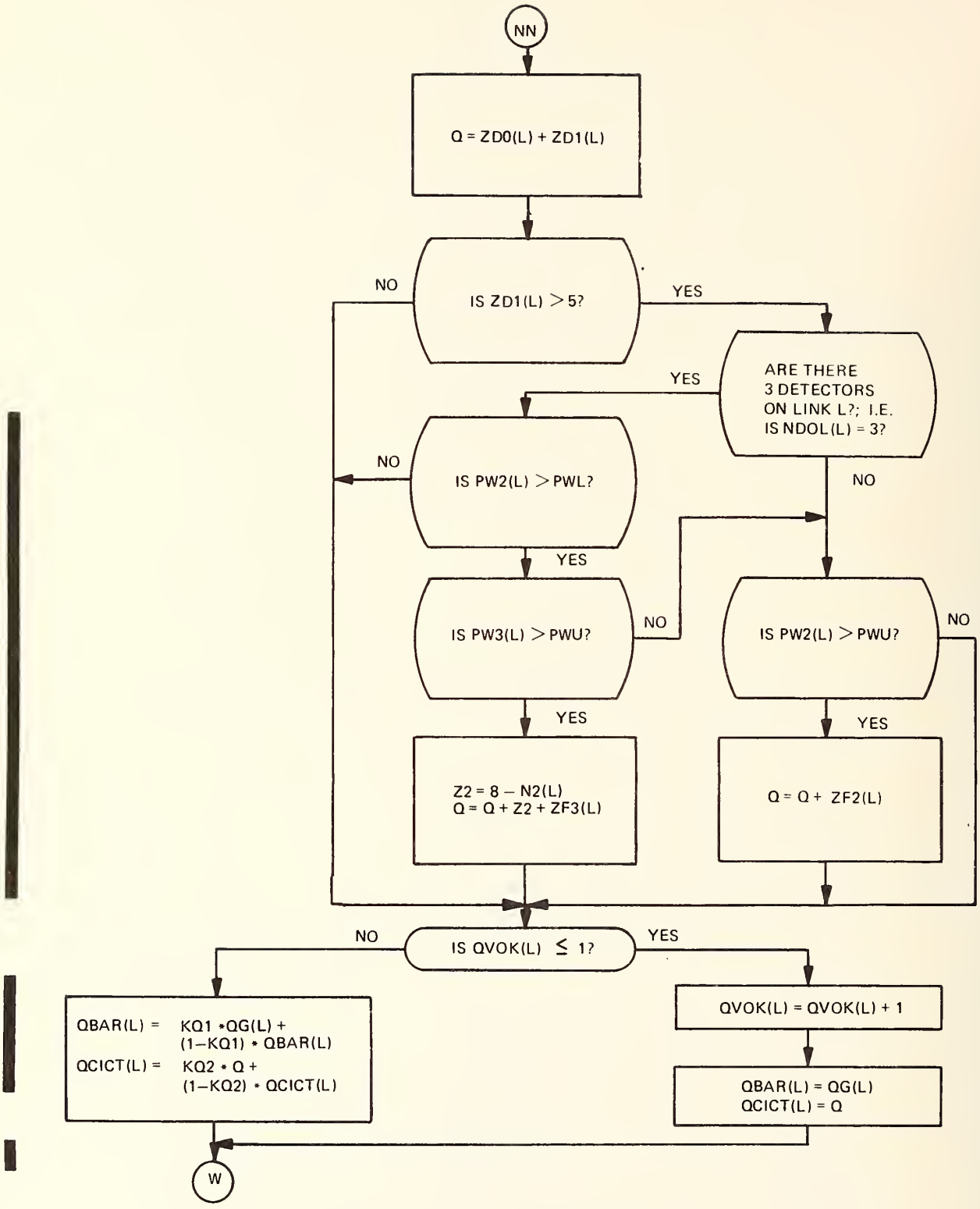


FIGURE 2.5.5.15. ROUTINE D FLOW CHART

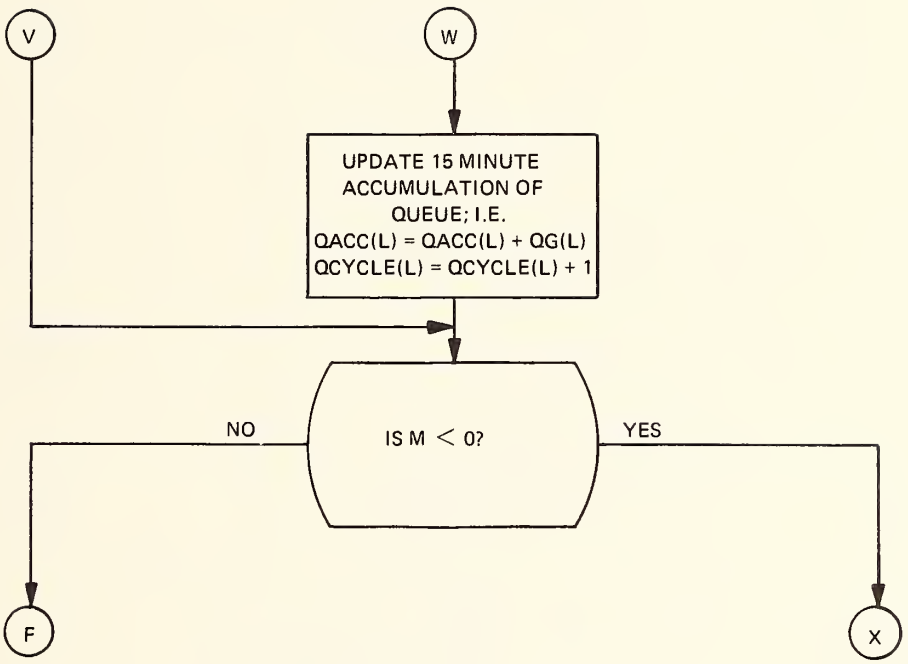


FIGURE 2.5.5.16. ROUTINE D FLOW CHART

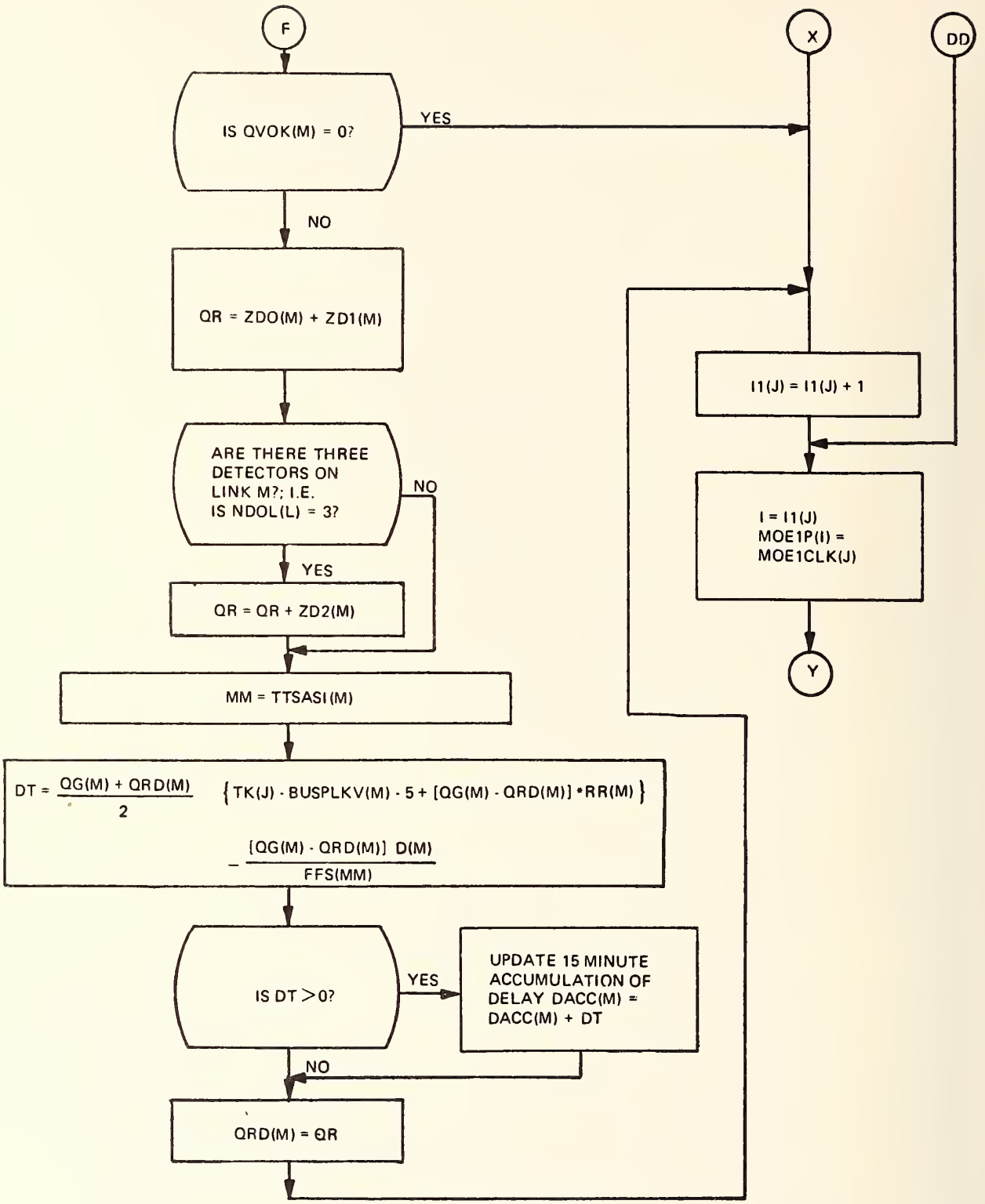


FIGURE 2.5.5.17. ROUTINE D SPECIFICATION

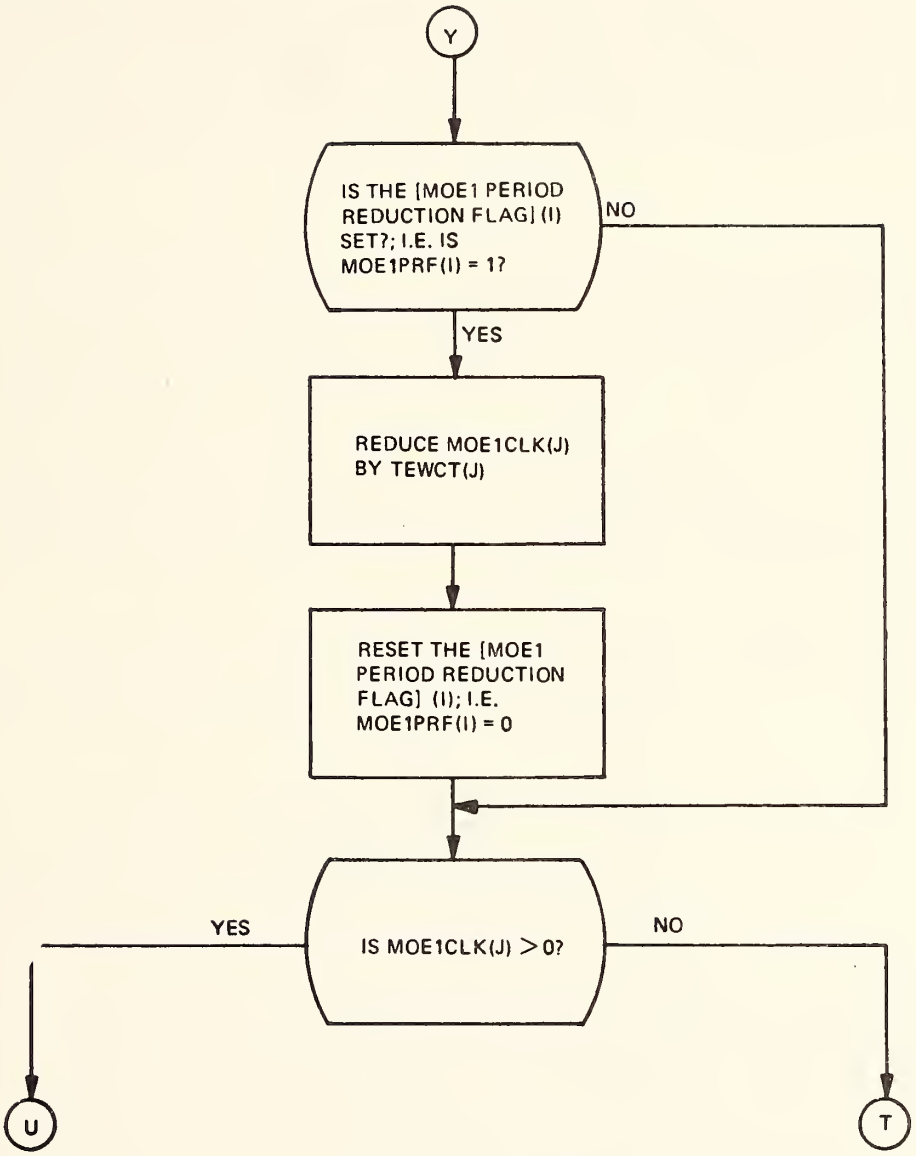


FIGURE 2.5.5.18. ROUTINE D SPECIFICATION

2.6 Routine E (Detector and Communications Failure Detection) Specification

2.6.1 Purpose

This routine identifies detector failures and informs the operator as to the location and type (detector electronics, detector obstruction or communications). It sets flags to prevent use of information emanating from these locations, and it updates raw link count, raw link occupancy and raw link speed.

2.6.2 Method

This routine first identifies, from the kth cycle start flag, which set of detectors (grouped by link for each controller) is to be checked. Detector numbers are indexed and if one belongs to the set under consideration, failure status for each detector is determined in the following manner.

If present pulse duration, TT, exceeds a specified interval, TT7, detector failure is indicated and the failed detector flag is set. If TT3 < TT < TT7, the "possible detector obstruction" flag is set, where TT3 is related to the maximum cycle length encountered in the system.

If a present gap duration, Tp, exceeds some multiple, M, of normal gap length, Tn, and is also greater than a specified interval, 180 secs, i.e.

$$\begin{aligned} & Tp > MTn \\ \text{and} \quad & TP > 180 \text{ secs} \end{aligned} \qquad (1)$$

and if the "possible detector obstruction" flag has been set, detector obstruction is identified. The "detector obstruction" flag is then set.

If the "possible detector obstruction" flag is not set and inequalities (1) hold, the operator is notified that communication failure and the "communication failure" flag is set. The detector is also reported as failed if the count is greater than a threshold, NCT.

If no failure is identified, the detector raw car count is added to the corresponding link count and the detector raw occupancy count is added to the corresponding raw link occupancy count. If any failure on a link is detected, an MOE Inactive Flag and a Failed Detector Flag are set. If the corresponding controller is in Standby, the MOE Inactive Flag is also set.

2.6.3 Repetition Rate

This routine is entered once per cycle for each group of controllers having the same cycle length.

2.6.4 Cross Reference

This routine is called by the Executive Routine in Level 3 and exits to that routine. It calls the CRT Failure Table Update Subroutine of Routine F and also calls Routine F.

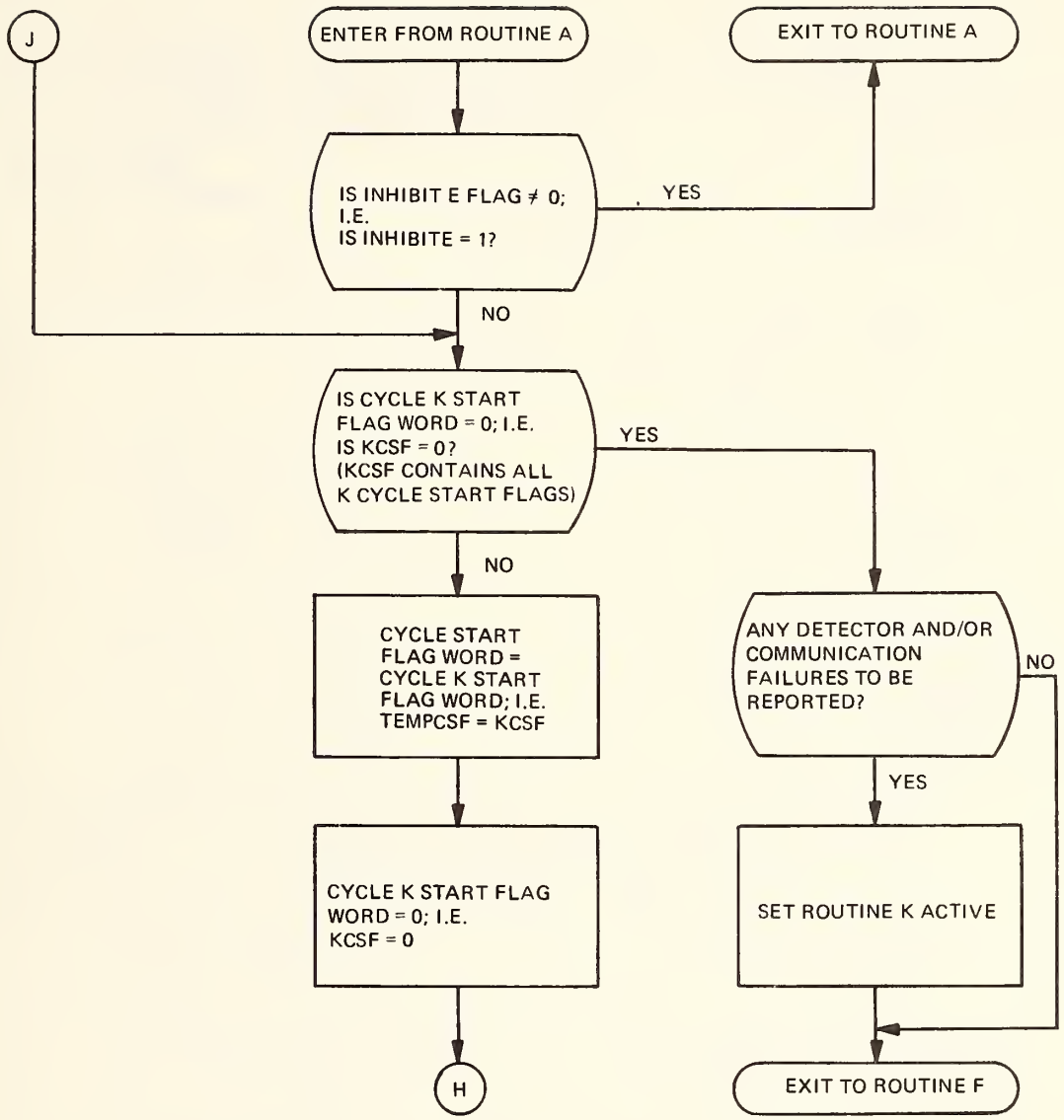


FIGURE 2.6.5.1. ROUTINE E FLOW CHART

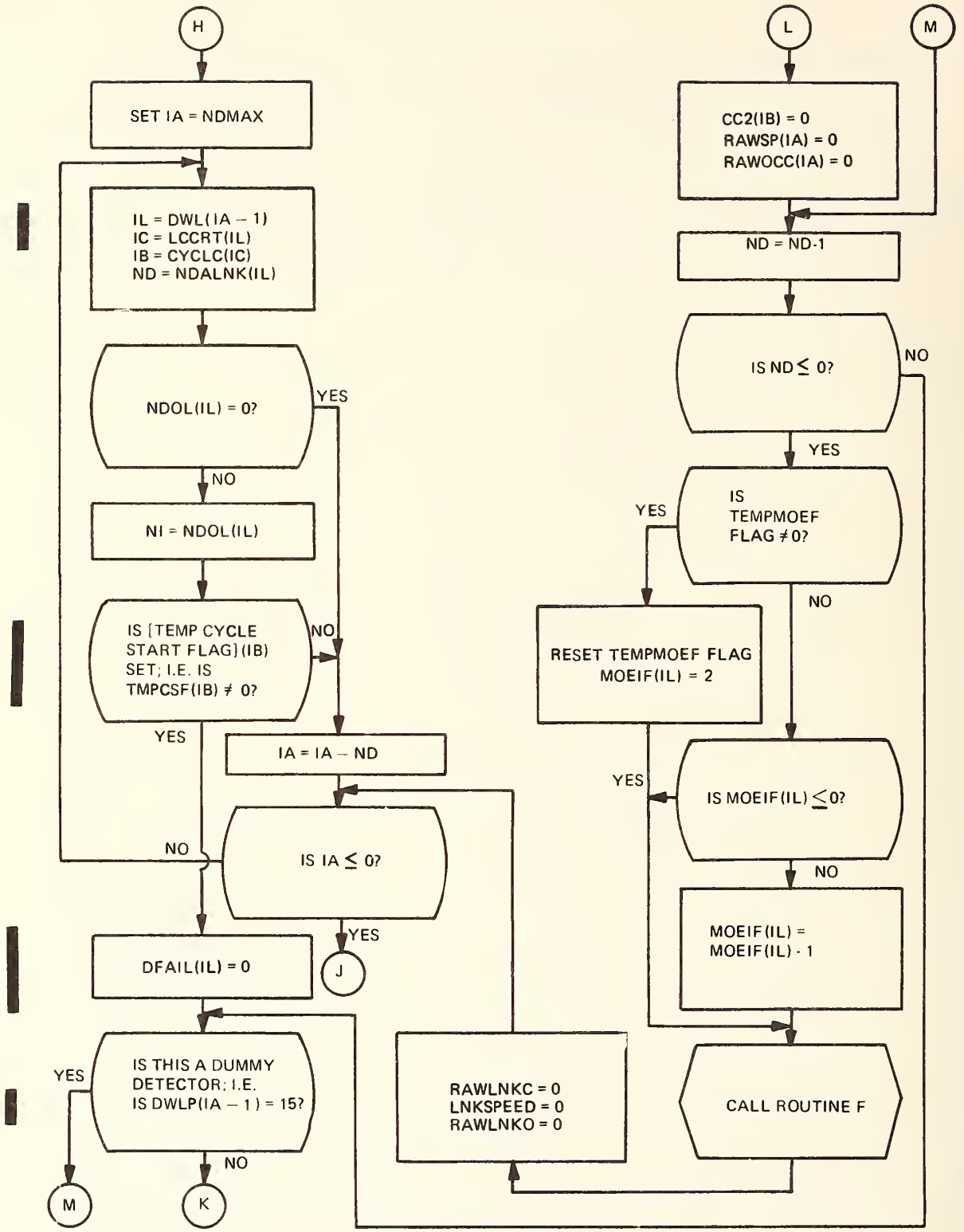


FIGURE 2.6.5.2. ROUTINE E FLOW CHART

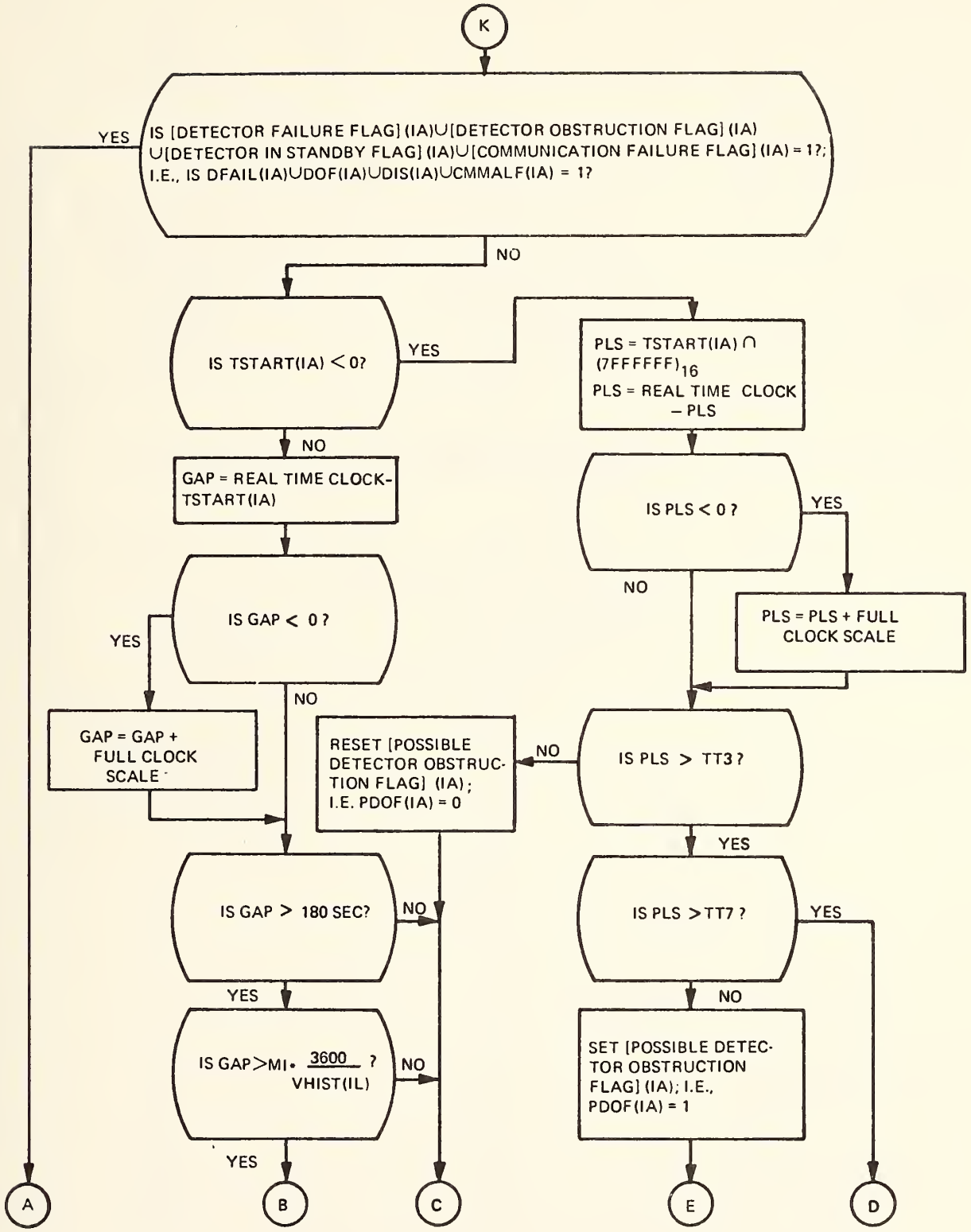


FIGURE 2.6.5.3. ROUTINE E SPECIFICATION

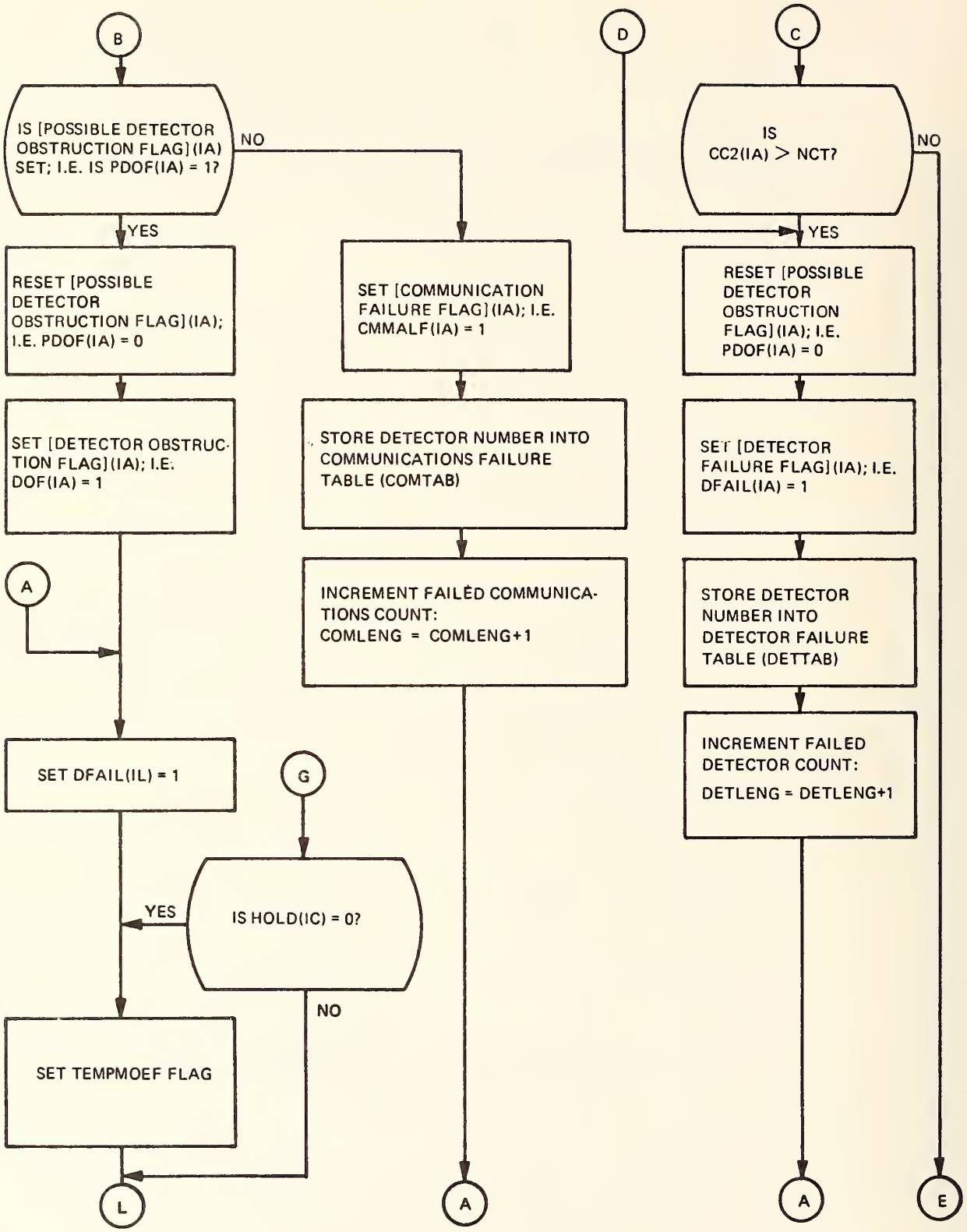


FIGURE 2.6.5.4. ROUTINE E SPECIFICATION

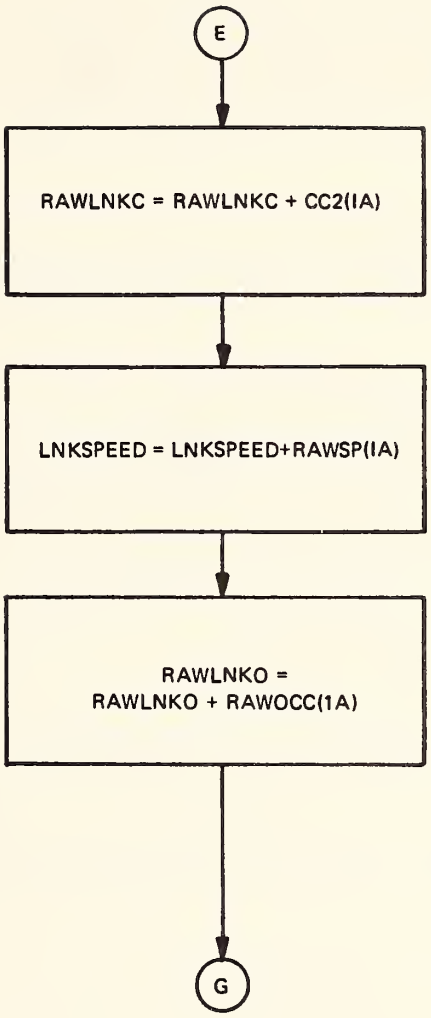


FIGURE 2.6.5.5. ROUTINE E SPECIFICATION

2.7 Routine F (Link Volume, Occupancy and Speed Evaluation) Specification

2.7.1 Purpose

Routine F accumulates link car count, link occupancy and link speed. It also computes volume, occupancy and average speed, by link, and smoothes these values with past data. If a link is inactive due to failures, stored typical volume and occupancy values are used for display.

2.7.2 Method

For the link being processed, the routine first determines the number of detectors on the link and the cycle length of its controller. If the link is active, the following computations are made:

- Raw link count, raw link occupancy and link speed are accumulated.
- Volume in vehicles/hour, occupancy in percent and average speed in miles/hour are computed and smoothed.

If the link is not active (failed), stored history values of volume and occupancy are accumulated.

2.7.3 Repetition Rate

This routine is entered once per cycle for each link.

2.7.4 Cross Reference

This routine is called by Routine E and returns to that routine.

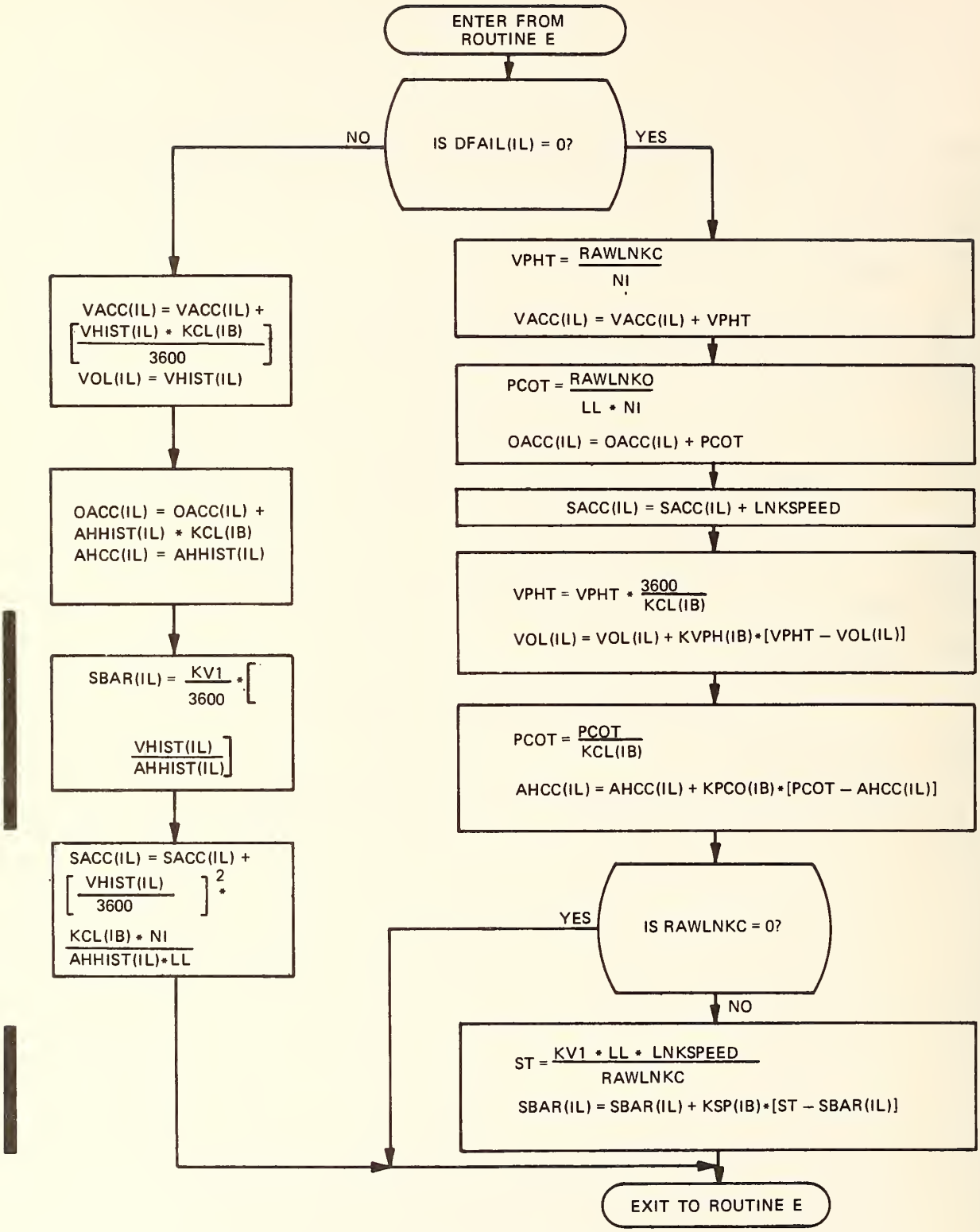


FIGURE 2.7.5.1. ROUTINE F FLOW CHART

2.8 Routine G (Controller-Link Cross Reference and Timing) Specification

2.8.1 Purpose

The purpose of Routine G is to compute the duration of intervals between successive action times, or MOE periods, for links that are both directed toward the controller being processed and are also instrumented for queue determination. It also formats the data so that these intervals can be easily associated with the applicable link(s) at the appropriate times.

2.8.2 Method

This routine computes the MOE periods as a function of the controller interval durations. For non-CIC intersections, these periods are fixed except for the first transition cycle and the first steady state cycle. As a result, this routine is required two times per transition of control parameters. The MOE periods for CIC intersections are further adjusted once per cycle by the CIC Routine, Routine V. Routine U may change these periods for any MOE controller, if an offset adjustment is required. The stored red and green link numbers correspond to the action time at the end of the MOE period. These MOE periods and the link cross reference are used by the "Computation of Stops Routine", Routine D. Appendix 4.7.8 describes the algorithm used for MOE period calculation.

Upon entry, the routine sets L to the number of adjustable MOE periods for this controller. For a non - MOE controller, L is zero and the routine is exited. For non-zero L, the basic purpose of the routine is to adjust the duration of the elements comprising two MOE period arrays. MOE1P is the basic MOE period array with the time durations referenced to the start of A-Phase Green. MOE2P is the predicted MOE period array with the time durations referenced to the start of A-Phase Green less the predicted green time of 9 seconds. This is accomplished by subtracting 9 seconds from the first MOE period in the MOE1P array. If this period is less than 9 seconds, the first MOE period in MOE2P is set to zero and the balance of the predicted green time is subtracted from the second MOE period. An example of this operation is shown in Table 2.8.2.1.

TABLE 2.8.2.1, MOE2P COMPUTATIONAL EXAMPLE

MOE Period Number	MOE1P Duration	MOE2P Duration
1	7	0
2	8	6
3	2	2
4	6	6
5	3	3
6	27	27

The MOE1P duration for the Mth adjustable MOE period is computed by summing the interval durations from array, INTDUR, for each of the controller intervals in this MOE period. This is accomplished by first computing the largest controller interval number, JM, in the Mth adjustable MOE period. Then the interval durations are summed from the present controller interval number, J, through JM, to yield MOETMP which later is stored in the appropriate element of MOE1P.

It should be noted that the only inputs to this routine that cause changes in MOE1P and MOE2P are the elements of INTDUR. In addition, arrays AMOEPN, NCONTI, INTDUR, MOE1P and MOE2P are essentially doubly dimensioned arrays since they contain data for each controller. Arrays AMOEPN and NCONTI contain 6 elements per controller, array INTDUR contains 16 elements per controller and arrays MOE1P and MOE2P have different numbers of elements assigned to each controller. The relative starting index for each controller in the last two arrays is found from array MOEPSI.

2.8.3 Repetition Rate

This routine is entered only when called by Routines S, T, or V which can only occur at the start of a controller interval.

2.8.4 Cross Reference

This routine is called either by the Transition Routine, Routine S; by the Interval Advance Routine, Routine T; or by the Critical Controller Routine, Routine V; and returns to the routine from which it was called. The controller currently being processed must be designated by the calling routine.

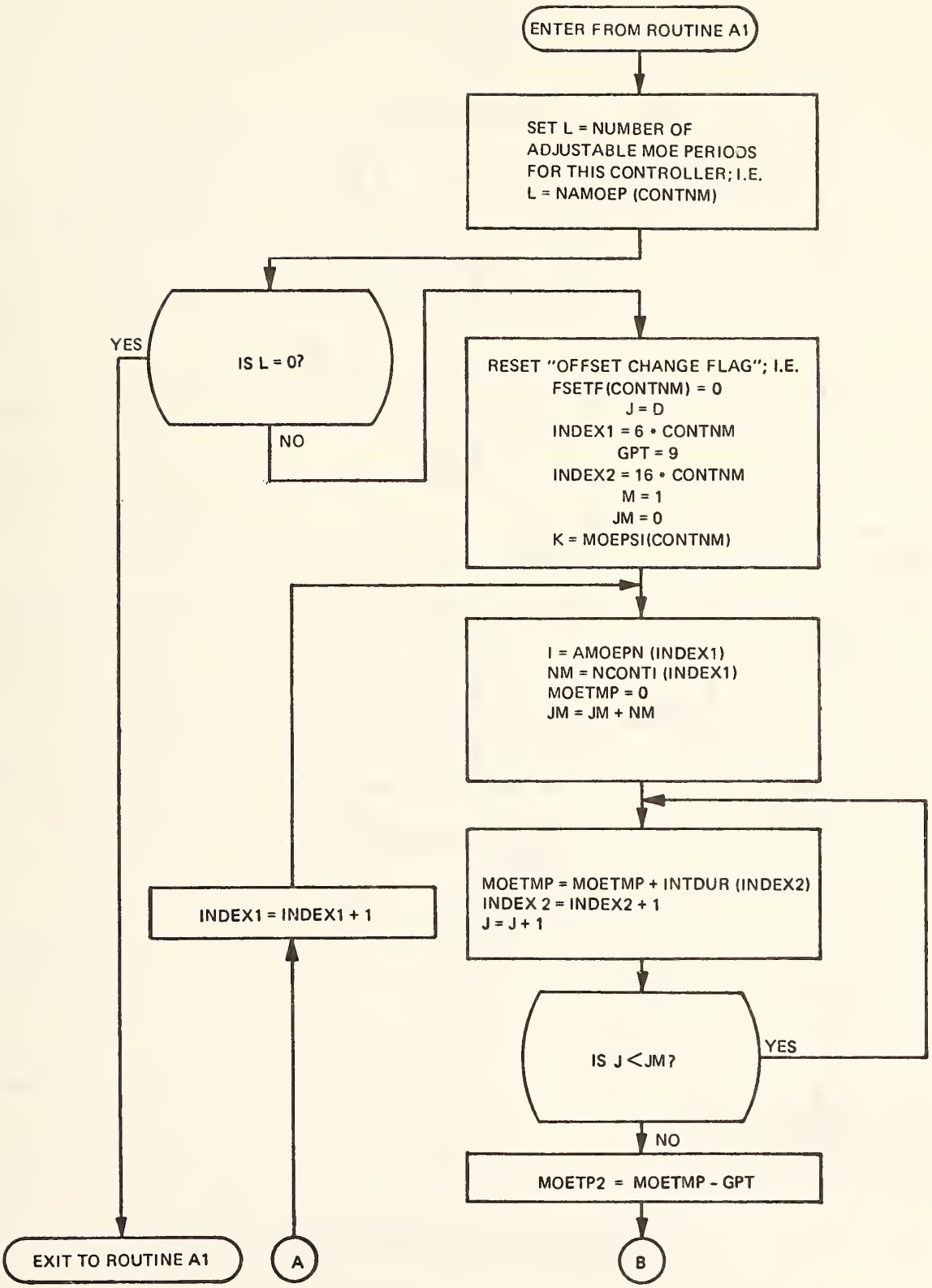


FIGURE 2.8.5.1. ROUTINE G SPECIFICATION

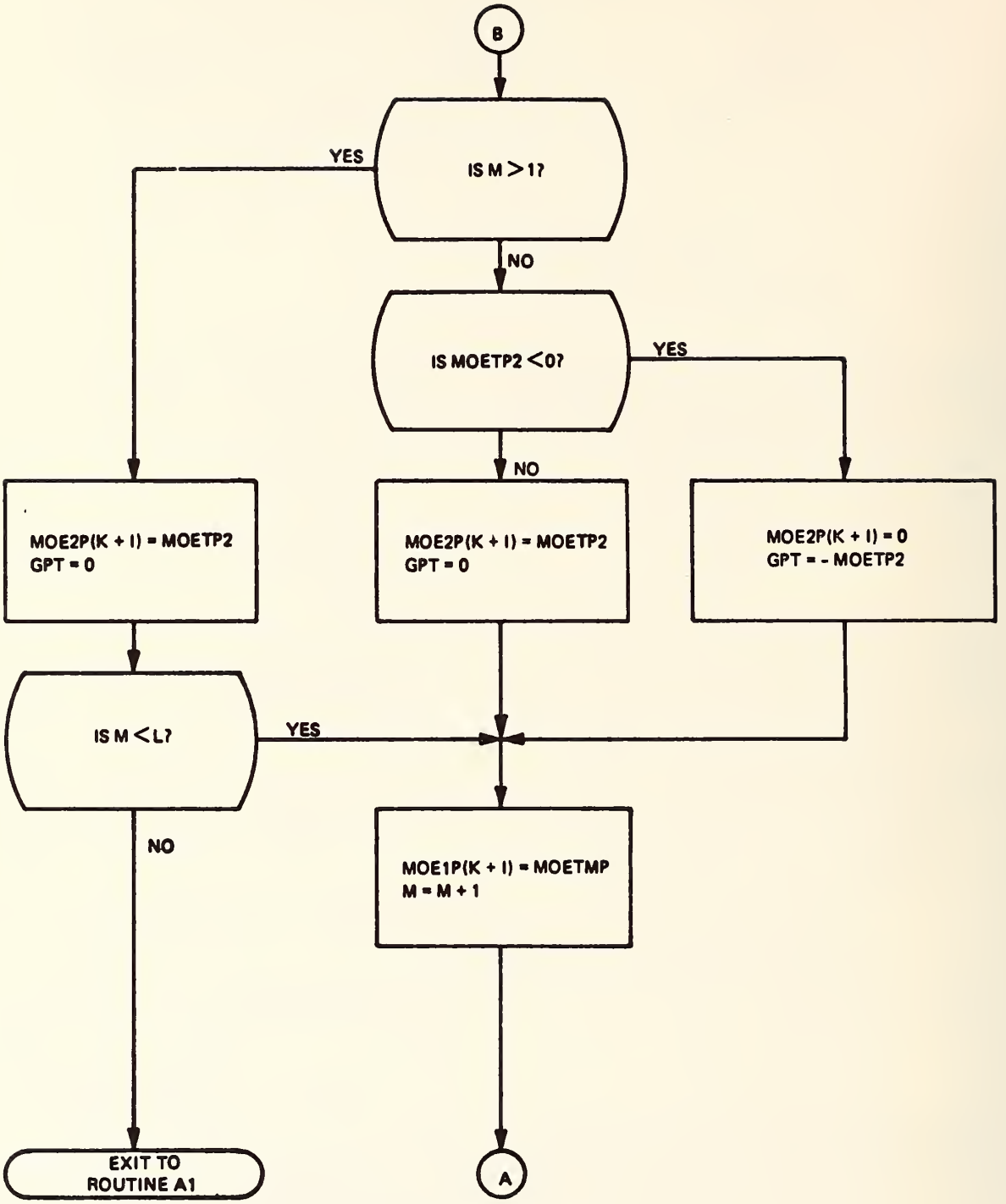


FIGURE 2.8.5.2. ROUTINE G SPECIFICATION

2.9 Routine H (15-Minute Performance and Status Report) Specification

2.9.1 Purpose

The purpose of Routine H is to provide a 15 minute performance and status report on the line printer for both the UTCS and BPS parts of the system. This report contains a log of all operator entered control panel system requests made during the last 15 minutes, the number of failures in the system, controller and detector status, system status by section, UTCS system performance by link, BPS section summary and BPS zone summary. In addition, on magnetic tape it records all the Measures of Effectiveness (MOEs) at 15-minute intervals.

If the Change Formatting Subroutine (HFMT), which logs operator control panel requests, finds the log table filled it sets Routine H active in order to force a print out of the log table.

2.9.2 Method

Upon entry Routine H calls Subroutine CTPSRT to print out the system requests log. CTPSRT will check to see if this is a forced printout (log table filled) and if it is will set a flag so that Routine H will exit after the page is printed. If it is not a forced printout, CTPSRT will check to see if the PRINTOUT SUPPRESS button is engaged on the control panel. If it is engaged CTPSRT will return to Routine H and begin processing link data. If the printout is not to be suppressed, CTPSRT will check to see if there is anything in the table. If the table is empty, CTPSRT returns to Routine H and begins processing the Failure Status page. If there is something to be printed out, CTPSRT sets a flag so that Routine H will begin processing the Failure Status page after the log has been printed.

Routine H begins processing the Failure Status page by checking to see if there are any failures in the failure table (FAILTAB). If there are none, Routine H begins processing the Controller Status page. If there are failures, the equipment type and number, the time and day of the failure, and whether the operator has taken action in response to the failure is printed out. A flag is set so that Routine H will begin processing the Controller Status page after the Failure Status page has been outputted.

Routine H checks the status of all the controllers in the system. It creates a list, in increasing numerical order, of the controllers that are under critical intersection control, have been selected for critical intersection control but not operating as such (inhibited CIC), are in standby, and those that have failed. It prints out this list, if it is not empty, as the Controller Status page and then proceeds to process the Detector Status page.

The Detector Status page is processed in a way similar to the Controller Status page. A list is created, in increasingly numerical order, of those detectors that are in standby, have communication failures, and those that have failed. It prints out this list, if it is not empty, as the Detector Status page and then proceeds to process the System Status page.

For each section, the actual mode (TOD, STBY, etc.) and the time it was imposed, the desired mode, the pattern number, number of CIC intersections in operation, number of BPS intersections in operation, number of failed detectors, and number of failed controllers is determined and printed out as the UTCS System Status page.

Routine H processes link data every 15-minutes regardless of the state of the SUPPRESS PRINTOUT button on the control panel. For each link, percent occupancy (OPC), average speed (AVSP) and travel time (TRTM) are calculated. Accumulated daily volume (VDAY), accumulated daily occupancy (ODAY), and accumulated average speed in the day (SDAY) are updated. For each link with more than one detector, queues (QPT), delays (DELAY), and stops (STPTEMP) are also calculated. Accumulated daily queues (QDAY), accumulated daily delays (DELDAY), and accumulated daily stops (NSDAY) are updated. The arrays used for the 15-minute accumulations of queues (QACC), delays (DACC), stops (NSACC), volume (VACC), speed (SACC) and occupancy (OACC) are set to zero. The MOEs are collected for each link and placed into the tape buffer (15TBUFF). The tape format is shown in Figure 2.9.2.6. Any link that had out of tolerance performance during the interval since the last 15-minute report is flagged by setting the sign bit of the link number half-word that is put onto tape. Out of tolerance links are determined by performing two checks: the absolute values of the difference between current accumulated volume plus weighted occupancy and stored (history) volume plus weighted occupancy is computed. If this difference and the percent difference exceed preselected threshold values, the link is considered out of tolerance. Following the transfer of the MOE data record, a second record is output containing the operator action table (CHGTABLE), the Controller Malfunction Array (CMALF), the Detector Malfunction Array (DMALF), and the Communications Malfunction Array (CMMALF). The format of this record is shown in Figure 2.9.2.6.

After all the links are processed, Routine W is scheduled and a check is made of the PRINTOUT SUPPRESS button on the control panel. If the button is engaged, the program branches and begins processing for BPS Zone Summary. If the printout is not suppressed, Routine H prints out the UTCS System Performance Report. For each link that is out of tolerance the following information is printed out:

- link number
- history volume

- history percent occupancy
- current cumulative volume
- current cumulative percent occupancy
- average queue per cycle
- current cumulative number of stops
- average speed
- average travel time
- delay

In addition, if the controller associated with the link is not on-line an "*" is printed next to the link number. If there is a failed detector on the link, a "H" is printed next to the link number and all MOE's except volume and occupancy are set to zero on both the printout and the tape. Queue, stops and delay are only printed out for multidetector links.

Routine H calculates the number of BPS intersections, the number of pre-empt intersections, the number of inhibited intersections, and the number of failed BPS detectors in each section. This information is printed out as the BPS System Status.

Routine H processes zone data every 15-minutes regardless of the state of the SUPPRESS PRINTOUT button on the control panel. The daily bus sums for each zone are incremented. These are: through bus count (TB), stop bus count (SB), eligible through bus count (ETB), eligible stop bus count (ESB), extensions granted (EG), helped through buses (HTB), helped stop buses (HSB), and passenger minutes saved (PMS). In addition, the number of buses helped (HTB15+HSB15) during the last 15 minutes and the passenger gain (IG15) during the last 15 minutes for each zone are placed into the MOE tape buffer.

The 15-minute mode of operation is calculated for each zone (REL, OFF, etc.) for use on the printout.

A check is made to see if the page is to be printed out. If it is not, the program does some clean up before exiting. If it is to be printed out, the following information is outputted for each zone; direction, 15-minute mode of operation, stop bus volume, through bus volume, eligible stop buses, eligible through buses, extensions granted, helped stop buses, helped through buses and passenger minutes saved. Also the following values are calculated and printed out: section and system totals for bus volume (stop and thru), eligible buses (stop and thru), the number of extensions granted, helped buses (stop and thru) and passenger minutes saved.

During clean up Routine H increments the number of 15-minute reports (NREPORT) and clears the 15-minute accumulation arrays for through buses (TBV15), stop buses (SBV15), eligible through buses (ETB15), eligible stop buses (ESB15), helped through buses (HTB15), helped stop buses (HSB15), extensions granted (EG15) and passenger gain (IG15). A check is made to see if the MOE tape is to be written (SENSE SWITCH 3 IS SET). If it is, the MOE tape buffer is outputted to a 7 track tape in packed binary format. If not, a check is made to see if it was written during the last 15-minute period. If it was, an EOF mark is placed on the tape.

Finally a check is made to see if it is midnight or if it is a shutdown. If it is either, Routine I is scheduled. Routine H then exits.

The Change Formatting Subroutine (HFMT) is contained within Routine H. It is called by Routine M to log control panel system requests. For each system request the following information is logged: Time of Change, Type (system, section, controller, detector, detector communications, BPS detector, BPS detector communications, BPS zone), Number, Change (standby, manual, time of day, traffic responsive, history record on, history record off, split, offset, CIC on, CIC off, failure acknowledge, failure repair, on line, BPS off, BPS on, BPS pre-empt off, BPS pre-empt on, manual extension). In addition, if a manual pattern change was requested, the manual pattern number is logged. If a manual extension was requested, the extension is logged. The change table (CHGTABLE) is designed to hold 44 requests. When this table is filled Routine H is set active in order to print out the table.

2.9.3 Repetition Rate

This routine is entered every 15 minutes on the 15 minute mark. It is also entered when shutdown is requested.

The Change Formatting Subroutine (HFMT) is scheduled asynchronously from Routine M.

2.9.4 Cross Reference

This routine is scheduled at Level 3. The Change Formatting Subroutine is scheduled, as required, by Routine M.

UTCS/BPS 15 MINUTE STATUS AND PERFORMANCE REPORT

DATE MAR 18 74 TIME 0730

CHANGES SINCE LAST REPORT

TIME	TYPE	NUMBER	CHANGE
0717	SYS	0	BPON
0719	BCAM	66	REPR
0719	BCAM	65	REPR
0720	BDFT	94	REPR
0721	CONT	68	BPON
0727	BDFT	94	REPR
0727	DET	201	FACK
0727	DET	202	FACK
0727	DET	207	FACK

FIGURE 2.9.2.1. UTCS/BPS 15 MINUTE STATUS AND PERFORMANCE REPORT

*** UTCS/BPS FAILURE STATUS ***

TYPE	NUMBER	TIME	MONTH	DAY	ACK
BDET	94	0728	MAR	18	N
DET	201	0724	MAR	18	Y
DET	202	0724	MAR	18	Y
DET	207	0724	MAR	18	Y

FIGURE 2.9.2.2. UTCS/BPS 15 MINUTE STATUS AND PERFORMANCE REPORT

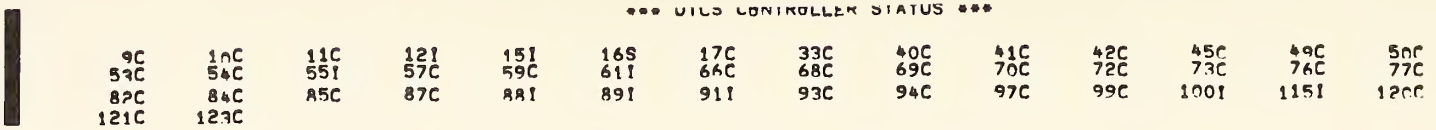


FIGURE 2.9.2.2. UTCS/BPS 15 MINUTE STATUS AND PERFORMANCE REPORT (CONTINUED)

FIGURE 2.9.2.2. UTCS/BPS 15 MINUTE STATUS AND PERFORMANCE REPORT (CONTINUED)

*** UTCS SYSTEM STATUS ***

HISTORY OFF

SECTION	TIME	DESIRED MODE	ACTUAL MODE	PATTERN NO.	CIC IN OPER	BPS IN OPER	FAILURES DET	FAILURES CONT
1	0717	MAN	MAN	2	1	1	0	0
2	0717	MAN	MAN	2	6	3	0	0
3	0717	MAN	MAN	2	18	13	4	0
4	0717	MAN	MAN	2	9	4	0	0

FIGURE 2.9.2.2. UTCS/BPS 15 MINUTE STATUS AND PERFORMANCE REPORT (CONTINUED)

UTCS SYSTEM PERFORMANCE REPORT

CURRENT CUMULATIVE MOE

OUT OF TOLERANCE LINK NUMBER	HISTORY VOL (VEH)	HISTORY OCC (PCT)	VOL (VPH)	OCC (PCT)	QUEUE (VEH/CYCLE)	STOPS (NO.)	AV.SP. (MPH)	TRAV.TIME (SEC/VEH)	DELAY (SEC/VEH)
1	0	0	316	5			24	7.1	
3	0	0	544	30	9	40	20	31.9	20
4	0	0	488	8			22	9.2	
5	0	0	248	10	3	31	24	27.9	22
7	0	0	272	10	3	20	22	25.1	15
8	0	0	76	1	2	14	21	45.8	39
9	0	0	184	3			22	13.2	
10	0	0	368	11	7	45	23	35.2	24
11	0	0	152	8	6	52	25	83.1	73
12	0	0	356	5			24	12.0	
13	0	0	392	4			34	7.6	
15	0	0	416	5			29	5.7	
16	0	0	200	4			19	15.8	
17	0	0	92	1			21	1.8	
18	0	0	352	4			28	5.8	
19	0	0	264	4			26	11.9	
20	0	0	276	8	3	28	29	26.4	18
21	0	0	236	4	2	4	19	17.4	10
22	0	0	104	2			21	12.4	
23	0	0	288	4			24	12.7	
24	0	0	448	6	4	24	26	22.9	12
25	0	0	568	12	6	41	24	25.5	15
26	0	0	124	2	1	0	18	16.9	9
27	0	0	248	12	7	51	23	56.0	46
28	0	0	128	7	2	20	19	26.4	19
29	0	0	120	1			30	6.0	
30	0	0	392	13	1	5	19	10.7	3
31	0	0	100	3	3	29	20	75.3	68
32	0	0	216	3	2	8	32	14.9	8
33	0	0	336	9	2	14	21	13.7	7
34	0	0	444	5	2	2	29	11.9	4
35	0	0	108	6	2	20	20	38.3	31
37	0	0	132	6	2	15	18	27.8	20
38	0	0	120	2	1	3	27	13.4	8
39	0	0	68	2	2	14	30	45.8	41
40	0	0	340	7	5	54	27	25.4	20
41	0	0	52	1	1	6	23	20.3	14
42	0	0	488	8	3	29	28	12.1	7
43	0	0	24	0	0	1	23	38.2	32
44	0	0	264	11	6	48	19	26.4	19
45	0	0	204	10	3	31	19	37.6	30
46	0	0	428	12	6	64	22	25.6	19
47	0	0	260	7	5	30	20	22.1	15
48	0	0	56	24	1	11	19	34.7	27
49	0	0	264	4	1	8	33	8.3	4

FIGURE 2.9.2.3. UTCS/BPS 15 MINUTE STATUS AND PERFORMANCE REPORT

UTCS SYSTEM PERFORMANCE REPORT

CURRENT CUMULATIVE MOE

OUT OF TOLERANCE LINK NUMBER	HISTORY VOL (VEH)	HISTORY OCC (PCT)	VOL (VPH)	OCC (PCT)	QUEUE (VEH/CYCLE)	STOPS (NO.)	AV.SP. (MPH)	TRAV.TIME (SEC/VEH)	DELAY (SEC/VEH)
50	0	0	124	2			23	11.1	
51	0	0	172	3			20	3.4	
52	0	0	192	3			25	12.5	
53	0	0	456	5			31	9.6	
54	0	0	152	7			16	17.6	
55	0	0	60	1			33	4.9	
56	0	0	236	4			24	10.1	
57	0	0	68	1			23	11.6	
58	0	0	172	3			21	5.8	
59	0	0	88	2			18	1.9	
60	0	0	216	11			17	10.1	
61	0	0	112	2			24	8.7	
62	0	0	220	10	6	42	21	49.9	38
63	0	0	368	13	4	24	24	25.7	16
64	0	0	88	1			21	6.4	
65	0	0	236	3	2	14	28	17.3	9
66	0	0	212	4	2	6	20	23.2	14
67	0	0	336	8	6	47	25	39.3	29
68H	0	0	44	1	0	0	0	0	0
69	0	0	260	11	4	22	23	28.6	19
71	0	0	36	0			28	8.6	
72	0	0	200	5	2	10	23	20.9	10
73	0	0	540	10	2	22	26	11.6	6
74	0	0	316	6	6	46	26	39.9	32
75	0	0	196	8	6	49	21	43.3	32
77	0	0	556	12	5	39	28	19.0	10
78	0	0	264	24			15	6.2	
80	0	0	528	18	7	20	20	27.2	15
81	0	0	280	4			25	8.2	
83	0	0	180	3			19	11.6	
86	0	0	132	3			16	17.3	
87	0	0	136	3			20	9.5	
88	0	0	220	9	3	26	23	23.3	17
89	0	0	196	3	4	24	27	47.2	38
90	0	0	188	13	4	41	16	41.2	32
91	0	0	280	5			23	13.2	
92	0	0	428	7			20	3.8	
93	0	0	360	20	3	27	19	23.7	13
95	0	0	160	4	3	11	21	27.6	16
96	0	0	136	6			11	25.6	
98	0	0	260	15	5	41	24	42.9	33
99	0	0	324	12	3	26	22	19.6	13
100	0	0	48	1			15	18.3	
102	0	0	24	0			13	22.1	
104	0	0	180	3	4	27	30	42.7	34

FIGURE 2.9.2.3. UTCS/BPS 15 MINUTE STATUS AND PERFORMANCE REPORT (CONTINUED)

UTCS SYSTEM PERFORMANCE REPORT

CURRENT CUMULATIVE MOE

OUT OF TOLERANCE LINK NUMBER	HISTORY VOL (VEH)	HISTORY OCC (PCT)	VOL (VPH)	OCC (PCT)	QUEUE (VEH/CYCLE)	STOPS (NO.)	AV.SP. (MPH)	TRAV.TIME (SEC/VEH)	DELAY (SEC/VEH)
105	0	0	160	5	2	17	17	24.3	16
106	0	0	252	13			14	19.4	
107	0	0	328	6			21	4.6	
108	0	0	204	8	3	25	23	25.4	15
109	0	0	516	13	5	30	25	19.1	9
110	0	0	220	6	4	28	22	38.7	29
111	0	0	220	12	2	20	24	17.0	11
112	0	0	236	9	4	30	20	30.7	21
113	0	0	300	4			25	8.6	
114	0	0	528	8	1	9	27	11.6	2
116	0	0	476	9			26	6.6	
117	0	0	368	5			25	12.4	
118	0	0	76	1			40	7.6	
119	0	0	364	4			26	11.8	
120	0	0	284	5			20	10.3	
121	0	0	208	4			19	8.4	
122	0	0	388	6			21	5.8	
123	0	0	264	4			22	10.5	
124	0	0	216	7	5	36	22	35.7	24
125	0	0	440	12	6	32	20	27.6	15
126	0	0	336	5			23	8.6	
127	0	0	332	7	6	34	24	34.8	26
128	0	0	252	3			26	8.1	
129	0	0	248	6	3	10	22	24.6	13
130	0	0	408	5			27	10.7	
131	0	0	56	1			25	8.4	
132	0	0	304	5			20	14.1	
133	0	0	216	3			26	11.7	
134	0	0	396	6			24	10.1	
135	0	0	104	4	2	14	23	33.3	25
136	0	0	112	1			29	7.6	
137	0	0	176	4	2	14	27	25.9	17
138	0	0	308	13	6	32	19	29.1	16
139	0	0	336	8			18	14.7	
140	0	0	260	4			23	9.1	
141	0	0	260	5			21	10.1	
142	0	0	304	5			22	9.6	
143	0	0	284	4			23	12.8	
144	0	0	72	2			24	13.0	
146	0	0	368	6	3	18	24	18.9	10
147	0	0	396	15	5	42	23	29.7	19
148	0	0	368	5			23	9.1	
149	0	0	308	7	5	41	23	29.9	21
150	0	0	260	3			25	8.9	
151	0	0	284	6	3	14	24	22.4	12

FIGURE 2.9.2.3. UTCS/BPS 15 MINUTE STATUS AND PERFORMANCE REPORT (CONTINUED)

UTCS SYSTEM PERFORMANCE.REPORT

CURRENT CUMULATIVE MOE

OUT OF TOLERANCE LINK NUMBER	HISTORY VOL (VEH)	HISTORY OCC (PCT)	VOL (VPH)	OCC (PCT)	QUEUE (VEH/CYCLE)	STOPS (NO.)	AV.SP. (MPH)	TRAV.TIME (SEC/VEH)	DELAY (SEC/VEH)
152	0	0	396	5			25	7.9	
153	0	0	344	15	5	29	22	32.6	21
154	0	0	288	13	3	20	24	24.2	14
155	0	0	96	1			23	9.4	
156	0	0	508	9			19	6.8	
157	0	0	192	3	6	38	26	52.6	45
158	0	0	288	13	5	35	19	29.7	17
159	0	0	104	4	3	22	19	55.8	44
160	0	0	548	15	2	16	24	14.3	4
161	0	0	296	9	6	35	19	38.4	28
162	0	0	304	6			21	4.0	
163	0	0	144	7	3	15	22	37.0	28
164	0	0	472	15	6	32	20	24.5	12
165	0	0	20	7			15	14.5	
166	0	0	36	0			29	8.3	
167	0	0	340	5			22	10.2	
168	0	0	80	7	4	18	19	117.5	107
169	0	0	324	5			25	8.4	
170	0	0	120	10	4	41	16	68.1	59
171	0	0	124	6	1	1	15	21.0	9
172	0	0	204	4			18	7.8	
173	0	0	56	9	4	38	16	216.6	201
174	0	0	340	9	2	35	22	10.2	0
175	0	0	348	16	2	17	17	14.5	6
177	0	0	276	5	4	30	21	34.7	25
178	0	0	240	18			16	7.9	
179	0	0	300	5			22	11.1	
180	0	0	352	6			21	8.9	
181	0	0	292	6			20	14.3	
183	0	0	336	5	5	43	23	27.2	18
184	0	0	256	14	4	32	19	32.6	25
185	0	0	448	15	7	49	19	26.3	13
186	0	0	284	13	5	36	21	26.8	15
187	0	0	344	15	5	41	20	24.5	15
188	0	0	148	21			10	20.9	
189	0	0	328	14	2	22	27	17.5	9
190	0	0	248	6	9	22	21	47.4	38
191	0	0	300	5	7	59	24	40.4	31
193	0	0	340	8			19	7.1	
194	0	0	276	8	4	45	23	41.6	32
193	0	0	184	5	1	11	28	15.1	10
195	0	0	40	1			18	10.6	
197	0	0	448	17	5	17	28	9.0	0
198	0	0	588	20	10	40	26	28.2	19
199	0	0	188	6	4	41	31	8.0	0

FIGURE 2.9.2.3. UTCS/BPS 15 MINUTE STATUS AND PERFORMANCE REPORT (CONTINUED)

UTCS SYSTEM PERFORMANCE REPORT

CURRENT CUMULATIVE MOE

OUT OF TOLERANCE LINK NUMBER	HISTORY VOL (VEH)	HISTORY OCC (PCT)	VOL (VPH)	OCC (PCT)	QUEUE (VEH/CYCLE)	STOPS (NO.)	AV.SP. (MPH)	TRAV.TIME (SEC/VEH)	DELAY (SEC/VEH)
200	0	0	184	3			23	5.3	
201	0	0	256	4	4	22	28	37.1	28
202	0	0	620	9			26	6.3	
203	0	0	356	12	3	25	25	13.7	8
204	0	0	144	2			22	13.4	
205	0	0	288	3			29	7.2	
206	0	0	684	7			32	9.4	
207	0	0	276	4	3	6	29	18.5	10
208	0	0	596	7	2	14	32	7.4	3
209	0	0	100	3	5	32	21	103.1	92
210	0	0	164	4	2	17	22	25.8	15
211	0	0	248	4			19	16.6	
212	0	0	376	7	3	15	31	20.5	12
213	0	0	660	7			32	8.4	
214	0	0	468	6	3	18	30	15.3	7
215	0	0	372	8	1	11	34	12.6	5
216	0	0	348	11	7	35	24	31.5	21
217	0	0	576	10	5	35	30	21.3	13
218	0	0	236	6	4	22	31	36.1	28
219	0	0	192	3			21	9.9	
220	0	0	140	2			22	9.5	
221	0	0	320	9			17	4.4	
222	0	0	416	10			17	4.4	
223	0	0	200	5			18	15.0	
224	0	0	208	4	5	36	25	43.1	33
225	0	0	316	5			21	12.9	
226	0	0	204	4	5	33	23	48.9	38
227	0	0	264	4			27	11.6	
228	0	0	344	15			20	3.8	
229	0	0	88	1			17	11.6	
230	0	0	128	2			20	9.9	
231	0	0	680	19			23	11.9	
232	0	0	480	13			19	14.1	
233	0	0	204	2			27	7.6	
234	0	0	568	7			28	7.3	
235	0	0	180	5			15	5.1	
236	0	0	184	4	2	16	30	21.7	13
237	0	0	564	10	6	32	23	21.9	11
238	0	0	280	3			28	7.2	
239	0	0	272	4	1	3	23	9.3	3
240	0	0	280	9	4	31	27	23.3	14
241	0	0	328	5	2	5	27	11.4	6
242	0	0	384	5			29	5.9	
243	0	0	56	1			18	17.0	
244	0	0	340	5			23	8.5	

FIGURE 2.9.2.3. UTCS/BPS 15 MINUTE STATUS AND PERFORMANCE REPORT (CONTINUED)

UTCS SYSTEM PERFORMANCE REPORT

CURRENT CUMULATIVE MOE

OUT OF TOLERANCE LINK NUMBER	HISTORY VOL (VEH)	HISTORY OCC (PCT)	VOL (VPH)	OCC (PCT)	QUEUE (VEH/CYCLE)	STOPS (NO.)	AV.SP. (MPH)	TRAV.TIME (SEC/VEH)	DELAY (SEC/VEH)
245	0	0	220	3			24	7.1	
246	0	0	248	7	5	36	26	36.1	26
247	0	0	512	9	4	25	26	19.3	10
248	0	0	300	7	2	10	24	9.9	4
249	0	0	140	5	6	64	17	97.6	89
250	0	0	392	8	3	28	27	12.3	7
251	0	0	360	5			24	6.4	
252	0	0	356	5	2	8	28	12.8	4
254	0	0	72	1			24	11.7	
255	0	0	160	2			30	8.3	
256*	0	0	192	6			15	18.8	
257*	0	0	132	2			26	5.3	
258*	0	0	548	6			30	12.5	
260*	0	0	372	5			25	15.1	
261*	0	0	312	6			21	14.6	
262*	0	0	528	11			19	14.5	
263*	0	0	520	7			23	11.8	
264*	0	0	348	7			22	3.1	
265*	0	0	288	5			21	17.6	
266*	0	0	420	6			24	15.4	
267*	0	0	364	4			32	11.7	
269*	0	0	32	0			39	9.5	
270*	0	0	312	4			27	4.6	

FIGURE 2.9.2.3. UTCS/BPS 15 MINUTE STATUS AND PERFORMANCE REPORT (CONTINUED)

BPS SYSTEM STATUS

SECTION	BPS	INTERSECTIONS PRE-EMPT	INHIBIT	FAILURES
1	1	0	0	0
2	3	0	2	0
3	13	0	5	1
4	4	0	2	0

FIGURE 2.9.2.4. UTCS/BPS 15 MINUTE STATUS AND PERFORMANCE REPORT

BPS 15-MINUTE ZONE SUMMARY

SECT	INTSCT	ZONE	DIR	15-MIN. MODE OF OPER.	STOP BUS VOL.	THRU BUS VOL.	ELIGIBLE STOP BUSES	ELIGIBLE THRU BUSES	EXTNS GRANTED	HELPED STOP BUSES	HELPED THRU BUSES	PSG. MIN. SAVED
1	17	5	W	ACT	0	3	0	2	1	0	0	0
		6	E	ACT	0	0	0	0	0	0	0	0
		7	S	ACT	0	1	0	0	1	0	0	0
	SECTION TOTALS				0	4	0	2	2	0	0	0
2	10	1	N	INH	0	2	0	0	0	0	0	0
		2	S	INH	0	1	0	0	0	0	0	0
	12	3	N	INH	0	1	0	0	0	0	0	0
		4	S	INH	0	1	0	0	0	0	0	0
	120	67	N	ACT	0	5	0	1	2	0	1	32
		68	S	ACT	1	0	1	0	2	0	0	0
	121	69	N	ACT	0	2	0	2	2	0	0	0
		70	S	ACT	0	1	0	0	0	0	0	0
	123	71	N	ACT	0	2	0	0	1	0	0	0
		72	S	ACT	0	1	0	1	1	0	1	16
	SECTION TOTALS				1	16	1	4	8	0	2	48
3	54	15	NW	ACT	0	4	0	3	2	0	1	39
		16	N	ACT	0	1	0	0	0	0	0	0
		17	SE	ACT	0	2	0	1	1	0	1	21
	55	18	W	INH	0	4	0	2	2	0	2	46
		19	SE	INH	0	0	0	0	2	0	0	0
	59	22	W	INH	0	4	0	0	1	0	0	0
		23	E	INH	0	3	0	1	1	0	0	0
		24	S	INH	0	4	0	2	2	0	0	0
	60	25	W	INH	2	3	0	0	0	0	0	0
		26	N	INH	0	0	0	0	0	0	0	0
		27	E	INH	4	0	0	0	0	0	0	0
	66	30	NW	ACT	0	4	0	2	1	0	1	27
		31	SE	ACT	0	2	0	2	2	0	2	73
	68	32	W	ACT	2	0	0	0	0	0	0	0
		33	S	ACT	0	0	0	0	0	0	0	0
	70	34	NW	ACT	0	0	0	0	0	0	0	0
		35	SE	ACT	0	2	0	0	0	0	0	0
		36	S	ACT	0	1	0	0	0	0	0	0
	72	37	W	ACT	0	5	0	3	3	0	0	0
		38	E	ACT	0	0	0	0	3	0	0	0
		39	S	ACT	0	3	0	1	1	0	0	0
	73	40	W	INH	1	3	0	2	3	0	2	66
		41	N	INH	0	0	0	0	0	0	0	0
		42	E	INH	1	2	0	1	2	0	0	0
	76	43	S	ACT	1	0	1	0	1	0	0	0
	77	44	N	ACT	0	1	0	1	1	0	0	0
	82	45	N	ACT	0	1	0	1	3	0	0	0

FIGURE 2.9.2.5. UTCS/BPS 15 MINUTE STATUS AND PERFORMANCE REPORT

BPS 15-MINUTE ZONE SUMMARY 14

SECT	INTSCT	ZONE	DIR	15-MIN. MODE OF OPER.	STOP BUS VOL.	THRU BUS VOL.	ELIGIBLE STOP BUSES	ELIGIBLE THRU BUSES	EXTNS GRANTED	HELPED STOP BUSES	HELPED THRU BUSES	PSG. MIN. SAVED
		46	S	ACT	0	12	0	6	3	0	0	0
	84	47	S	FAIL	0	0	0	0	0	0	0	0
	85	48	N	ACT	0	2	0	1	1	0	0	0
	88	49	W	INH	0	4	0	0	0	0	0	0
		50	N	INH	0	1	0	0	0	0	0	0
		51	E	INH	2	5	0	0	0	0	0	0
		52	S	INH	2	6	0	0	0	0	0	0
	91	53	N	INH	0	0	0	0	0	0	0	0
		54	S	INH	0	0	0	0	0	0	0	0
	93	55	W	ACT	1	0	0	0	0	0	0	0
		56	N	ACT	6	0	0	0	0	0	0	0
		57	S	ACT	0	0	0	0	0	0	0	0
	94	58	W	ACT	5	0	0	0	0	0	0	0
	97	59	N	ACT	0	0	0	0	0	0	0	0
		60	S	ACT	0	0	0	0	0	0	0	0
	99	61	W	ACT	0	3	0	0	5	0	0	0
		62	N	ACT	0	0	0	0	0	0	0	0
		63	E	ACT	2	6	2	3	5	0	1	24
		64	S	ACT	0	3	0	0	0	0	0	0
	SECTION TOTALS				29	91	3	32	45	0	10	296
4	40	8	W	ACT	0	0	0	0	0	0	0	0
		9	E	ACT	0	0	0	0	0	0	0	0
	42	10	W	INH	0	1	0	0	0	0	0	0
		11	E	INH	0	0	0	0	0	0	0	0
	45	12	W	ACT	0	0	0	0	0	0	0	0
		13	S	ACT	0	1	0	0	0	0	0	0
	49	14	N	ACT	0	0	0	0	0	0	0	0
	57	20	W	ACT	0	0	0	0	0	0	0	0
		21	N	ACT	0	1	0	0	0	0	0	0
	115	65	N	INH	1	1	0	0	0	0	0	0
		66	E	INH	0	0	0	0	0	0	0	0
	SECTION TOTALS				1	4	0	0	0	0	0	0
	SYSTEM TOTALS				31	115	4	38	55	0	12	344

FIGURE 2.9.2.5. UTCS/BPS 15 MINUTE STATUS AND PERFORMANCE REPORT (CONTINUED)

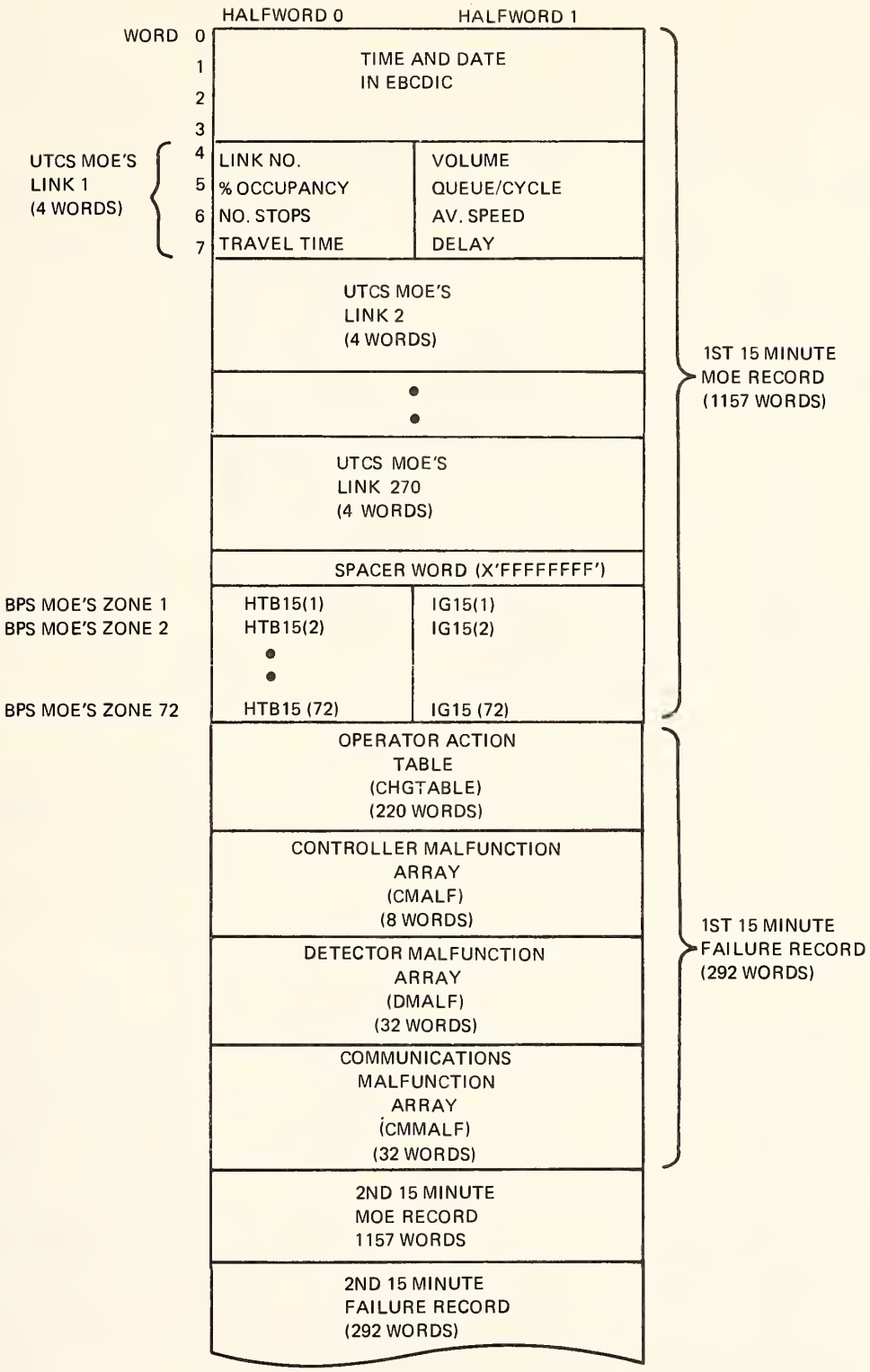


FIGURE 2.9.2.6. 15 MINUTE TAPE FORMAT

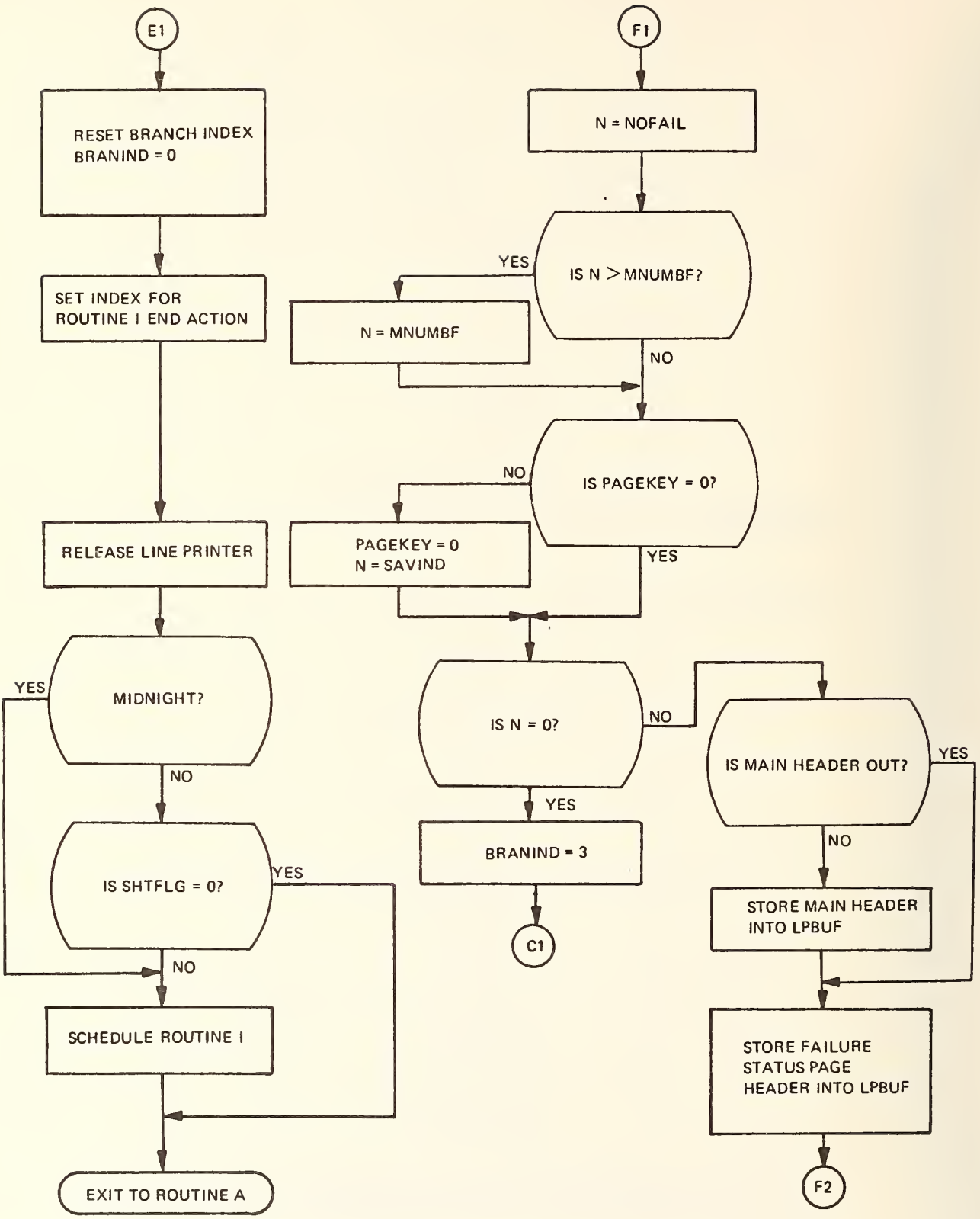


FIGURE 2.9.5.5. ROUTINE H SPECIFICATION

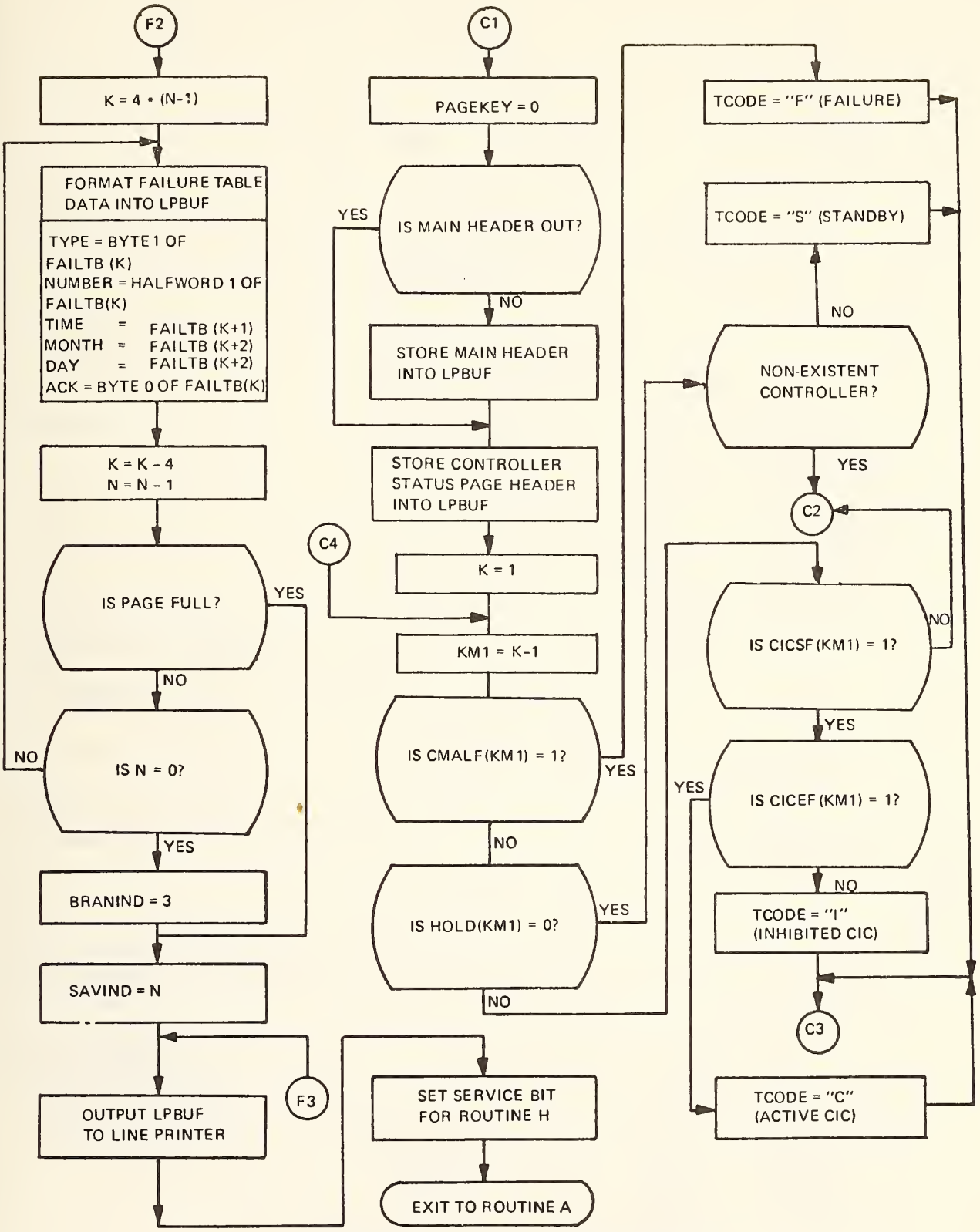


FIGURE 2.9.5.6. ROUTINE H SPECIFICATION

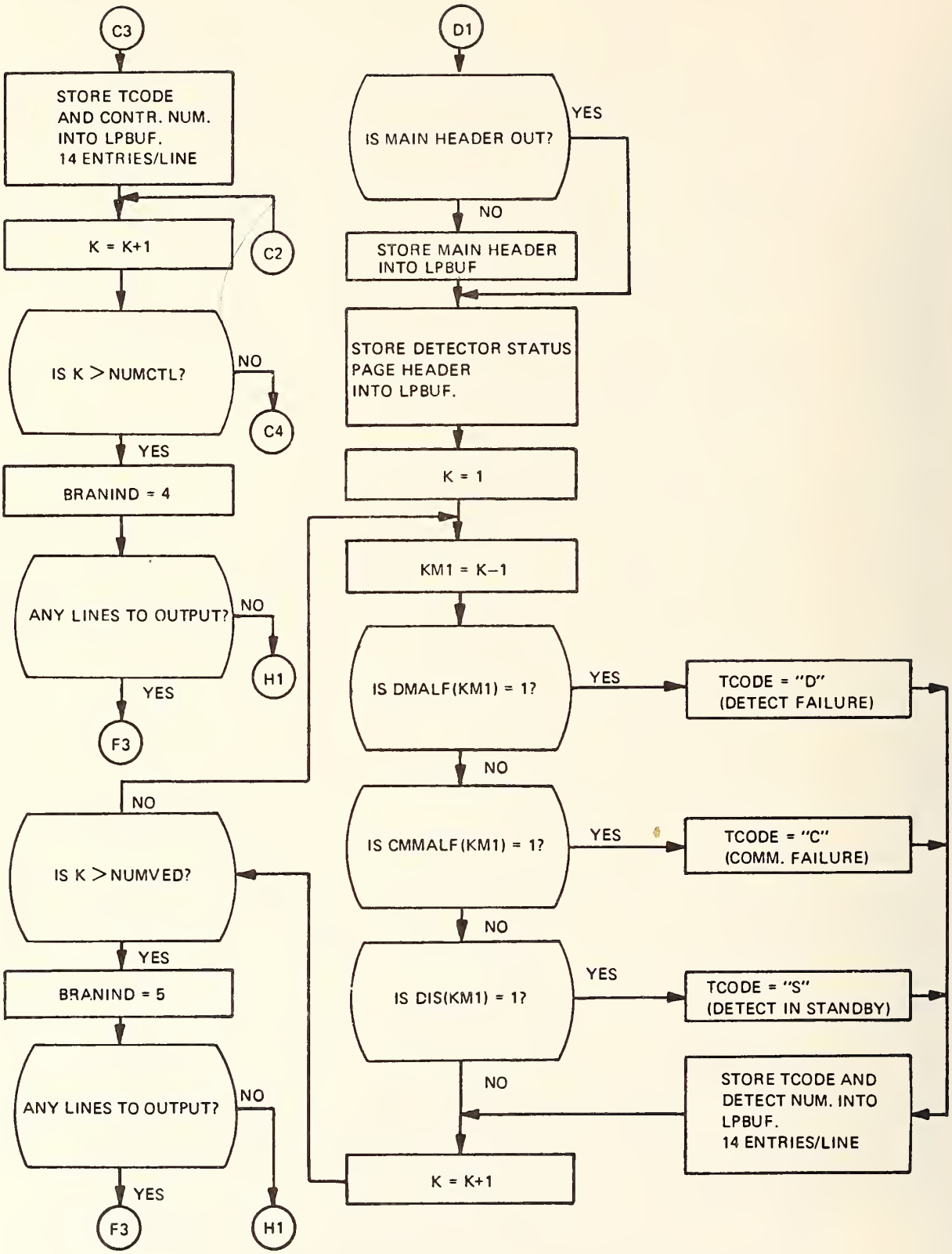


FIGURE 2.9.5.7. ROUTINE H SPECIFICATION

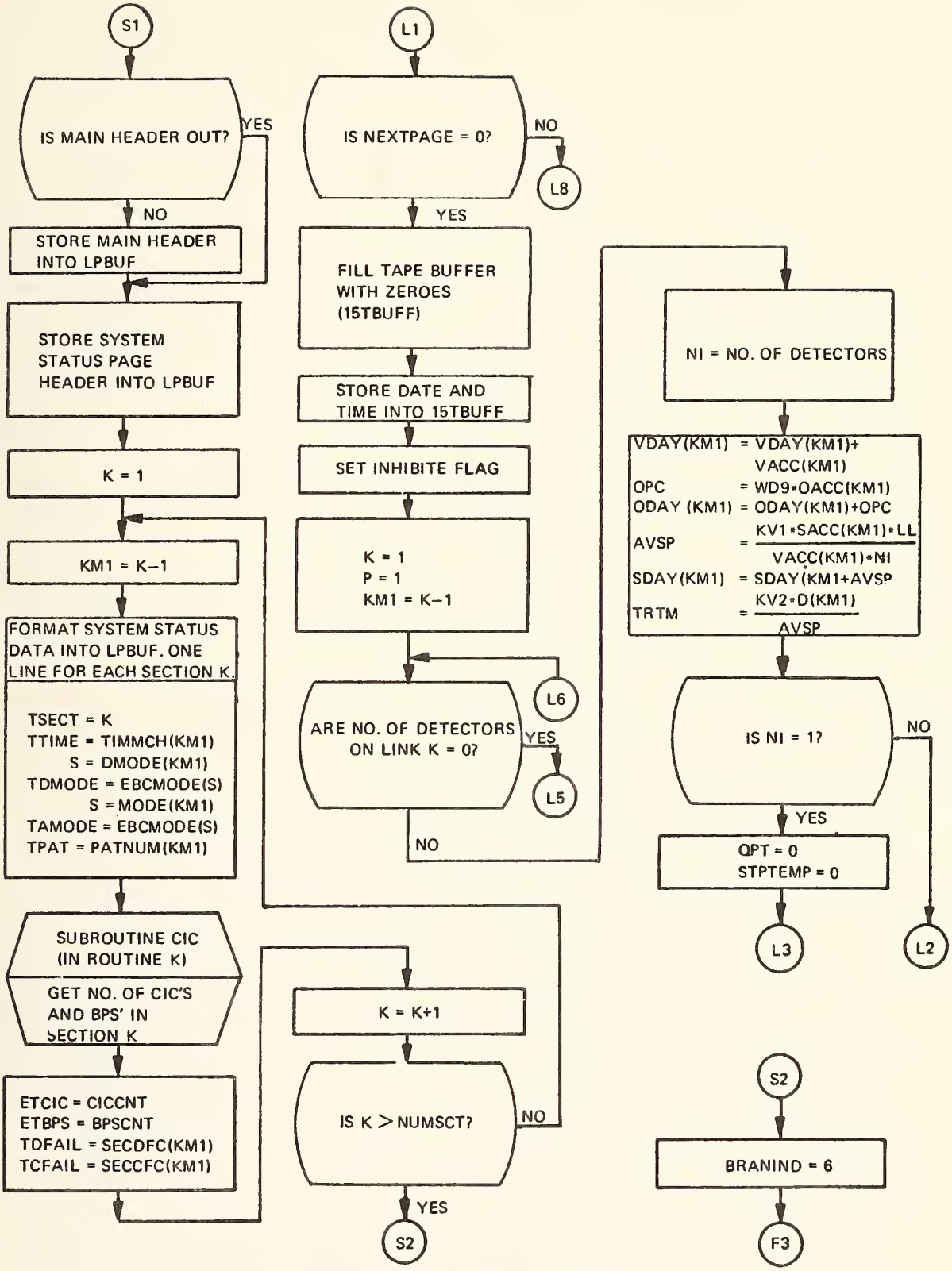


FIGURE 2.9.5.8. ROUTINE H SPECIFICATION

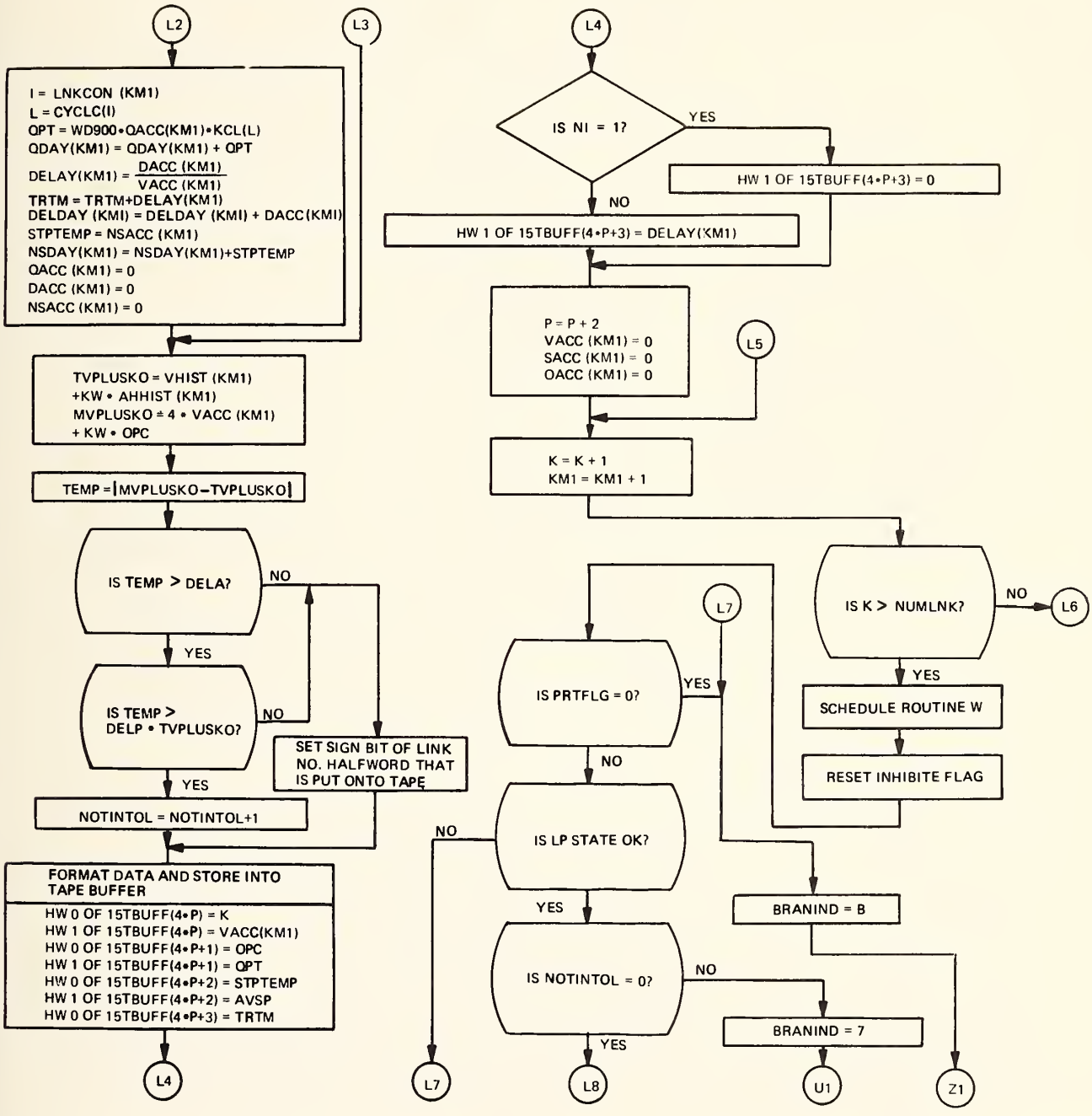


FIGURE 2.9.5.9. ROUTINE H SPECIFICATION

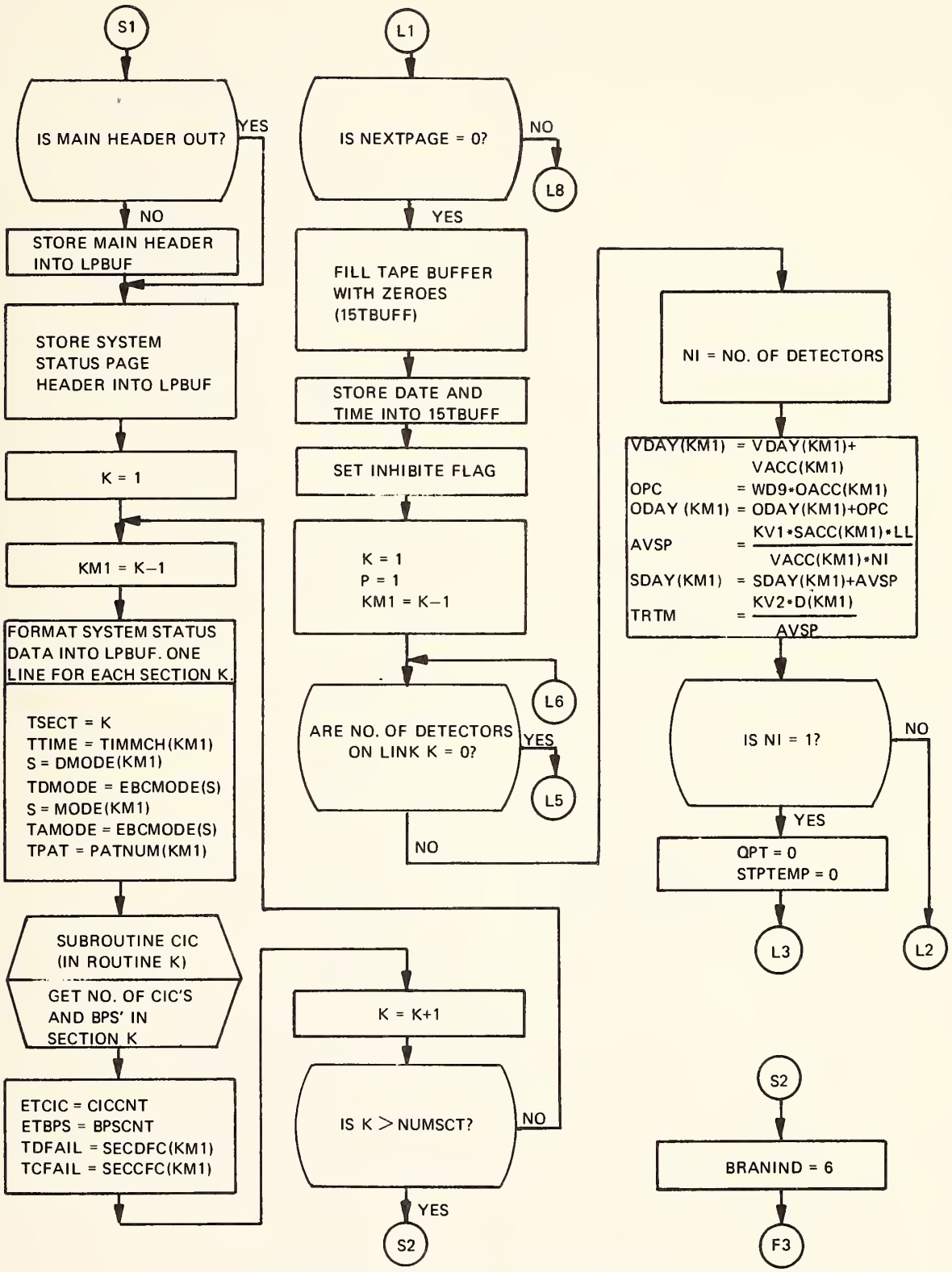


FIGURE 2.9.5.8. ROUTINE H FLOW CHART

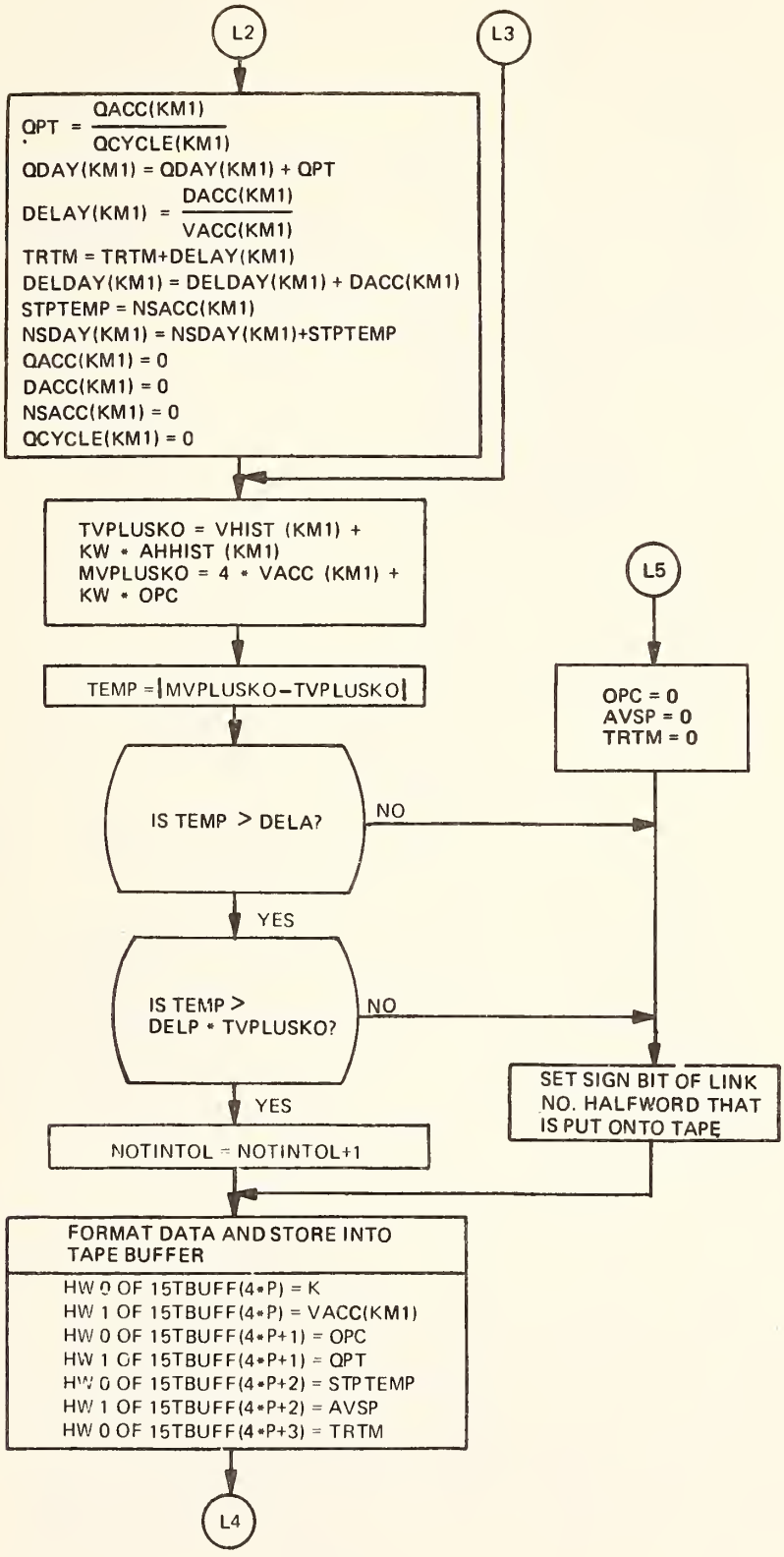


FIGURE 2.9.5.9. ROUTINE H FLOW CHART

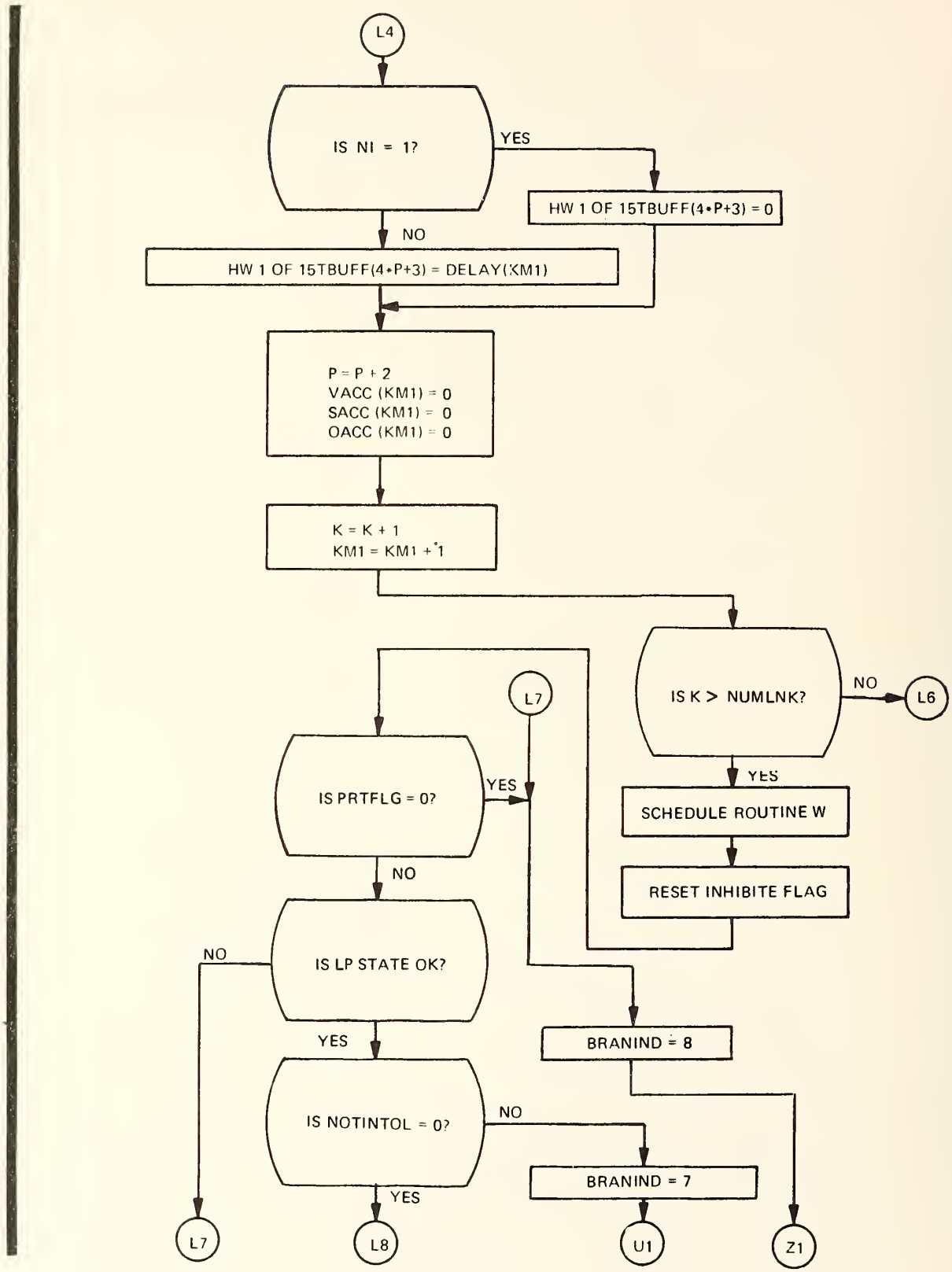


FIGURE 2.9.5.9. ROUTINE H FLOW CHART

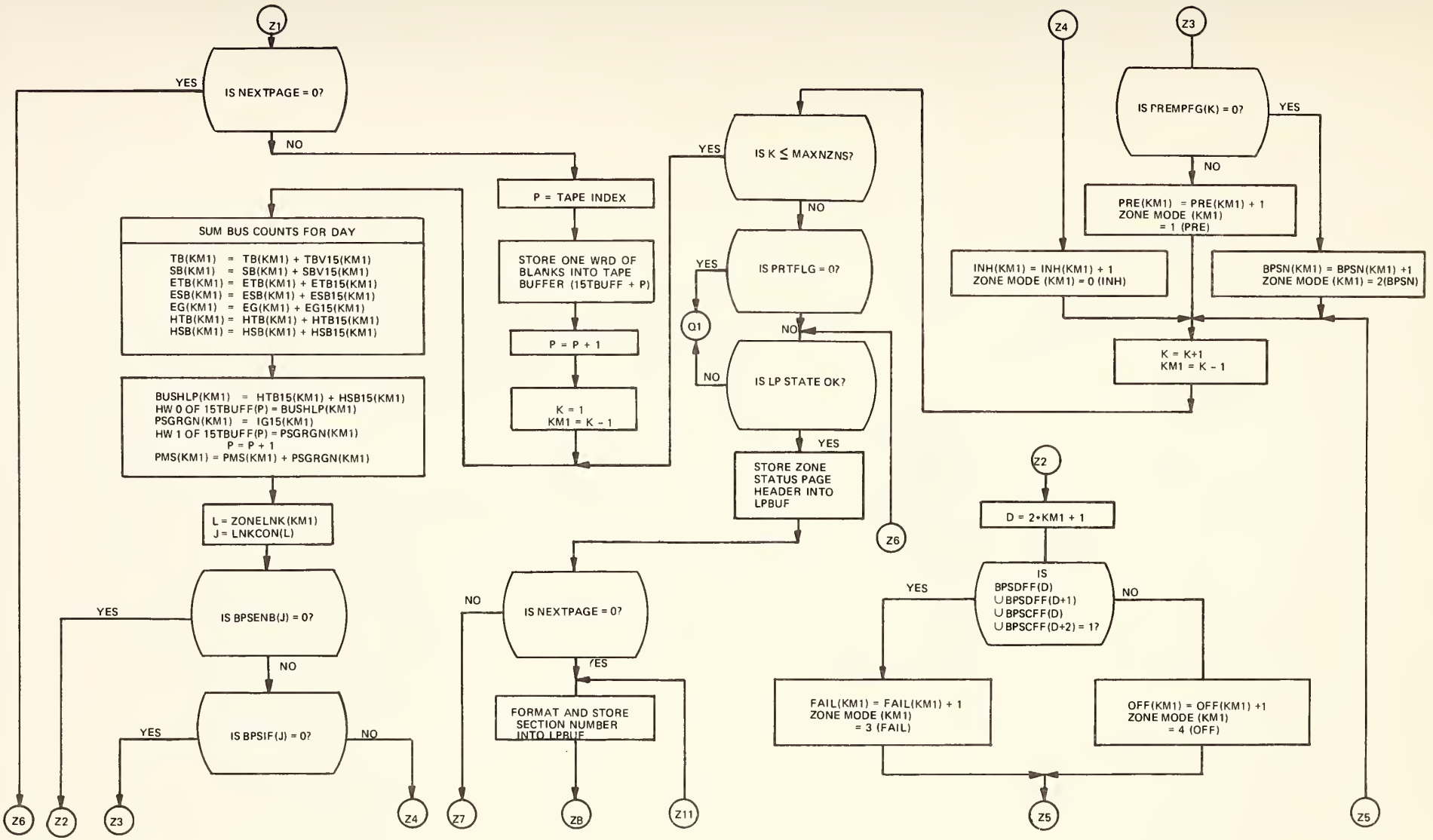


FIGURE 2.9.5.13. ROUTINE H SPECIFICATION

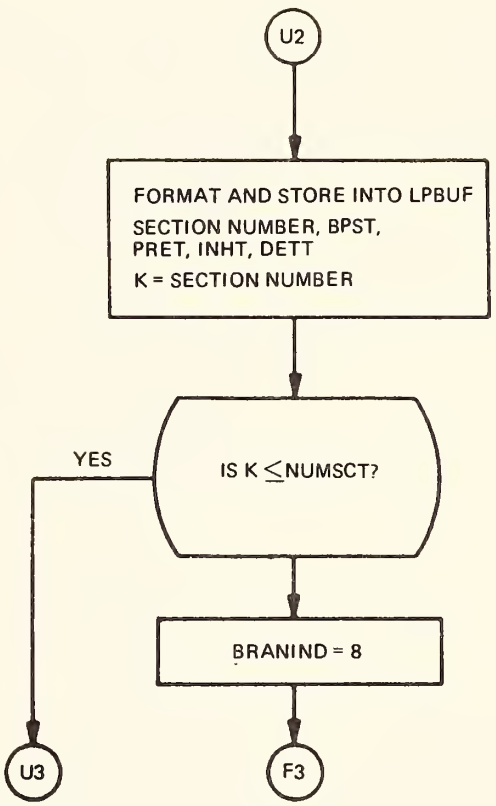


FIGURE 2.9.5.12. ROUTINE H FLOW CHART

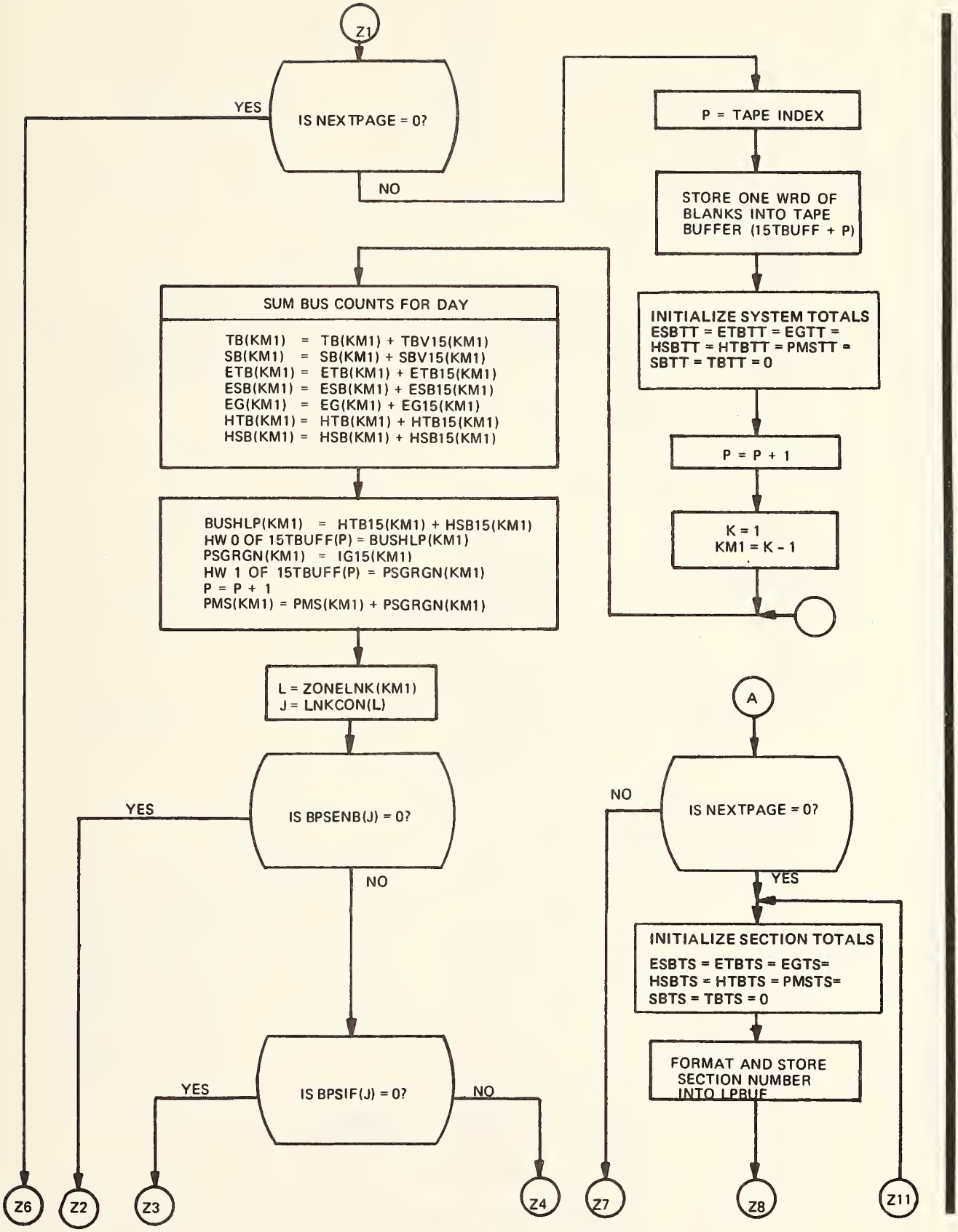


FIGURE 2.9.5.13. ROUTINE H FLOW CHART

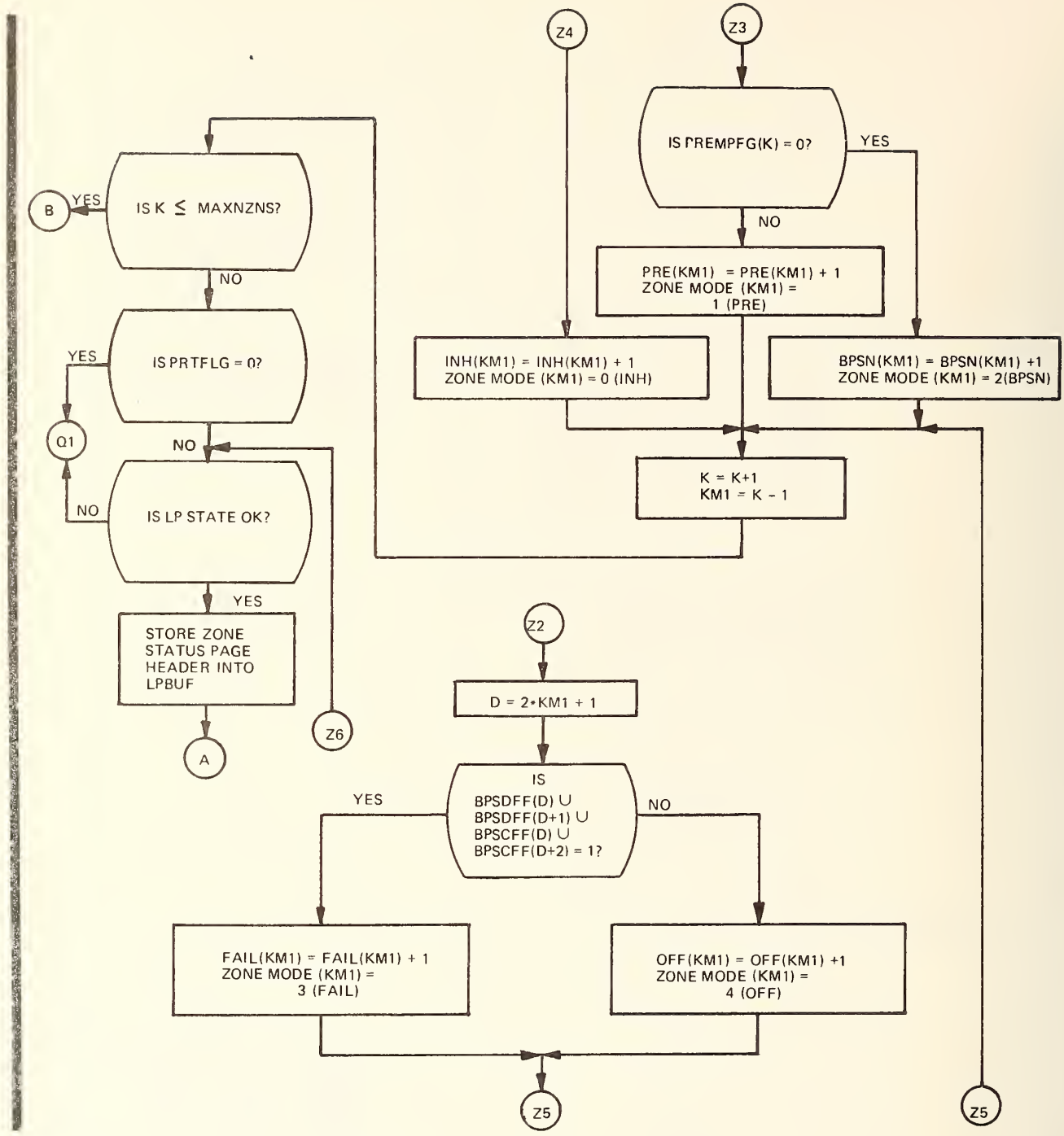


FIGURE 2.9.5.13. ROUTINE H FLOW CHART

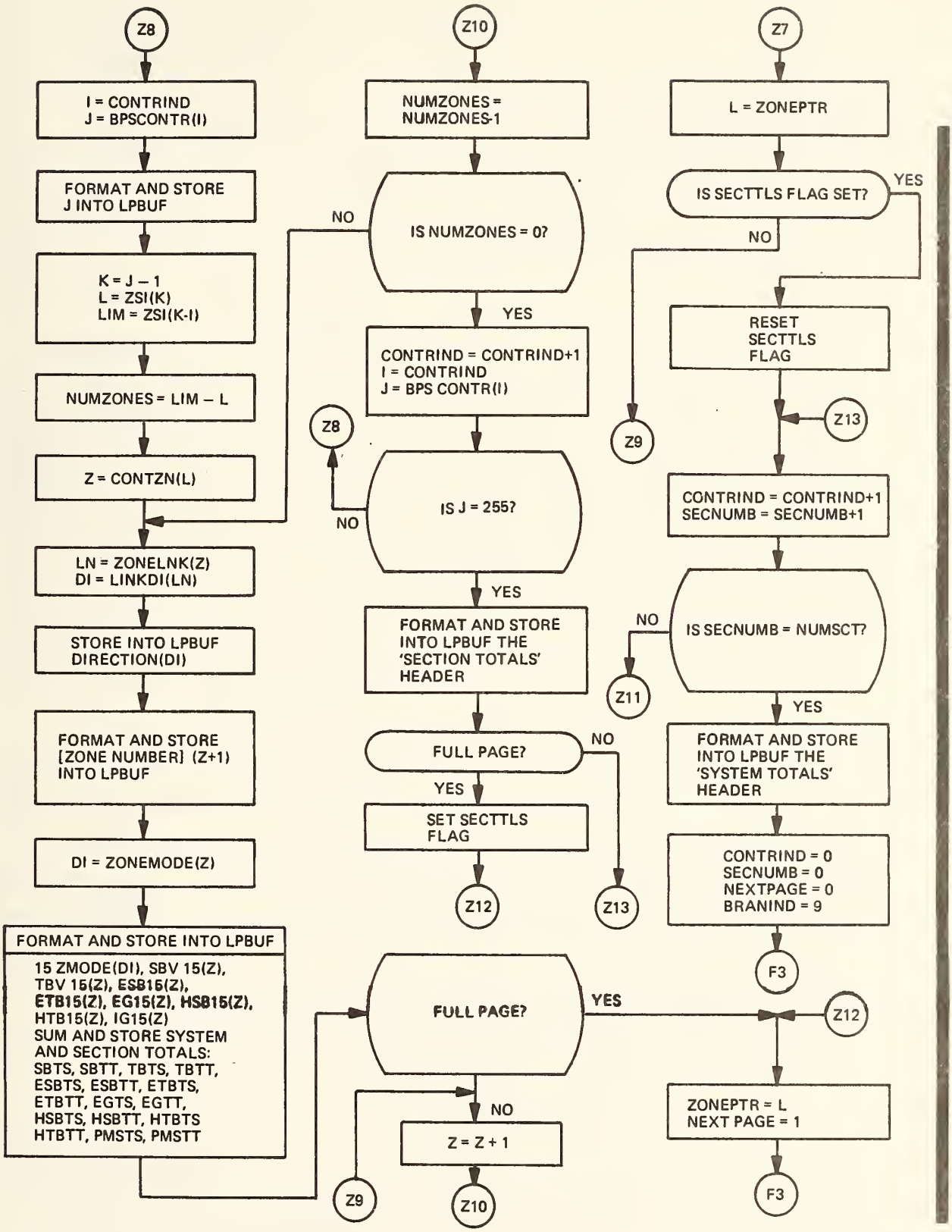


FIGURE 2.9.5.14. ROUTINE H FLOW CHART

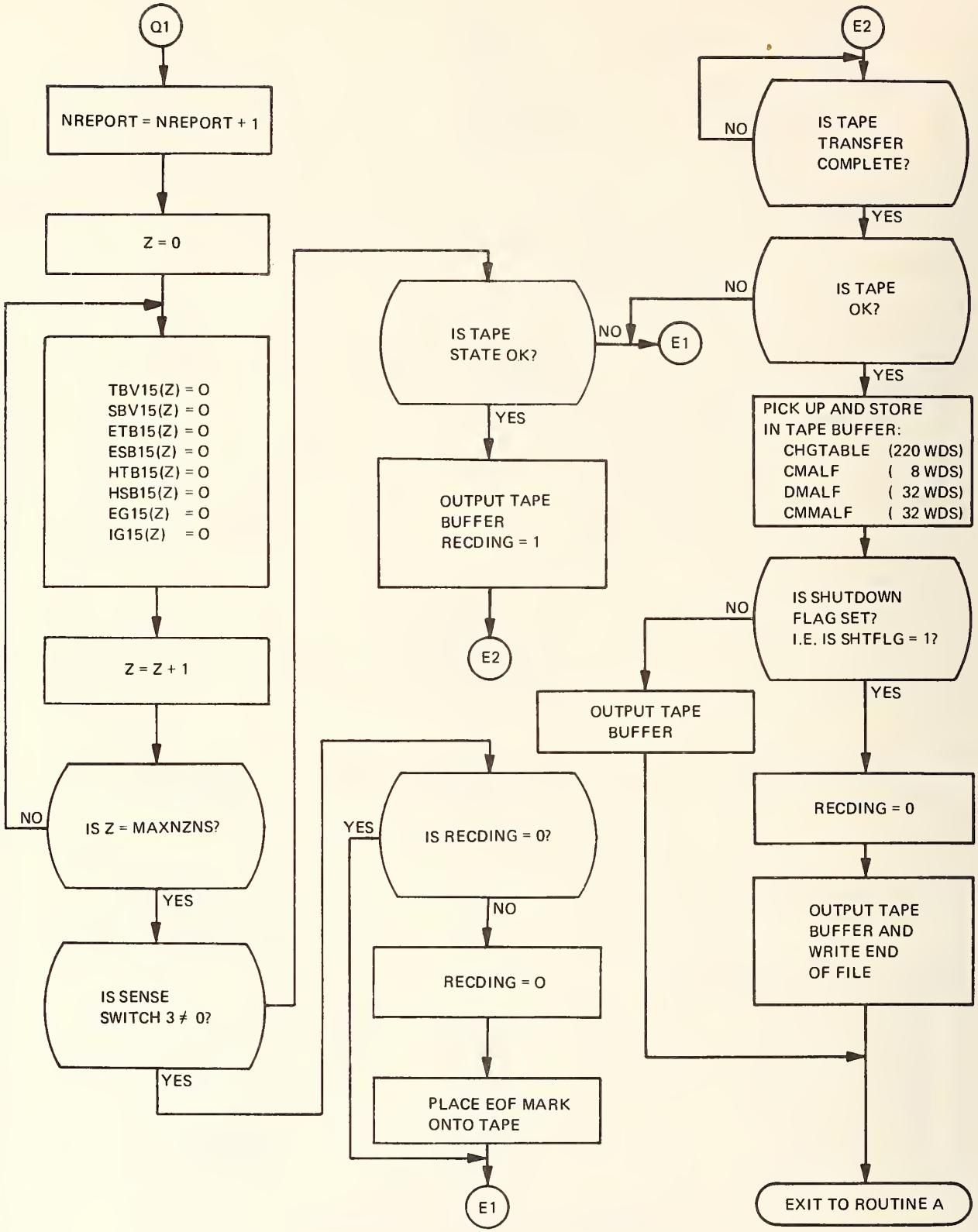


FIGURE 2.9.5.15. ROUTINE H FLOW CHART

2.10 Routine I (End of Day Report) Specification

2.10.1 Purpose

At the end of each 24-hour period or when the system is instructed to shutdown, Routine I produces a hard copy report which is a summary of the UTCS and BPS systems. This report contains a link by link summary of all measures of effectiveness as well as section and overall system measures of effectiveness. The BPS part of the report contains summaries of bus priority operation on a section basis and for each individual bus zone.

2.10.2 Method

Upon entry, Routine I begins processing the links in increasing numerical order. For each link that has detectors associated with it, it prints out accumulated daily volume (VDAY), accumulated daily percent occupancy (OPC = ODAY/NREPORT), accumulated daily speed (AVSP = SDAY/NREPORT), accumulated daily travel time (TTTEMP = D*VDAY/5280*AVSP). If the controller associated with a link is not on line and the link has at least one failed detector, speed (AVSP) and travel time (TTTEMP) are set to zero. In addition, for all multi-detector links, it prints out accumulated daily stops (STPTEMP = NSDAY), accumulated daily delay (DELTEMP = DELDAY/3600), and accumulated daily queues (QPT = QDAY/NREPORT). If the controller associated with a multidetector link is in standby, the stops (STPTEMP), delay (DELTEMP), and queues (QPT) are set to zero. For single detector links "NI" is printed out for stops, delays and queues.

For each section, totals are printed out for volume (VSECT), travel time (TTSECT/NLAVSP), delay (DELSECT) and stops (STPSECT). Averages are printed out for occupancy (OSECT/NLS), queues (QSECT/NLI) and speed (SSECT/NLAVSP).

After all the links and sections summaries are printed out, system performance is printed. This report contains volume (VSUM), travel time (TTSUM), delays (DELSUM), stops (STPSUM), average occupancy (OSUM/NLSS), average speed (SSUM/NLAVSPS), average queues (QSUM/NLIS).

The BPS end of day zone summary processes each zone and prints them out by section, maintaining increasing numerical order within a section. For each zone the

15 minute mode of operation is printed out. That is, the number of 15-minute periods during the day that the zone was in a failed mode (FAIL), a released mode (OFF), an active mode (BPSN), a pre-empt mode (PRE), or an inhibited mode (INH). For each zone the stop and through bus volumes (SB, TB), the eligible stop and through bus volumes (ESB, ETB), the number of extensions granted (EG), the helped stop and through bus volumes (HSB, HTB), and the passenger minutes saved (PMS) are printed out. The section and system totals for SB, TB, ESB, ETB, EG, HSB, HTB and PMS are also printed out.

Routine I then initializes to zero the mode of operation counts, the volume counts, the extension count and the passenger minutes saved count for each zone. It also initializes to zero the accumulated daily queues (QDAY), accumulated daily stops (NSDAY), accumulated daily delay (DELDAY), accumulated daily volume (VDAY), accumulated daily occupancy (ODAY), and the accumulated daily speed (SDAY).

Routine I checks to see if it is midnight (FMTODC = O). If it isn't, the end of day count (EODC) is incremented and Routine Q (SHUT DOWN) is scheduled. Routine I then exits. If it is midnight, the holiday flag (HOLIDF) is set: O - no holiday, 1 - Saturday type holiday, 2 - Sunday type holiday. The end of day count (EODC) is reset to 1. Routine I then exits.

2.10.3 Repetition Rate

This routine is entered once per 24-hour period or at any time the shutdown procedure is called.

2.10.4 Cross-Reference

This routine is called at Level 3. It schedules Routine Q, when required.

END OF DAY REPORT

DATE MAR 18 74 TIME 0953

INITIAL TIME 0715 REPORT NO 1

		LINK	VOLUME VEHICLES	TRAV.TIME VEH-HRS	DELAY HRS	STOPS VEH	OCCUPANCY PERCENT	QUEUE VEH/CYCLE	SPEED MPH
SECTION	1	1	918	1.8	NI	NI	4.5	NI	22.7
		2	0	.0	.0	0	.0	.0	.0
		3	1514	16.0	10.5	1018	39.0	6.3	17.7
		4	1372	3.8	NI	NI	8.3	NI	20.3
		5	699	7.3	6.0	485	19.3	4.2	21.1
		6	0	.0	NI	NI	.0	NI	.0
		7	840	6.3	4.0	314	12.3	3.5	21.5
		8	371	5.3	4.5	309	8.3	2.8	17.4
		9	535	2.0	NI	NI	4.3	NI	19.3
		10	1344	11.8	7.5	487	15.0	7.4	21.5
		11	754	12.3	10.0	551	16.0	5.9	22.4
		12	1109	4.0	NI	NI	6.8	NI	22.3
		13	1591	3.5	NI	NI	5.5	NI	32.2
		15	1621	2.8	NI	NI	7.3	NI	25.4
		16	765	4.0	NI	NI	9.5	NI	15.8
		17	291	.0	NI	NI	1.8	NI	17.2
		18	1267	2.0	NI	NI	5.3	NI	27.3
		50	444	1.3	NI	NI	2.5	NI	22.4
		51	403	.3	NI	NI	2.5	NI	17.9
		52	1066	3.8	NI	NI	6.0	NI	23.1
		53	1477	4.5	NI	NI	10.3	NI	27.3
		54	544	3.0	NI	NI	15.5	NI	13.4
		55	178	.3	NI	NI	.8	NI	24.6
		56	1111	3.5	NI	NI	7.0	NI	20.5
		57	232	.8	NI	NI	1.3	NI	20.6
TOTAL			20446	99.8	42.5	3164			
AVERAGE				4.2	7.1	527	8.3	5.0	20.6
SECTION	2	19	878	3.0	NI	NI	5.0	NI	23.7
		20	786	4.8	3.0	312	7.8	3.3	29.3
		21	774	3.0	1.5	64	5.3	2.2	18.7
		22	574	2.0	NI	NI	5.0	NI	19.9
		23	1174	4.0	NI	NI	9.0	NI	23.8
		24	1549	11.3	6.0	369	14.3	4.8	22.4
		25	1612	13.5	8.5	467	17.3	6.5	22.3
		26	404	6.8	6.0	375	11.3	3.1	17.9
		27	801	10.8	8.5	703	13.0	6.6	22.7
		28	495	4.5	3.5	317	12.0	2.7	18.8
		29	556	.8	NI	NI	3.0	NI	29.7
		30	1177	5.0	2.5	262	17.5	2.5	18.0
		31	283	6.5	6.0	454	5.8	3.8	17.2
		32	629	2.5	1.5	89	3.0	2.0	33.2
		33	1028	4.3	2.5	280	9.0	2.5	20.9

FIGURE 2.10.2.1. UTCS/BPS END OF DAY REPORT

END OF DAY REPORT

DATE MAR 18 74 TIME 0953

INITIAL TIME 0715 REPORT NO 1

	LINK	VOLUME VEHICLES	TRAV.TIME VEH-HRS	DELAY HRS	STOPS VEH	OCCUPANCY PERCENT	QUEUE VEH/CYCLE	SPEED MPH
	34	1601	6.3	2.5	177	8.3	2.7	26.5
	35	440	4.3	3.5	335	10.5	2.9	19.3
	36	0	.0	.0	0	.0	.0	.0
	37	566	4.8	3.5	348	14.3	3.1	17.6
	38	691	3.0	2.0	289	5.8	2.8	22.7
	39	296	3.3	3.0	328	5.0	2.7	27.2
	40	1243	6.8	5.0	560	9.3	4.6	25.7
	41	426	2.8	2.0	245	10.3	2.2	18.5
	42	1793	5.0	2.5	292	9.0	2.6	26.1
	43	170	.8	.5	95	3.0	1.0	21.6
	44	957	5.3	3.5	620	12.8	5.6	19.4
	45	836	7.8	6.0	551	24.3	4.7	16.7
	46	1378	8.5	6.0	713	16.0	5.9	19.9
	47	923	4.3	2.5	345	8.8	4.2	20.5
	48	385	4.3	3.5	321	9.8	2.7	18.5
	49	1017	2.8	1.5	215	5.8	1.9	29.3
TOTAL		25442	152.0	97.0	9126			
AVERAGE			5.1	3.7	351	9.3	3.4	22.3
SECTION 3	50	444	1.3	NI	NI	2.5	NI	22.4
	51	403	.3	NI	NI	2.5	NI	17.9
	58	626	1.0	NI	NI	6.0	NI	20.3
	59	252	.0	NI	NI	1.8	NI	15.6
	60	640	2.0	NI	NI	16.5	NI	14.8
	61	292	.8	NI	NI	5.0	NI	17.2
	62	988	15.5	12.0	539	18.0	7.0	19.1
	63	1282	12.0	7.5	456	25.0	4.8	18.5
	64	328	.5	NI	NI	2.5	NI	19.6
	65	1194	5.0	2.0	183	8.8	2.5	24.8
	66	761	4.3	2.5	99	6.5	2.5	20.5
	67	1254	11.8	7.5	469	19.8	6.1	21.4
	68	13	.0	.0	0	.0	.0	.0
	69	995	7.8	5.0	381	13.0	4.1	21.3
	70	0	.0	NI	NI	.0	NI	.0
	71	192	.5	NI	NI	2.8	NI	21.7
	72	665	5.5	3.5	278	6.5	3.3	22.2
	73	1517	5.0	2.5	289	13.5	2.4	22.7
	74	1238	10.8	7.5	489	15.8	6.1	21.0
	75	748	7.8	5.5	624	11.0	6.5	21.2
	77	1465	8.5	4.5	492	14.0	4.6	25.8
	78	929	1.5	NI	NI	23.0	NI	15.3
	79	0	.0	.0	0	.0	.0	.0
	80	1370	11.3	6.5	318	17.3	5.6	19.1

END OF DAY REPORT

DATE MAR 18 74 TIME 0953

INITIAL TIME 0715 REPORT NO 1

LINK	VOLUME VEHICLES	TRAV.TIME VEH-HRS	DELAY HRS	STOPS VEH	OCCUPANCY PERCENT	QUEUE VEH/CYCLE	SPEED MPH
A1	1229	3.3	NI	NI	10.5	NI	20.9
A2	0	.0	.0	0	.0	.0	.0
A3	698	2.3	NI	NI	17.0	NI	16.8
A5	0	.0	NI	NI	.0	NI	.0
A6	515	3.5	NI	NI	23.8	NI	11.0
A7	393	1.3	NI	NI	7.0	NI	16.2
A8	762	7.0	5.5	652	20.5	5.1	17.6
A9	1201	10.0	6.5	400	13.3	5.0	22.2
90	681	7.3	5.5	604	20.5	5.2	14.3
91	1211	5.3	NI	NI	10.0	NI	19.5
92	1396	1.8	NI	NI	18.5	NI	16.9
93	1181	8.3	4.5	485	23.8	4.1	17.4
95	844	9.0	5.5	393	23.0	4.9	16.0
96	750	5.3	NI	NI	31.0	NI	10.5
98	886	14.0	10.5	784	30.8	7.4	15.7
99	962	10.8	8.0	759	39.5	6.0	13.0
100	145	.5	NI	NI	1.0	NI	15.3
102	81	.3	NI	NI	.5	NI	13.8
104	1353	11.8	8.0	424	12.5	6.3	24.2
105	720	5.5	4.0	343	8.5	3.5	17.9
106	1160	5.8	NI	NI	33.8	NI	14.2
107	1568	2.0	NI	NI	18.0	NI	19.5
108	542	5.8	4.5	430	6.3	4.0	25.7
109	1672	11.8	6.0	374	22.3	4.4	20.1
110	965	11.0	8.0	454	20.3	6.7	17.3
111	630	3.0	2.0	301	12.0	2.5	22.3
112	816	8.5	6.0	494	14.0	5.7	17.5
113	1175	3.3	NI	NI	8.8	NI	20.0
114	906	.0	.0	0	6.5	.0	.0
116	1563	3.8	NI	NI	20.8	NI	19.7
117	1144	4.3	NI	NI	6.0	NI	22.4
118	627	1.3	NI	NI	2.0	NI	35.9
119	1432	5.3	NI	NI	9.3	NI	23.2
120	1080	3.3	NI	NI	17.0	NI	17.8
121	720	2.0	NI	NI	18.3	NI	15.2
122	1775	3.3	NI	NI	21.0	NI	17.6
123	1485	5.5	NI	NI	14.0	NI	17.3
124	1234	4.3	.0	0	15.3	.0	20.2
125	1297	4.8	.0	0	21.0	.0	18.1
126	1303	3.5	NI	NI	11.0	NI	20.3
127	1241	10.3	6.5	473	19.3	6.5	19.3
128	1232	3.3	NI	NI	12.0	NI	21.5
129	1292	10.0	5.5	393	15.3	5.3	19.3
130	1451	4.8	NI	NI	6.8	NI	24.2
131	318	.8	NI	NI	2.0	NI	21.1

FIGURE 2.10.2.1. UTCS/BPS END OF DAY REPORT (CONT)

END OF DAY REPORT

DATE MAR 18 74 TIME 0953

INITIAL TIME 0715 REPORT NO 1

LINK	VOLUME VEHICLES	TRAV.TIME VEH-HRS	DELAY HRS	STOPS VEH	OCCUPANCY PERCENT	QUEUE VEH/CYCLE	SPEED MPH
132	1071	4.5	NI	NI	11.0	NI	18.0
133	679	2.3	NI	NI	4.0	NI	24.2
134	1357	4.3	NI	NI	8.8	NI	20.6
135	498	3.0	2.0	145	5.8	2.4	23.7
136	617	1.3	NI	NI	2.5	NI	28.0
137	888	8.3	5.5	452	9.8	5.0	21.2
138	1062	7.8	4.0	391	14.5	5.4	19.1
139	1046	5.0	NI	NI	11.5	NI	17.6
140	755	1.8	NI	NI	3.8	NI	23.5
141	913	3.0	NI	NI	9.5	NI	16.7
142	1235	4.5	NI	NI	25.8	NI	15.7
143	1215	4.8	NI	NI	7.8	NI	20.2
144	243	1.0	NI	NI	2.5	NI	20.1
145	0	.0	NI	NI	.0	NI	.0
146	1487	8.3	4.0	360	16.8	4.5	19.8
147	1452	11.3	6.5	483	18.3	6.3	21.1
148	1205	4.3	NI	NI	19.0	NI	16.1
149	1134	10.3	7.0	606	11.5	6.2	19.4
150	1165	3.0	NI	NI	5.8	NI	22.6
151	1107	8.3	4.5	312	12.0	4.3	20.3
152	1298	3.3	NI	NI	9.0	NI	21.4
153	1139	12.3	8.0	450	22.3	6.0	18.2
154	1001	8.0	5.0	441	17.0	4.6	21.6
155	520	1.8	NI	NI	7.8	NI	16.9
156	1323	2.5	NI	NI	8.3	NI	17.8
157	628	9.5	8.0	540	10.8	6.1	21.0
158	1032	8.3	5.0	436	14.8	5.8	20.1
159	615	7.8	6.0	403	11.5	4.3	16.1
160	1383	6.3	2.0	247	16.3	2.2	22.4
161	957	7.3	5.0	310	9.3	3.9	21.7
162	1077	1.3	NI	NI	9.8	NI	20.2
163	703	7.0	5.0	434	15.5	4.3	18.3
164	1152	10.0	5.5	353	18.3	6.1	17.0
165	115	.3	NI	NI	2.8	NI	18.6
166	433	1.3	NI	NI	8.8	NI	19.5
167	1108	3.5	NI	NI	9.5	NI	18.2
168	513	10.8	9.0	394	14.8	5.5	16.4
169	1063	2.8	NI	NI	6.8	NI	21.2
170	454	6.5	5.5	457	15.8	4.1	17.1
171	101	.0	.0	0	2.3	.0	.0
172	819	1.8	NI	NI	6.3	NI	18.3
173	358	8.3	7.0	413	12.5	4.1	16.9
174	1025	3.8	.0	276	20.3	3.2	16.1
175	1273	5.8	2.5	327	20.3	3.2	15.3
177	980	8.0	5.0	357	8.8	4.5	18.1

FIGURE 2.10.2.1. UTCS/BPS END OF DAY REPORT (CONT)

END OF DAY REPORT

INITIAL TIME 0715 DATE MAR 18 74 TIME 0953 REPORT NO 1

	LINK	VOLUME VEHICLES	TRAV.TIME VEH-HRS	DELAY HRS	STOPS VEH	OCCUPANCY PERCENT	QUEUE VEH/CYCLE	SPEED MPH
	178	688	1.3	NI	NI	13.5	NI	17.6
	179	913	3.0	NI	NI	5.5	NI	20.6
	180	1184	2.8	NI	NI	6.0	NI	22.3
	181	1003	4.0	NI	NI	9.3	NI	19.3
	183	1088	8.0	5.0	522	8.0	5.0	21.5
	184	739	4.0	2.5	217	11.5	2.3	19.3
	185	1206	9.5	5.0	470	14.0	6.2	18.9
	186	986	7.8	4.5	461	13.8	5.6	19.6
	187	1090	7.0	4.0	577	19.8	5.1	19.1
	188	598	2.8	NI	NI	25.8	NI	12.3
	189	722	4.3	2.5	253	11.5	2.5	24.3
	190	729	8.0	6.0	473	6.0	8.3	19.2
	191	1100	8.5	5.5	534	11.0	5.2	21.5
	192	0	.0	.0	0	.0	.0	.0
TOTAL		113477	645.3	310.0	24474			
AVERAGE			5.4	5.3	421	12.0	4.8	19.3
SECTION 4	193	1072	2.0	NI	NI	8.8	NI	18.1
	194	875	9.5	7.0	579	12.8	5.3	19.7
	195	394	5.0	4.5	304	6.8	2.6	28.1
	196	72	.0	NI	NI	.3	NI	21.0
	197	1388	3.8	.0	261	19.5	5.8	24.8
	198	1414	13.3	9.5	640	24.0	4.1	24.0
	199	502	1.0	.0	326	4.8	3.8	29.6
	200	390	.5	NI	NI	2.0	NI	22.1
	201	565	9.0	7.5	377	6.0	4.9	24.0
	202	1971	3.5	NI	NI	12.0	NI	24.1
	203	1193	4.3	2.5	278	12.8	2.9	23.9
	204	461	1.5	NI	NI	2.5	NI	22.4
	205	664	1.3	NI	NI	3.3	NI	26.1
	206	2049	5.8	NI	NI	8.3	NI	30.2
	207	483	3.3	2.0	69	2.8	2.7	24.7
	208	1730	4.8	2.5	287	9.5	2.4	30.0
	209	311	10.3	9.5	625	3.3	6.3	22.4
	210	848	5.5	3.0	308	8.5	3.7	21.0
	211	909	4.0	NI	NI	6.5	NI	19.2
	212	672	7.5	6.0	354	6.0	4.1	27.9
	213	1987	4.8	NI	NI	7.5	NI	30.5
	214	1824	7.3	3.0	230	8.8	3.1	29.2
	215	751	7.0	5.5	430	8.8	3.2	31.5
	216	1453	12.0	7.5	451	18.3	6.0	21.9
	217	1586	11.0	7.0	440	18.0	6.1	26.4
	218	773	6.5	5.0	332	5.8	3.9	32.0

FIGURE 2.10.2.1. UTCS/BPS END OF DAY REPORT (CONT)

END OF DAY REPORT

DATE MAR 18 74 TIME 0953

INITIAL TIME 0715 REPORT NO 1

	LINK	VOLUME VEHICLES	TRAV.TIME VEH-HRS	DELAY HRS	STOPS VEH	OCCUPANCY PERCENT	QUEUE VEH/CYCLE	SPEED MPH
	219	706	2.0	NI	NI	6.3	NI	20.3
	220	677	1.8	NI	NI	4.5	NI	21.4
	221	1221	1.3	NI	NI	11.3	NI	18.3
	222	1767	2.0	NI	NI	15.0	NI	17.7
	223	795	3.0	NI	NI	6.3	NI	18.8
	224	849	7.5	5.0	437	9.0	5.1	22.2
	225	1086	3.8	NI	NI	6.3	NI	20.8
	226	703	9.5	7.5	451	6.0	5.5	22.2
	227	1095	3.8	NI	NI	6.8	NI	23.9
	228	1356	1.3	NI	NI	16.3	NI	20.0
	229	613	2.3	NI	NI	12.3	NI	13.3
	230	686	2.0	NI	NI	9.8	NI	17.4
	231	1965	6.8	NI	NI	22.0	NI	21.9
	232	1746	7.5	NI	NI	25.5	NI	17.3
	233	656	1.8	NI	NI	4.8	NI	19.9
	234	1890	4.3	NI	NI	10.0	NI	24.4
	235	656	.8	NI	NI	7.8	NI	15.4
	236	980	7.8	5.0	438	14.0	4.6	24.1
	237	1741	10.8	5.0	345	14.8	5.2	20.4
	238	647	1.3	NI	NI	2.8	NI	26.5
	239	435	1.3	.5	56	2.3	.8	23.0
	240	1157	6.5	3.5	325	10.5	4.4	26.3
	241	900	4.0	2.5	242	13.5	3.1	22.0
	242	1501	3.0	NI	NI	17.5	NI	22.1
	243	355	2.0	NI	NI	7.3	NI	13.8
	244	1480	4.0	NI	NI	13.3	NI	19.9
	245	916	1.8	NI	NI	4.8	NI	22.7
	246	967	13.5	10.5	643	19.8	4.4	21.6
	247	1587	13.3	8.5	473	19.5	5.5	22.5
	248	980	2.5	1.0	160	8.0	1.7	24.8
	249	559	8.0	7.0	627	14.0	5.2	18.4
	250	1327	6.0	3.5	520	21.3	4.2	20.7
	251	1325	3.0	NI	NI	18.8	NI	19.1
	252	1398	8.5	4.5	371	14.3	5.0	22.7
	253	0	.0	.0	0	.0	.0	.0
TOTAL		63059	302.0	146.0	11379			
AVERAGE			5.0	4.8	379	10.0	4.2	22.7
SECTION 5	254	358	1.0	NI	NI	1.5	NI	26.8
	255	656	1.5	NI	NI	2.5	NI	29.0
	256	531	2.3	NI	NI	4.0	NI	17.6
	257	533	.8	NI	NI	2.8	NI	22.8
	258	1496	7.0	NI	NI	14.5	NI	21.5

FIGURE 2.10.2.1. UTCS/BPS END OF DAY REPORT (CONT)

END OF DAY REPORT

DATE MAR 18 74 TIME 0953

INITIAL TIME 0715 REPORT NO 1

LINK	VOLUME VEHICLES	TRAV.TIME VEH-HRS	DELAY HRS	STOPS VEH	OCCUPANCY PERCENT	QUEUE VEH/CYCLE	SPEED MPH
259	0	.0	NI	NI	.0	NI	.0
260	894	3.8	NI	NI	4.8	NI	24.2
261	1110	5.3	NI	NI	18.5	NI	17.4
262	1184	4.8	NI	NI	12.3	NI	18.3
263	1177	4.0	NI	NI	6.3	NI	21.4
264	1537	1.5	NI	NI	18.3	NI	19.1
265	691	2.8	NI	NI	4.0	NI	24.5
266	1021	5.5	NI	NI	13.5	NI	18.8
267	1054	3.5	NI	NI	4.0	NI	29.9
269	243	.8	NI	NI	1.0	NI	29.2
TOTAL	12485	44.3	.0	0			
AVERAGE		3.2	.0	0	7.0	.0	22.9

FIGURE 2.10.2.1. UTCS/BPS END OF DAY REPORT (CONT)

SYSTEM PERFORMANCE	VOLUME TOTAL	TRAV.TIME TOTAL	DELAY TOTAL	STOPS TOTAL	OCCUPANCY PERCENT	QUEUE AVERAGE	SPEED AVERAGE
	234909	1243.3	595.5	48143	10.5	4.4	20.8

FIGURE 2.10.2.1. UTCS/BPS END OF DAY REPORT (CONT)

BPS END OF DAY ZONE SUMMARY

SECT	ZONE	15-MIN. MODE OF OPERATION FAIL	REL	ACT	PRE	INH	STOP BUS VOL.	THRU BUS VOL.	ELIGIBLE STOP BUSES	ELIGIBLE THRU BUSES	EXTNS GRANTED	HELPED STOP BUSES	HELPED THRU BUSES	PSG. MIN. SAVED
1	5	0	0	2	0	9	0	26	0	4	3	0	2	36
	6	0	0	2	0	9	0	3	0	0	0	0	0	0
	7	0	0	2	0	9	0	16	0	0	3	0	0	0
	SECTION TOTALS						0	45	0	4	6	0	2	36
2	1	0	7	0	0	4	0	9	0	0	0	0	0	0
	2	7	0	0	0	4	0	19	0	1	1	0	2	40
	3	0	0	0	0	11	0	19	0	0	0	0	0	0
	4	0	0	0	0	11	2	15	0	0	0	0	0	0
	67	0	0	2	0	9	13	50	0	2	3	0	2	54
	68	0	0	2	0	9	6	28	1	0	3	0	0	0
	69	0	0	4	0	7	0	36	0	4	3	0	0	0
	70	0	0	4	0	7	0	18	0	1	1	0	0	0
	71	0	0	11	0	0	0	23	0	12	21	0	6	54
	72	0	0	11	0	0	2	16	1	5	21	2	2	60
	SECTION TOTALS						23	233	2	25	53	2	12	208
3	15	4	0	2	0	5	0	47	0	7	6	0	2	83
	16	0	4	2	0	5	9	23	0	0	0	0	0	0
	17	0	4	2	0	5	2	16	0	1	1	0	1	21
	18	0	0	0	0	11	0	54	0	2	2	0	2	46
	19	0	0	0	0	11	0	0	0	0	2	0	0	0
	22	0	7	0	0	4	0	19	0	0	2	0	0	0
	23	0	7	0	0	4	0	16	0	1	2	0	1	29
	24	7	0	0	0	4	0	40	0	5	3	0	2	29
	25	0	6	0	0	5	14	27	0	0	0	0	0	0
	26	0	6	0	0	5	0	0	0	0	0	0	0	0
	27	6	0	0	0	5	49	0	0	0	0	0	0	0
	28	0	11	0	0	0	0	0	0	0	0	0	0	0
	29	0	11	0	0	0	0	0	0	0	0	0	0	0
	30	0	0	2	0	9	0	56	0	8	6	0	3	56
	31	0	0	2	0	9	0	24	0	6	6	0	3	106
	32	3	0	2	0	6	20	0	0	0	0	0	0	0
	33	0	3	2	0	6	0	0	0	0	0	0	0	0
	34	0	0	2	0	9	0	0	0	0	0	0	0	0
	35	0	0	2	0	9	0	19	0	0	0	0	0	0
	36	0	0	2	0	9	0	12	0	2	2	0	0	0
	37	7	0	1	0	3	0	23	0	6	6	0	0	0
	38	0	7	1	0	3	0	0	0	0	6	0	0	0
	39	0	7	1	0	3	0	19	0	2	2	0	0	0
	40	6	0	0	0	5	6	29	2	3	7	1	3	120
	41	0	6	0	0	5	0	2	0	0	0	0	0	0
	42	0	6	0	0	5	7	20	0	1	5	0	0	0
	43	8	0	3	0	0	5	0	3	0	2	0	0	0

FIGURE 2.10.2.1. UTCS/BPS END OF DAY REPORT (CONT)

BPS END OF DAY ZONE SUMMARY

SECT	ZONE	15-MIN. MODE OF OPERATION FAIL	REL	ACT	PRE	INH	STOP BUS VOL.	THRU BUS VOL.	ELIGIBLE STOP BUSES	ELIGIBLE THRU BUSES	EXTNS GRANTED	HELPED STOP BUSES	HELPED THRU BUSES	PSG. MIN. SAVED
	44	0	0	4	0	7	0	42	0	8	7	0	3	40
	45	0	0	8	0	3	5	19	1	8	22	2	4	63
	46	0	0	8	0	3	0	49	0	21	22	0	6	150
	47	11	0	0	0	0	0	0	0	0	0	0	0	0
	48	0	0	8	0	3	0	49	0	18	16	0	7	129
	49	8	0	0	0	3	0	31	0	0	0	0	0	0
	50	0	8	0	0	3	0	9	0	0	0	0	0	0
	51	0	8	0	0	3	11	24	0	0	0	0	0	0
	52	6	2	0	0	3	2	19	0	0	0	0	0	0
	53	0	4	0	0	7	0	15	0	0	0	0	0	0
	54	2	2	0	0	7	0	0	0	0	0	0	0	0
	55	7	0	1	0	3	20	0	0	0	0	0	0	0
	56	6	1	1	0	3	34	0	0	0	0	0	0	0
	57	0	7	1	0	3	0	0	0	0	0	0	0	0
	58	0	0	6	0	5	57	0	0	0	0	0	0	0
	59	0	7	3	0	1	2	5	1	3	5	0	3	65
	60	7	0	3	0	1	0	0	0	0	5	0	0	0
	61	0	7	3	0	1	0	31	0	4	17	0	3	92
	62	3	4	3	0	1	2	9	1	0	0	0	0	0
	63	0	7	3	0	1	11	39	4	11	16	0	2	44
	64	7	0	3	0	1	4	9	0	1	0	0	0	0
	SECTION TOTALS						260	796	12	118	170	3	45	1073
4	8	0	0	5	0	6	0	0	0	0	0	0	0	0
	9	0	0	5	0	6	0	0	0	0	0	0	0	0
	10	9	0	0	0	2	0	1	0	0	0	0	0	0
	11	0	9	0	0	2	0	4	0	0	0	0	0	0
	12	0	0	11	0	0	0	3	0	0	0	0	0	0
	13	0	0	11	0	0	0	22	0	10	7	0	3	87
	14	0	0	3	0	8	2	25	0	0	0	0	0	0
	20	0	0	6	0	5	0	2	0	0	0	0	0	0
	21	0	0	6	0	5	0	32	0	5	4	0	3	34
	65	0	0	0	0	11	22	22	0	0	0	0	0	0
	66	0	0	0	0	11	6	5	0	0	0	0	0	0
	SECTION TOTALS						30	116	0	15	11	0	6	121
	SYSTEM TOTALS						313	1190	14	162	240	5	65	1438

FIGURE 2.10.2.1. UTCS/BPS END OF DAY REPORT (CONT)

DELETED

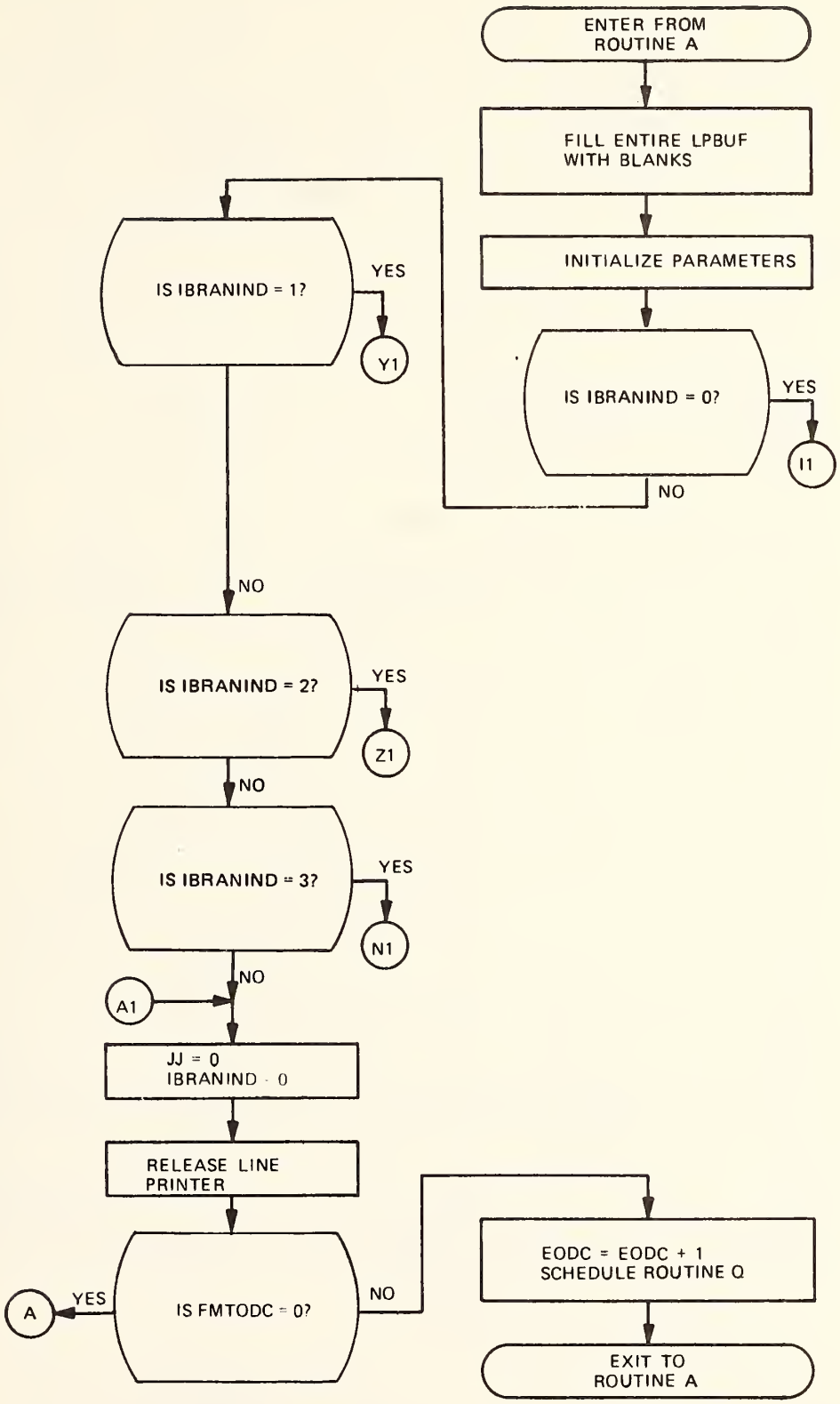


FIGURE 2.10.5.1. ROUTINE I FLOW CHART

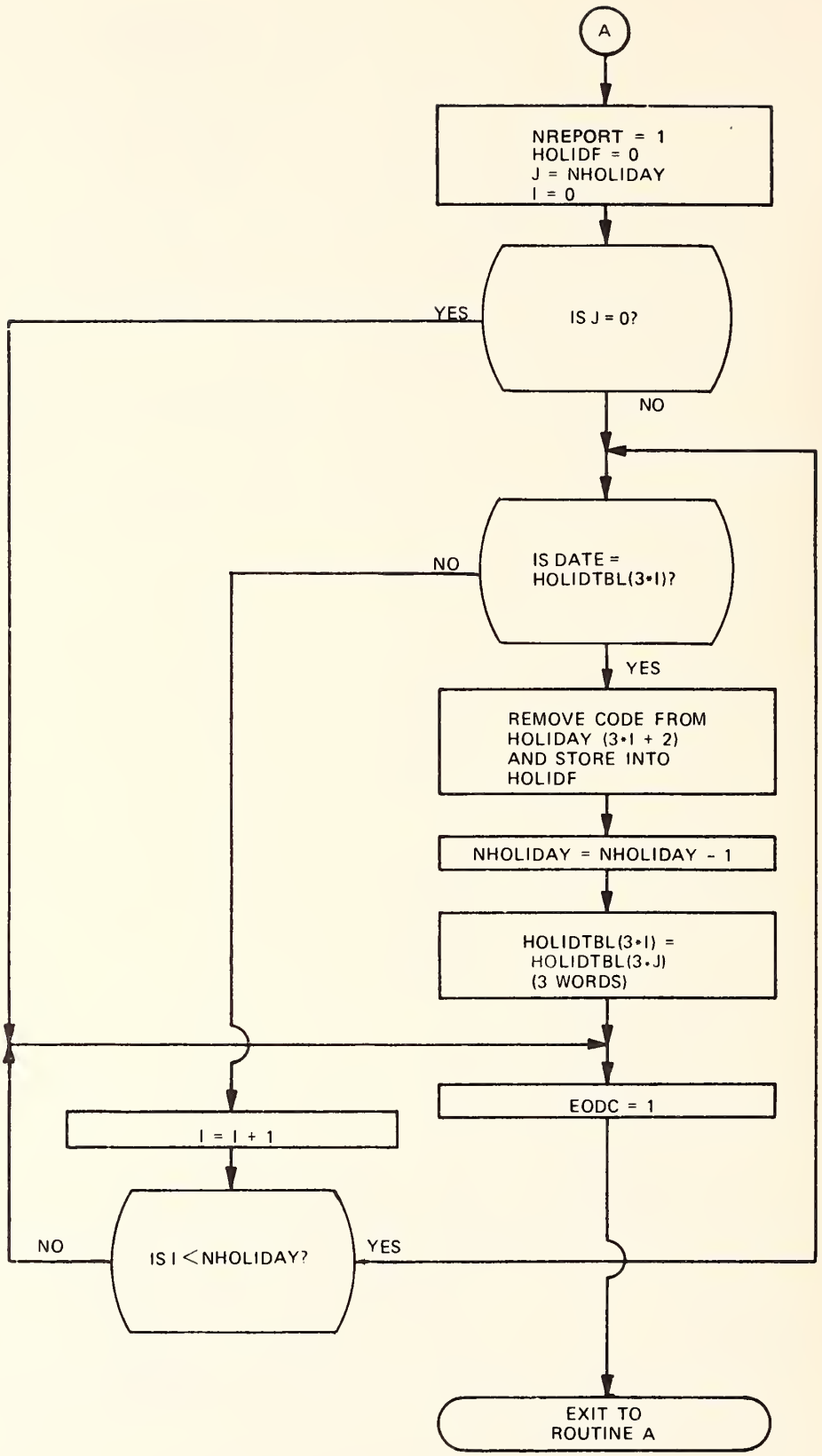


FIGURE 2.10.5.1. ROUTINE I FLOW CHART

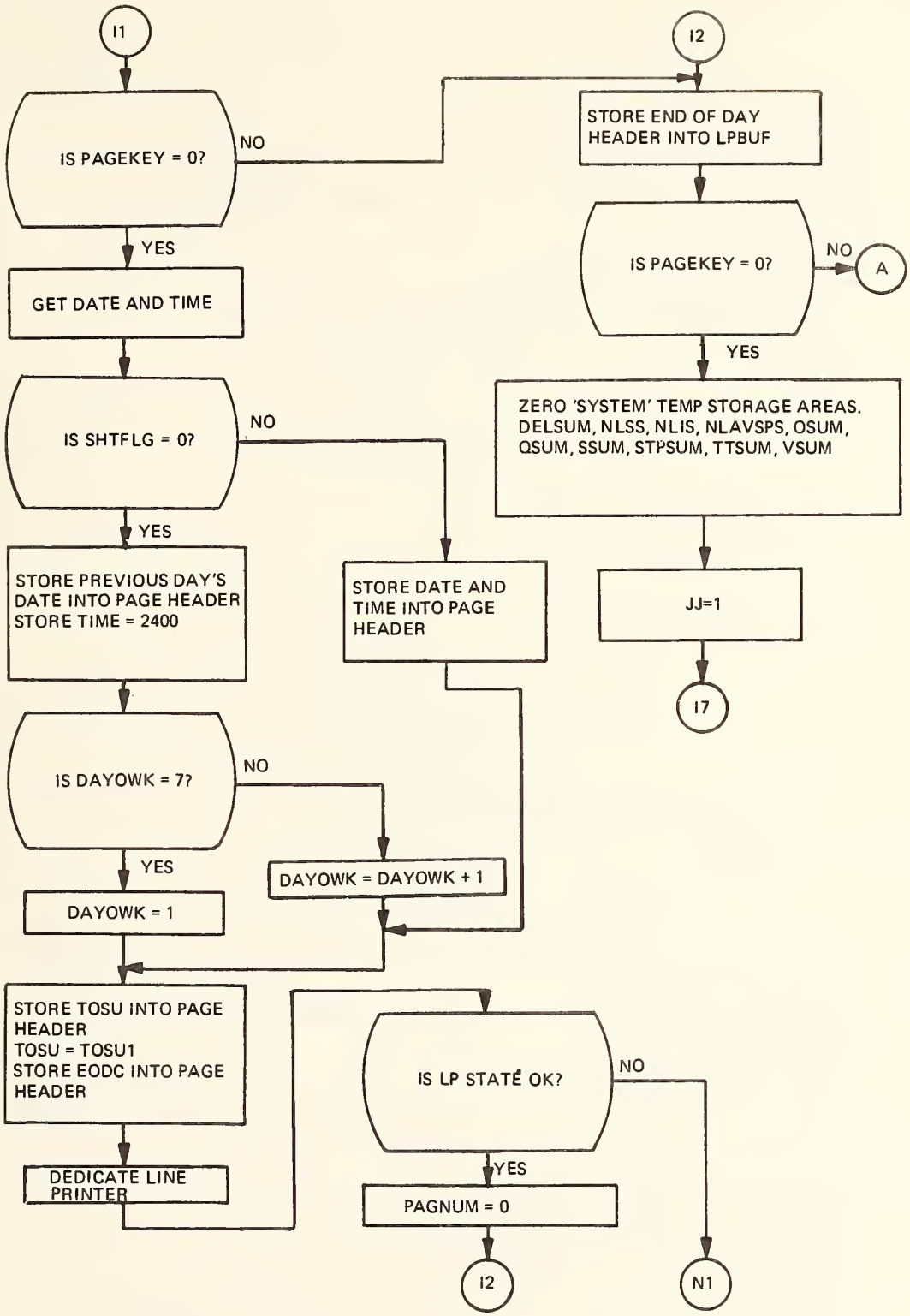


FIGURE 2.10.5.2. ROUTINE I FLOW CHART

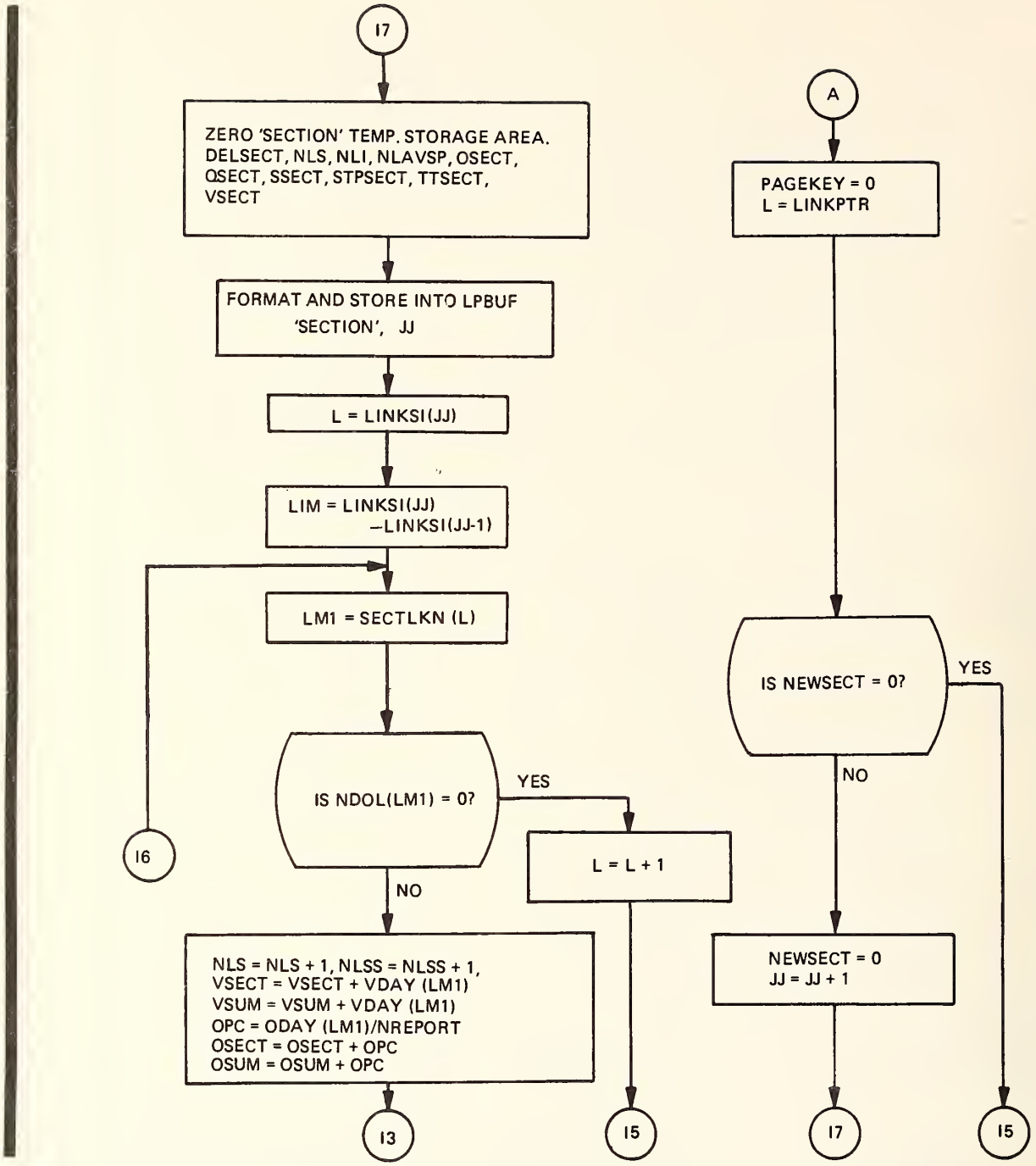


FIGURE 2.10.5.2. ROUTINE I FLOW CHART

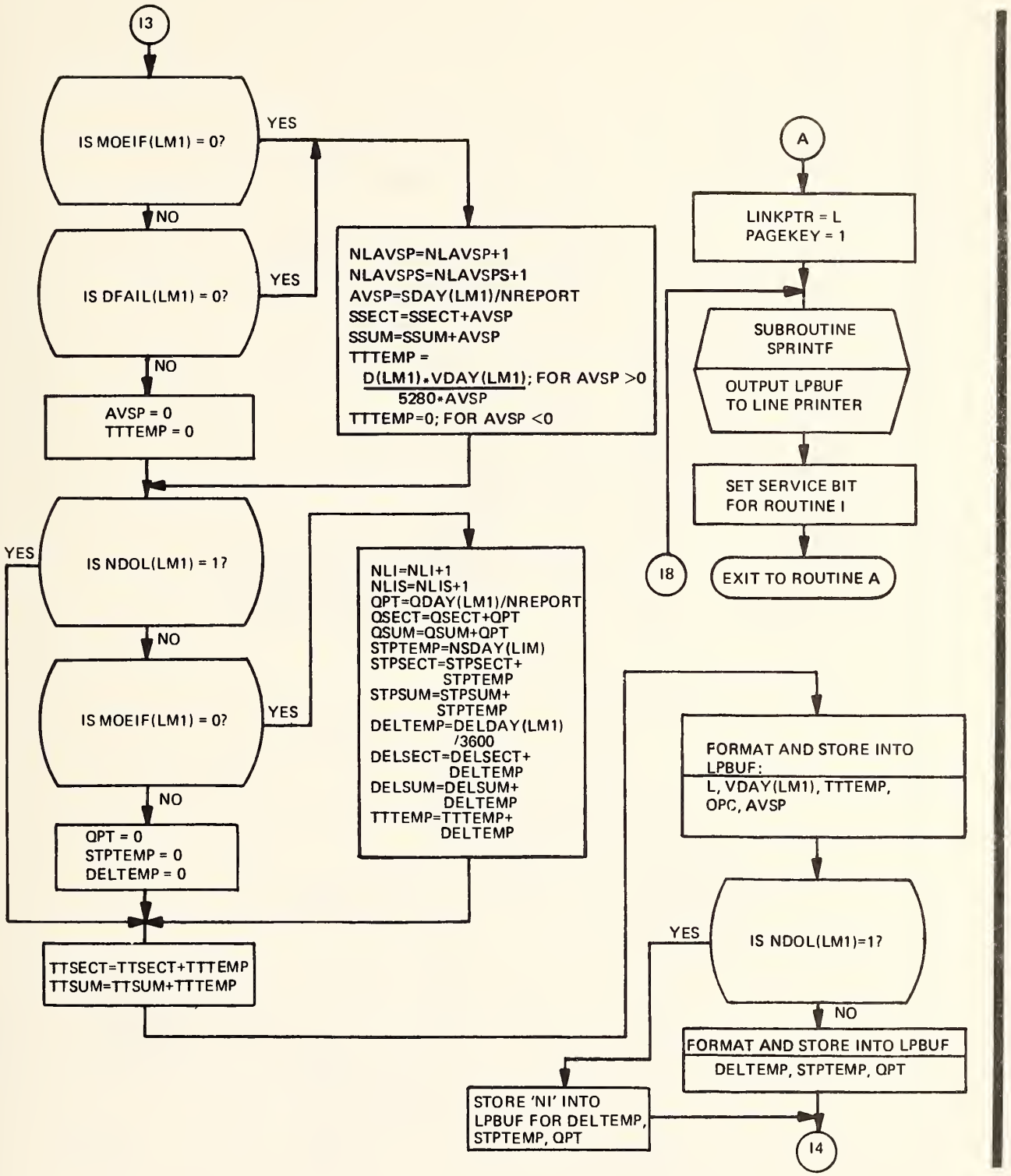


FIGURE 2.10.5.3. ROUTINE I FLOW CHART

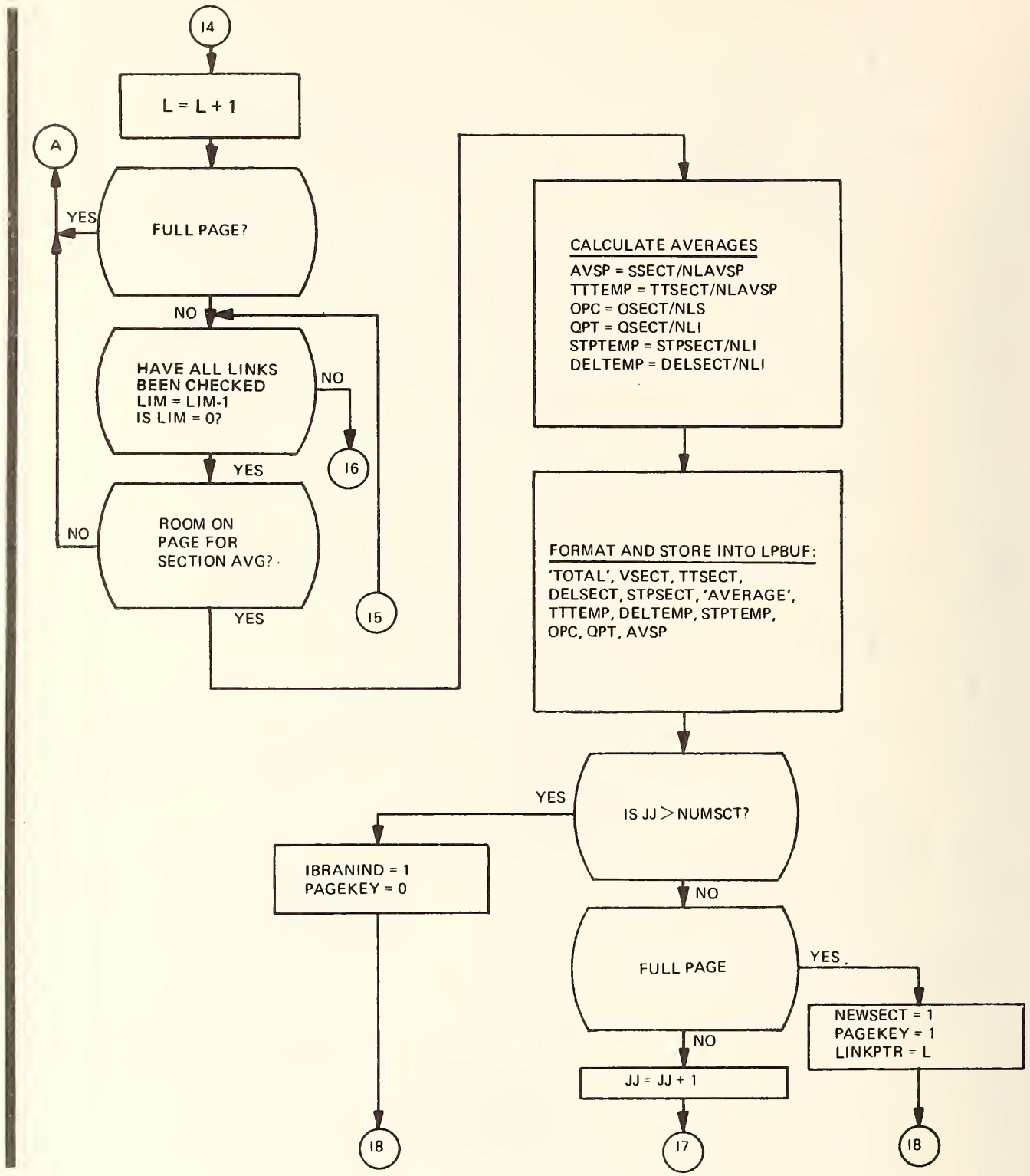


FIGURE 2.10.5.3. ROUTINE I FLOW CHART

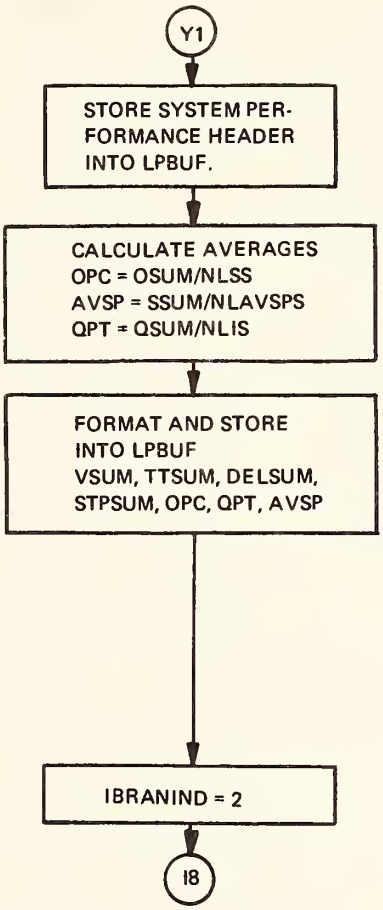


FIGURE 2.10.5.4. ROUTINE I FLOW CHART

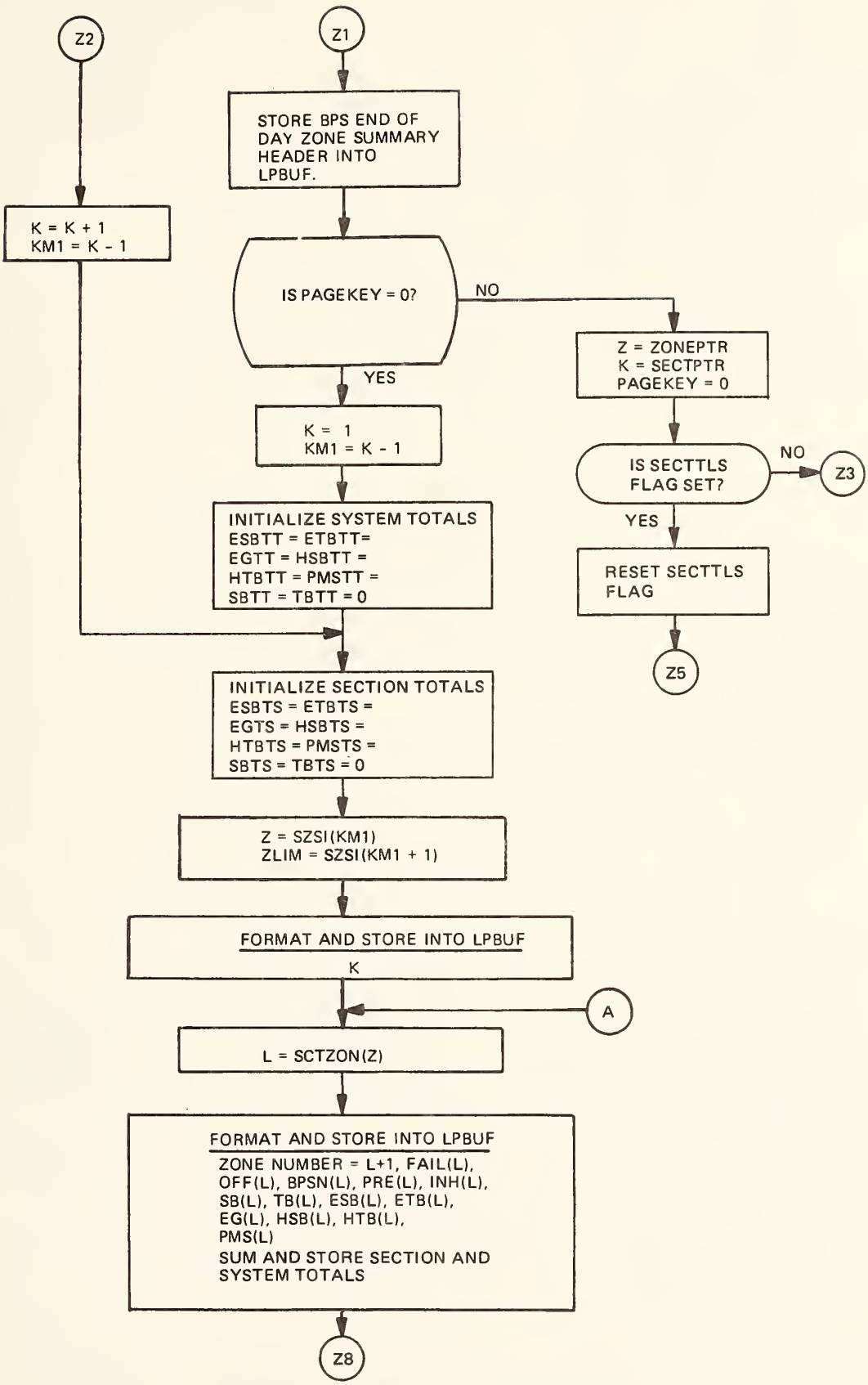


FIGURE 2.10.5.5. ROUTINE I FLOW CHART

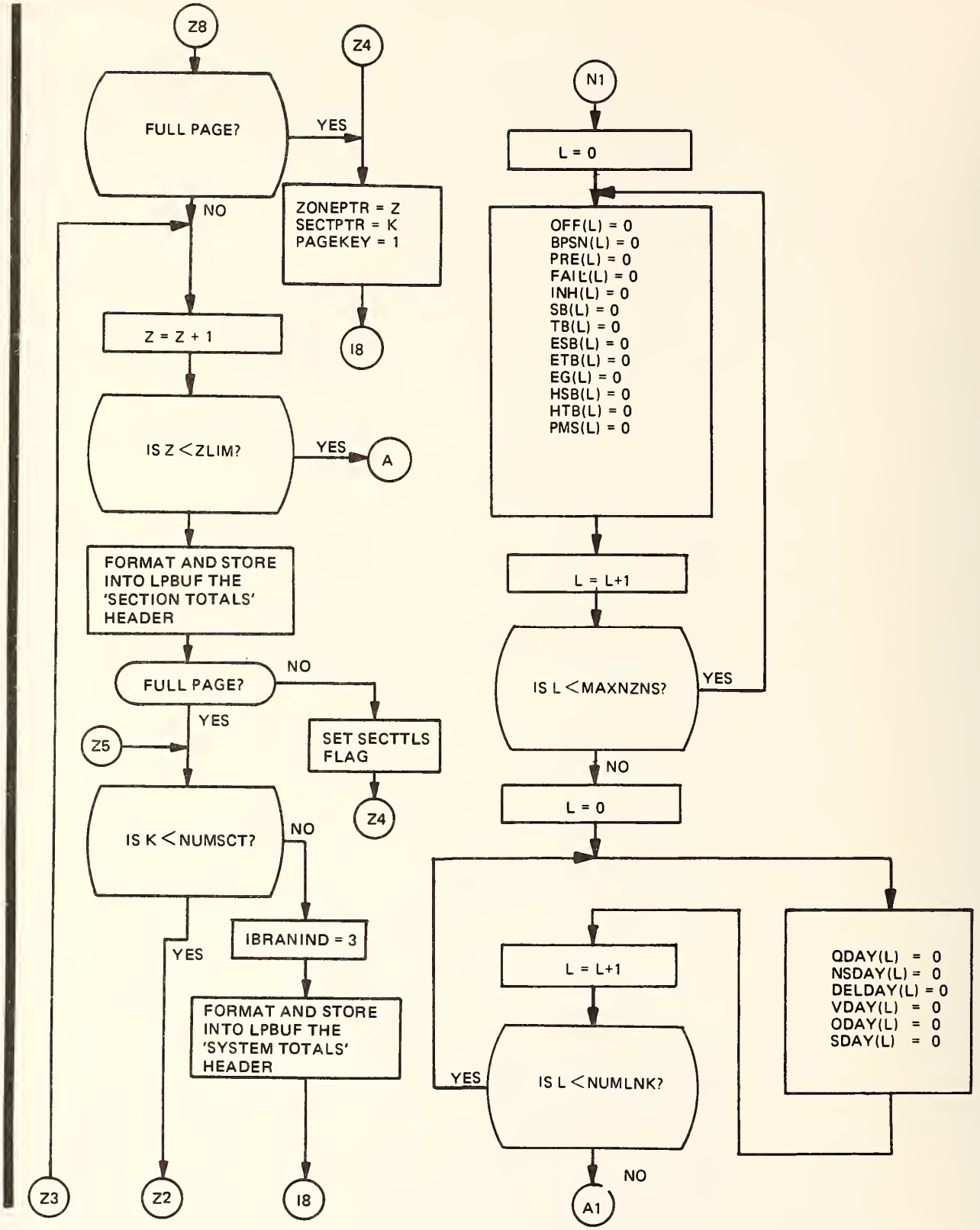


FIGURE 2.10.5.5. ROUTINE I FLOW CHART

2.11 Routine J (Map Control and Data Formatting) Specification

2.11.1 Purpose

The Map Control and Data Formatting Routine controls the indicator arrows on the illuminated street map display. The indicator arrows are of two types, those which provide controller status information, and those providing data on link parameters, including detector status information.

The Map Display consists of two separate displays. The Controller Display comprises the intersection arrows which are illuminated in green or red. The Surveillance Display comprises the link arrows which parallel their corresponding streets and which are illuminated in yellow. A third display, the Legend Display, identifies the display modes and indicates any flow data threshold being used.

The 397 Map Display control signals in the present system are included among the 32 per second MUX inputs and outputs (Figure 2.11.2.1). Each map output word, which is sent to the MUX along with a MUX format word, contains one nine-bit address and two signal state bits (Figure 2.11.2.1). Output words containing map switches and display controls (i.e. the 24 legend on/off switches, the 16 bits comprising the four BCD threshold digits, the enable/disable communication discrete, and the enable/disable traffic signal lamps switch) use only one of the two state bits. Most of those containing intersection of link arrow lamp controls use both state bits. However, some intersection state bits refer to non-existent controllers in order to maintain a consecutive numbering scheme: only 112 of the 124 intersection state bits provided in the 62 output words are used. On the other hand, all but one of the 254 state bits in the 127 link arrow output words are used.

The purpose of Routine J is to insert the appropriate state bits in the Map Signal Output Array for the requested Controller and Surveillance Displays. Every 1/32 second, the Executive Routine, Routine A, transmits 24 state bits and associated addresses (12 data words) to the map. (The 24 per 1/32 second limitation is due to the 2 signals per millisecond rate at which the map decoding logic can accept signal data.) The Map Signal Output Array (LMAP) comprises 35x12=420 data words, thus providing the capacity for 840 outputs. The entire array is output every 35/32 seconds.

The one-way arrows on 15th and 17th streets are operated directly by radio signals and are independent of Routine J.

In addition to the nine-bit address and the two signal state bits, each data word transmitted to the map contains a one-bit strobe signal. The value of this strobe signal is "1" for the odd-numbered sequential data words (i.e. first, third, ...) in each 12-word group transmitted during a 1/32 second time slot, and "0" for the even-numbered data words (i.e., second, fourth, ...). Thus, whenever a new word is transmitted, the strobe signal state changes. This state change informs the map decoding logic that a new word is ready to be processed.

In processing a data word, the map decoding logic operates on the nine-bit address to determine the destination of the two state bits. It then routes the state bits to their respective switches or lamps and waits for the next data word.

If the nine-bit address is invalid (i.e., it does not reference an existing signal or signal pair), it will be ignored by the decoding logic. If the address refers to one signal, rather than to a signal pair, the decoding logic will route the leftmost state bit in the data word to that signal.

2.11.2 Method

The status of the A-phase at each controlled intersection, whether red or green, is transmitted directly to the map and is always available even when the computer is not in operation. It will be displayed at all times except when deliberately turned off or when Controller Status or Controller Failed displays are requested.

Controller Status can be requested in three modes: Traffic Control, C.I.C., and B.P.S. In the Traffic Control mode, green arrows are displayed at all intersections under computer control, red arrows for those in standby. In the C.I.C. mode, green arrows are displayed for the intersections which have been activated for Critical Intersection Control, red for all others. In the B.P.S. mode, green arrows represent intersections activated for Bus Priority Operation, red arrows for all others.

Controllers Failed are called for in the Traffic Control mode only. Here all intersections where the controls have failed display red arrows, all others green arrows.

Surveillance Equipment Failed is called for in the Traffic Control or B.P.S. modes. In the Traffic Control mode, any link having a vehicle detector or communication failure will be illuminated in orange or yellow while in the B.P.S. mode,,links illuminated in orange or yellow represent bus detector or communication failure(s) on these links.

Link flow data is selected by type and threshold value. For the Traffic Control mode, the following types of flow data (MOE) can be selected:

Occupancy

Volume

Queue

Stops

Speed

Delay

Travel Time

For the B.P.S. mode, the following MOEs can be shown:

Passenger gain

Buses Helped.

In any case, only those links are illuminated (yellow or orange) where the MOE value exceeds the selected threshold for occupancy, volume, queues, stops, and delays, or is less than the selected threshold for speed.

The Executive Routine (A) schedules Routine J every six seconds for a periodic updating of the Controller and Surveillance Displays. Routine J is also scheduled by the Manual Control Panel Routine (M) whenever the operator enters a valid Map Display request. Note that up to 35/32 seconds may pass until all map switches and lamps are set to the states included in the updated Map Signal Output Array.

Upon entry, Routine J first examines the Controller Display Code to determine which Controller Display mode is to be presented (0 for A-Phase green; 1 for Controllers Off; 2 for Controllers Status, 3 for Controllers Failed; 4 for CIC Status; 5 for BPS Status). It then branches to the appropriate program segment to format the applicable Legend Display; to set the enable/disable lamp switches as required; and to determine the red/green state for each intersection arrow lamp according to the selected Controller Display mode. After preparing the Controller Display, Routine J examines the Surveillance Display Code (0 for Surveillance Display Off; 1 for Traffic Control System Equipment Failed; 2 for BPS Equipment Failed; 3 for Flow Data). It branches to the appropriate program segment to format the applicable Legend Display and to determine the on/off state for each link arrow lamp according to the selected Surveillance Display Mode. Note that the Controller and Surveillance Display Codes remain intact until the operator requests a mode change using the Control Panel.

Routine J enters the signal states for the Controller Display and for the Legend Display directly in the Map Signal Output Array. However, to avoid momentary "black-outs" of the Surveillance Display due to the fact that J turns off all link arrows prior to determining their on/off states, the routine first generates the Surveillance Display in a temporary buffer and then moves that array into the Map Signal Output Array.

When Routine J completes the updating of both the Controller Display and the Surveillance Display, it returns control to the calling routine. During the next 35/32 seconds all the updated switch and lamp states will be output to the map.

The following sections describe three utility subroutines employed in preparing Flow Data Surveillance Displays and data arrays upon which Routine J operates.

2.11.2.1 Subroutine TCSLPP (PAR, MTHLD, B, F, S) Description

The utility subroutine TCSLPP compares a Traffic Control System parameter value for each link with a threshold value, MTHLD. The link parameters are stored in a half-word (S=0) or byte (S=1) array starting at location PAR. If the flag F is zero, a link arrow is illuminated if and only if the corresponding link parameter exceeds the threshold value. If F is non-zero, the arrow is illuminated if and only if the parameter is less than the threshold.

TCSLPP uses subroutine BCDTHD to format MTHLD for BCD presentation in the Legend Display.

2.11.2.2 Subroutine BPSLPP (PAR, MTHLD) Description

The utility subroutine BPSLPP compares a BPS parameter value for each BPS link with a threshold value, MTHLD. The link parameters are stored in a byte array starting at location PAR. The link arrow is illuminated if and only if the corresponding link parameter is less than the threshold value.

BPSLPP uses subroutine BCDTHD to format MTHLD for BCD presentation in the Legend Display.

2.11.2.3 Subroutines BCDTHD Description

The utility subroutine BCDTHD converts the positive binary integer MTHLR ($\leq$9999) to BCD and stores the resulting bit configuration in the Map Signal Output Array.

The binary representations of BCD digits are:

	8-bit	4-bit	2-bit	1-bit
0 =	0	0	0	0
1 =	0	0	0	1
2 =	0	0	1	0
3 =	0	0	1	1
4 =	0	1	0	0
5 =	0	1	0	1
6 =	0	1	1	0
7 =	0	1	1	1
8 =	1	0	0	0
9 =	1	0	0	1

2.11.2.4 Map Signal Output Array (LMAP)

The Map Signal Output Array depicted in Figure 2.11.2.1 comprises 840 words: 420 MUX "order" words interleaved with 420 data words. All 420 MUX order words are identical: Each order word, when presented to the MUX, causes bytes 0, 1 and 2 of the following data word to be transmitted to the three 7950 stored output modules connected to the map; it then causes a one millisecond delay before the next order word is accepted by the MUX.

Each map data word has the following format:

Bit 0 (sign bit) is the alternating strobe signal discussed in Section 1.

Bits 4 and 20 are the two signal state bits.

Bits 7 through 15 are the nine-bit signal pair address.

The strobe signal (bit 0) and the nine-bit address (bits 7-15) in each data word are set to their appropriate values when the program is loaded into the computer and do not change. The state bits are inserted (using the logical operation instructions of the computer) by Routine J as a function of the display being presented.

Figure 2.11.2.1 illustrates the Map Signal Output Array organization. The first 48 data words contain signal status (one per data word) for the map controls and Legend Display; only 32 of these data words are used in the present system. The next 116 data words contain the green/red intersection arrow status (two per data word) of the Controller Display; the present system uses 62 words, providing 124 state bits. The next 256 data words contain the on/off link arrow states (two per data word) of the Surveillance Display; 127 of these are used in the present system, providing 254 state bits.

The following algorithms can be used to reference state bits in the LMAP array. These algorithms compute the byte address, relative to the first byte of the array, of the byte containing the signal state. The signal state itself is in bit position 4 of the byte (i.e. the fifth bit from the left end of the byte).

The Enable/Inhibit Communications control bit is in byte 4 of the array.

The Enable/Disable Traffic Signals control bit is in byte 8 of the array.

The Legend i On/Off control bit is in byte $8i + 12$ for $i=1, \ldots, 14$.

The jth-bit of threshold digit i is in byte $32i + 8k + 100$, where $k = 0, 1, 2, 3$ for $j = 8, 4, 2, 1$, and $i = 1, 2, 3, 4$.

The Controller i green/red control is in byte $8 [(i-1)/2] + k + 388$, where $[x]$ denotes the integer part of x, where $k = 0$ for i odd and $k = 2$ for i even, and where $i = 1, \ldots, 112$ for the present system.

The Link Arrow i On/Off control is in byte $8 [(i-1)/2] + k + 1316$, where $[x]$ denotes the integer part of x, where $k = 0$ for i odd and $k = 2$ for i even, and where $i = 1, \ldots, 253$ for the present system. When Routine J determines that Link Arrow is to be on, it clears bit 4 of byte i-1 of the internal byte array, LNKARW, each byte of which is set to X '00' at every entry of Routine J. After the Surveillance Display has been completely formatted, J replaces the state bit for Link Arrow i in the LMAP array by the state bit from byte i-1 of the LNKARW array, for $i=1, \ldots, 253$.

2.11.2.5 Link Arrow Arrays

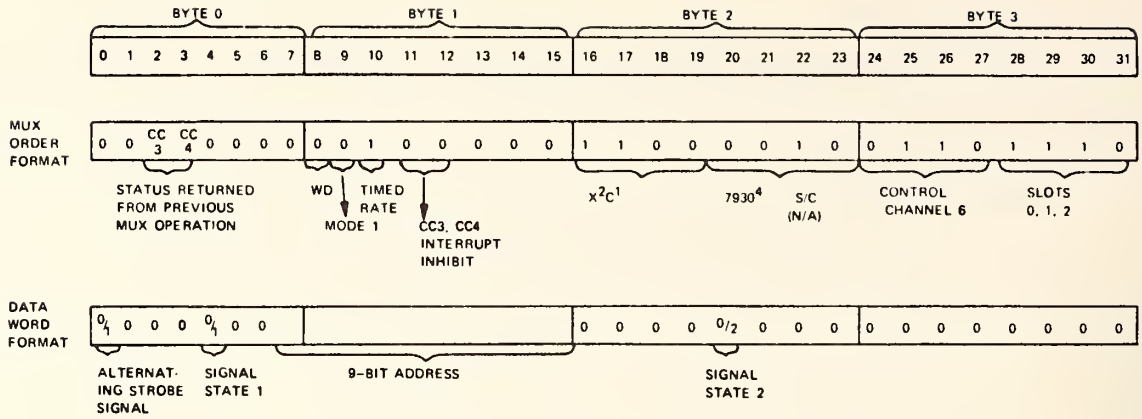
Four arrays provide the necessary cross-references between vehicle detector numbers and link arrow numbers (DETDSP); between BPS detector numbers and link arrow numbers (BDTDSP); between link numbers and link arrow numbers (LNKDSP); and between BPS link numbers and link arrow numbers (BLNDSP). Each is a byte array whose ith entry is the index of the LNKARW array entry containing the state bit for the ith detector, BPS detector, link, or BPS link, respectively.

2.11.3 Repetition Rate

This routine is entered whenever there is an operator request and at six second intervals for updating of data.

2.11.4 Cross Reference

This routine is scheduled by Routine A and returns to that routine.



	0 1	2 3	
	0 18 15	16 23 24 36	
LMAP	0 0 2 0	C 2 6 E	SSI = 1 (= 0) ENABLES (INHIBITS) COMMUNICATIONS (I.E. CAUSES (INHIBITS) A – O GREEN DISPLAY)
LMAP +1	B ENB/ INHBT COMM	0 0 0 0	
LMAP +2	0 0 2 0	C 2 6 E	SSI = 1 (= 0) TURNS ON (OFF) ALL INTERSECTION ARROWS
LMAP +3	0 ENB/DSB TRF SIG'S	0 0 0 0	
LMAP +4	0 0 2 0	C 2 8 E	SSI = 1 (= 0) TURNS ON (OFF) LEGEND 1, "OCCUPANCY"
LMAP +5	B LEGEND 1 ON/ OFF	0 0 0 0	
⋮		⋮	
LMAP +30	0 0 2 0	C 2 6 E	SSI = 1 (= 0) TURNS ON(OFF) LEGEND 14, "CONTROLLERS FAILED"
LMAP +31	0 LEGEND 14 ON/ OFF	0 0 0 0	
LMAP +32	0 0 2 0	C 2 6 E	EACH OF THE 4 THRESHOLD DIGITS IS REPRESENTED IN RCD CODE:
LMAP +33	B BCD DIGIT 1 8-BIT	0 0 0 0	
⋮		⋮	
LMAP +38	0 0 2 0	C 2 6 E	
LMAP +39	0 BCD DIGIT 1 1 - BIT	0 0 0 0	
⋮		⋮	
LMAP +62	0 0 2 0	C 2 8 E	
LMAP +63	0 BCD DIGIT 4 1-BIT	0 0 0 0	
LMAP +64	0 0 2 0	C 2 8 E	
LMAP +65	B 0 0 0 0	0 0 0 0	
⋮		⋮	
LMAP +96	0 0 2 0	C 2 6 E	
LMAP +97	B CTLR 1 GREEN/ RED	0 CTLR 2 GREEN/ RED	SSI = 1 (= 0) TURNS CONTROLLER 1 ARROW GREEN (RED) SS2 = 1 (= 0) TURNS CONTROLLER 2 ARROW GREEN (RED)
⋮		⋮	
LMAP +206	0 0 2 0	C 2 6 E	
LMAP +207	0 CTLR 111 GREEN/ RED	0 CTLR 113 GREEN/ RED	SSI = 1 (= 0) TURNS CONTROLLER 111 ARROW GREEN (RED) SS2 = 1 (= 0) TURNS CONTROLLER 112 ARROW GREEN (RED)
LMAP +208	0 0 2 0	C 2 6 E	
LMAP +209	B 0 0 0 0	0 0 0 0	AVAILABLE FOR EXPANSION TO 232 CONTROLLERS
⋮		⋮	
LMAP +328	0 0 2 0	C 2 6 E	
LMAP +329	B LINK 1 ON/OFF	0 LINK 2 ON/OFF	SSI = 1 (= 0) TURNS LINK ARROW 1 ON (OFF) SS2 = 1 (= 0) TURNS LINK ARROW 2 ON (OFF)
⋮		⋮	
LMAP +680	0 0 2 0	C 2 8 E	
LMAP +581	B LINK 253 ON/OFF	0 0 0 0	SSI = 1 (= 0) TURNS LINK ARROW 253 ON (OFF)
LMAP +582	0 0 2 0	C 2 8 E	
LMAP +583	0 0 0 0	0 0 0 0	AVAILABLE FOR EXPANSION TO 512 LINKS
⋮		⋮	

SEE MAP FOR OTHER LEGENDS

	8- BIT	4- BIT	2- BIT	1- BIT		8- BIT	4- BIT	2- BIT	1- BIT
0 =	0	0	0	0	5 =	0	1	0	1
1 =	0	0	0	1	6 =	0	1	1	0
2 =	0	0	1	0	7 =	0	1	1	1
3 =	0	0	1	1	8 =	1	0	0	0
4 =	0	1	0	0	9 =	1	0	0	1

FIGURE 2.11.2.1. MAP SIGNAL OUTPUT ARRAY

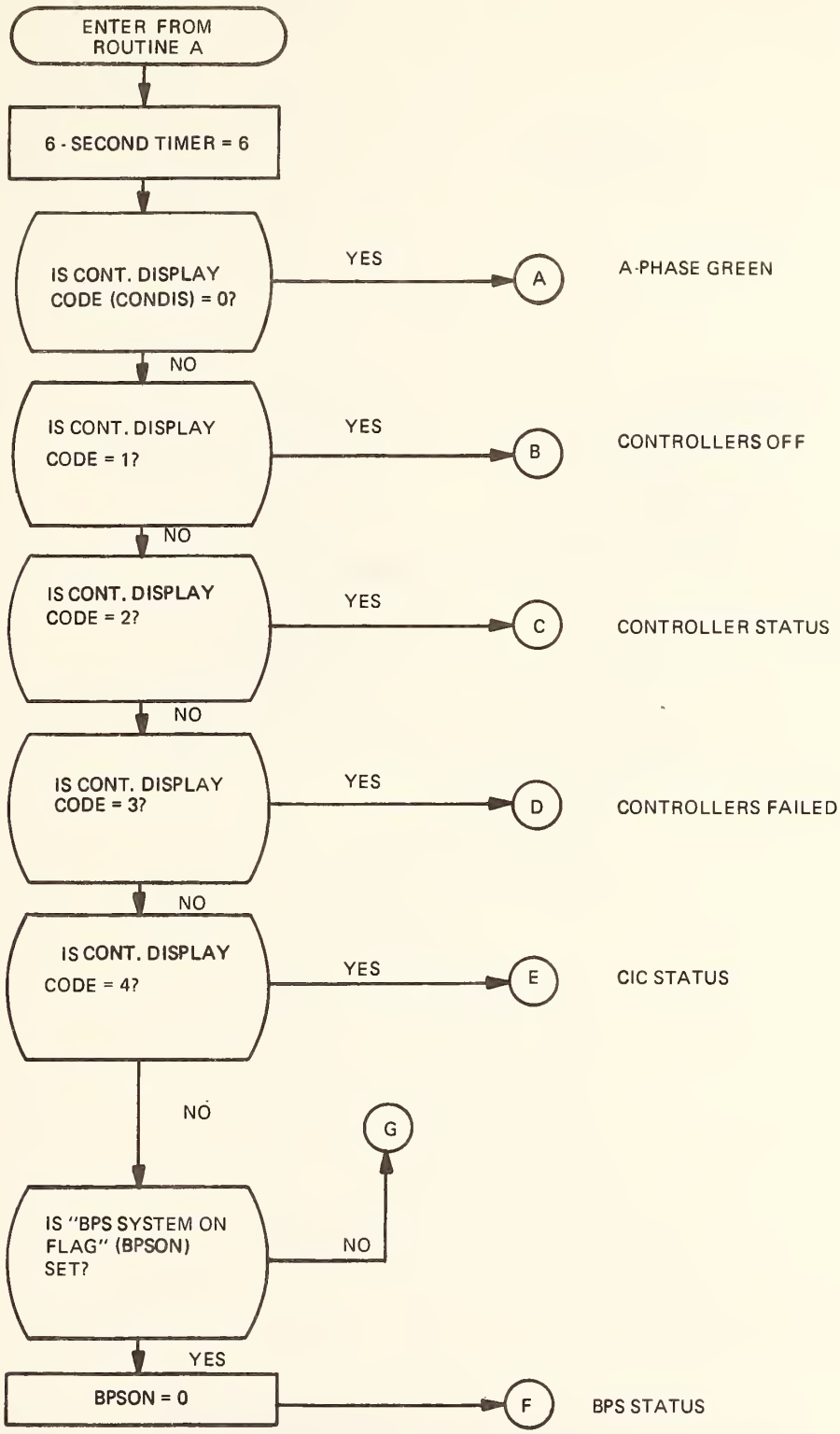


FIGURE 2.11.5.1. ROUTINE J FLOW CHART

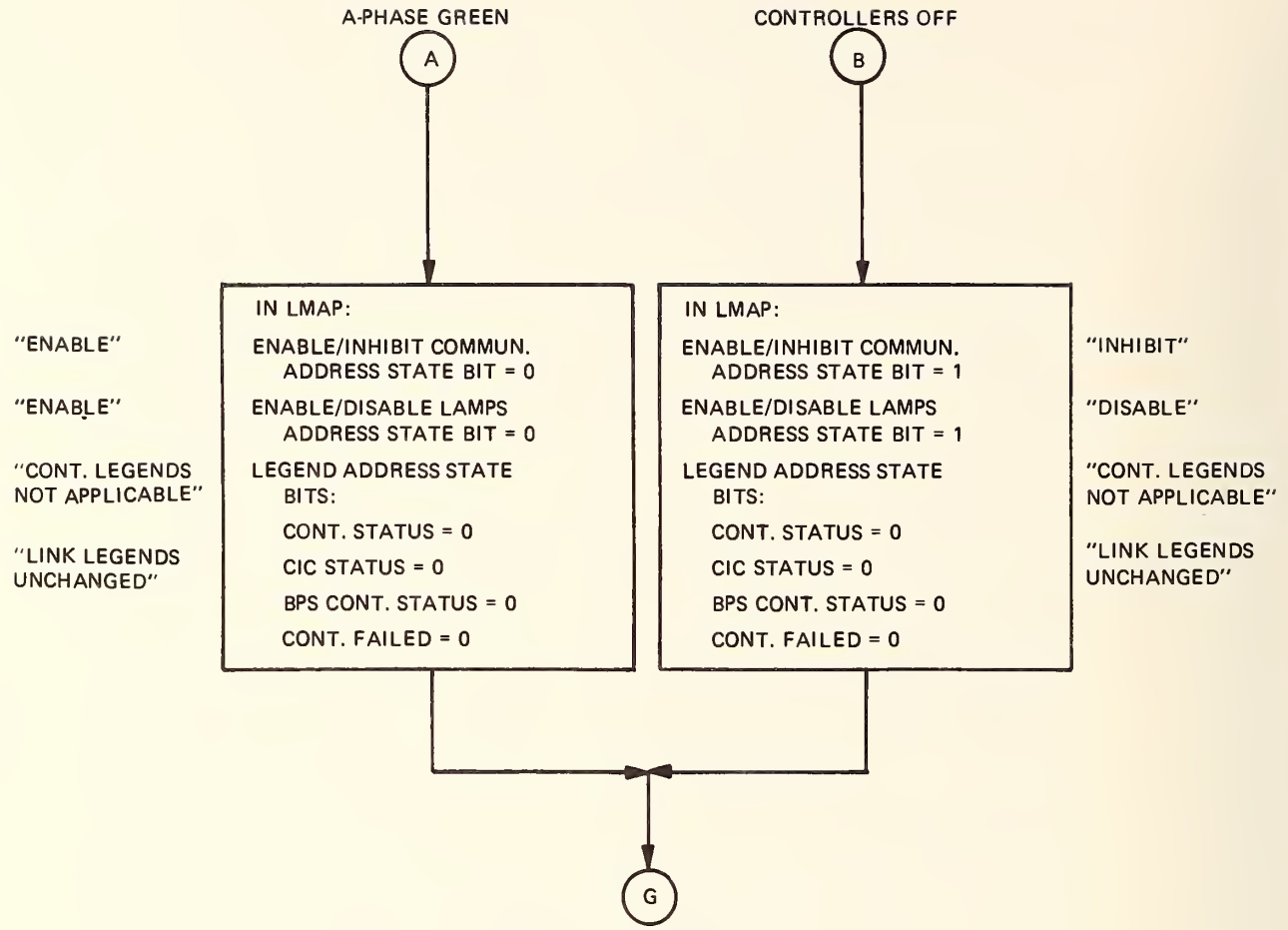


FIGURE 2.11.5.2. ROUTINE J FLOW CHART

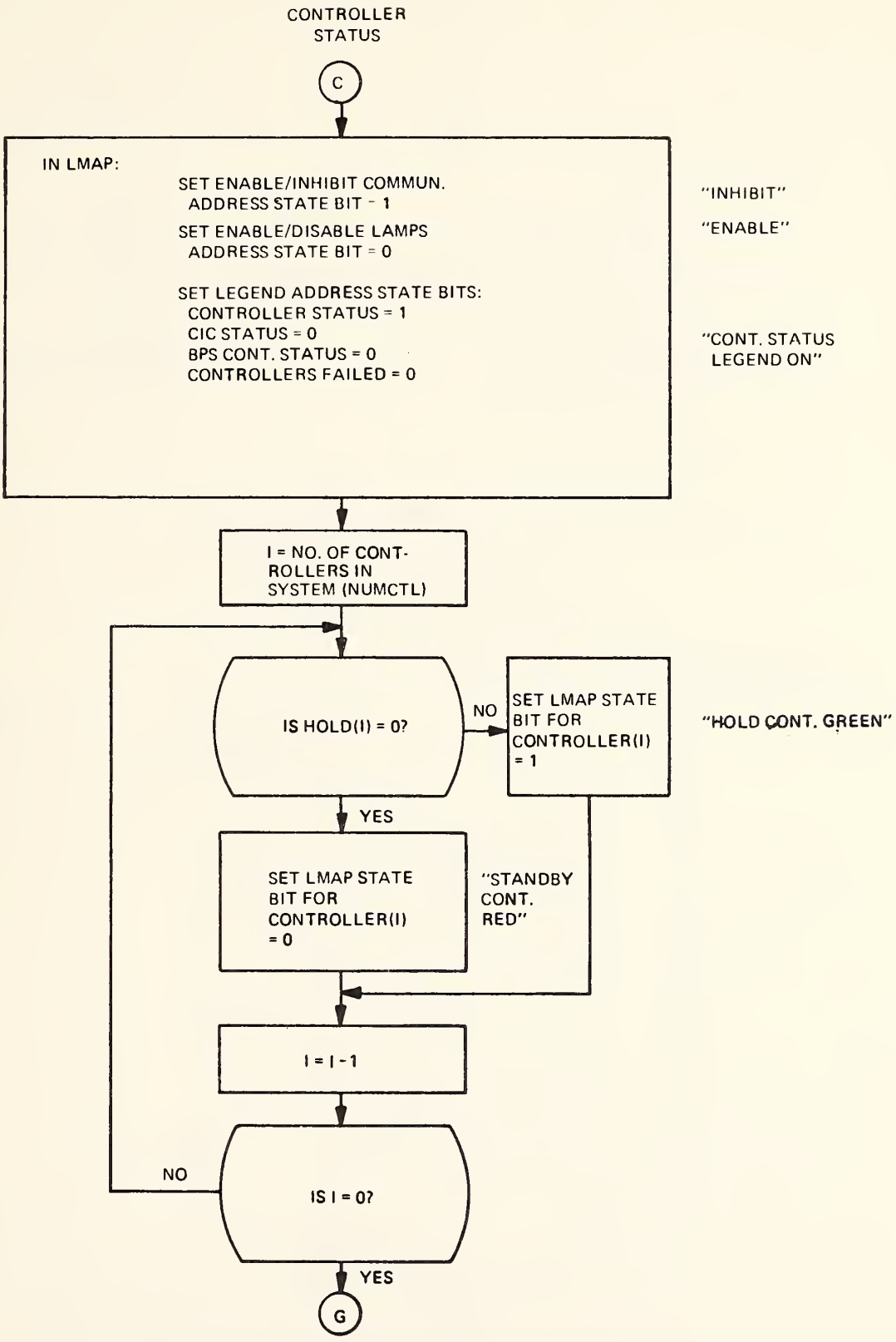


FIGURE 2.11.5.3. ROUTINE J SPECIFICATION

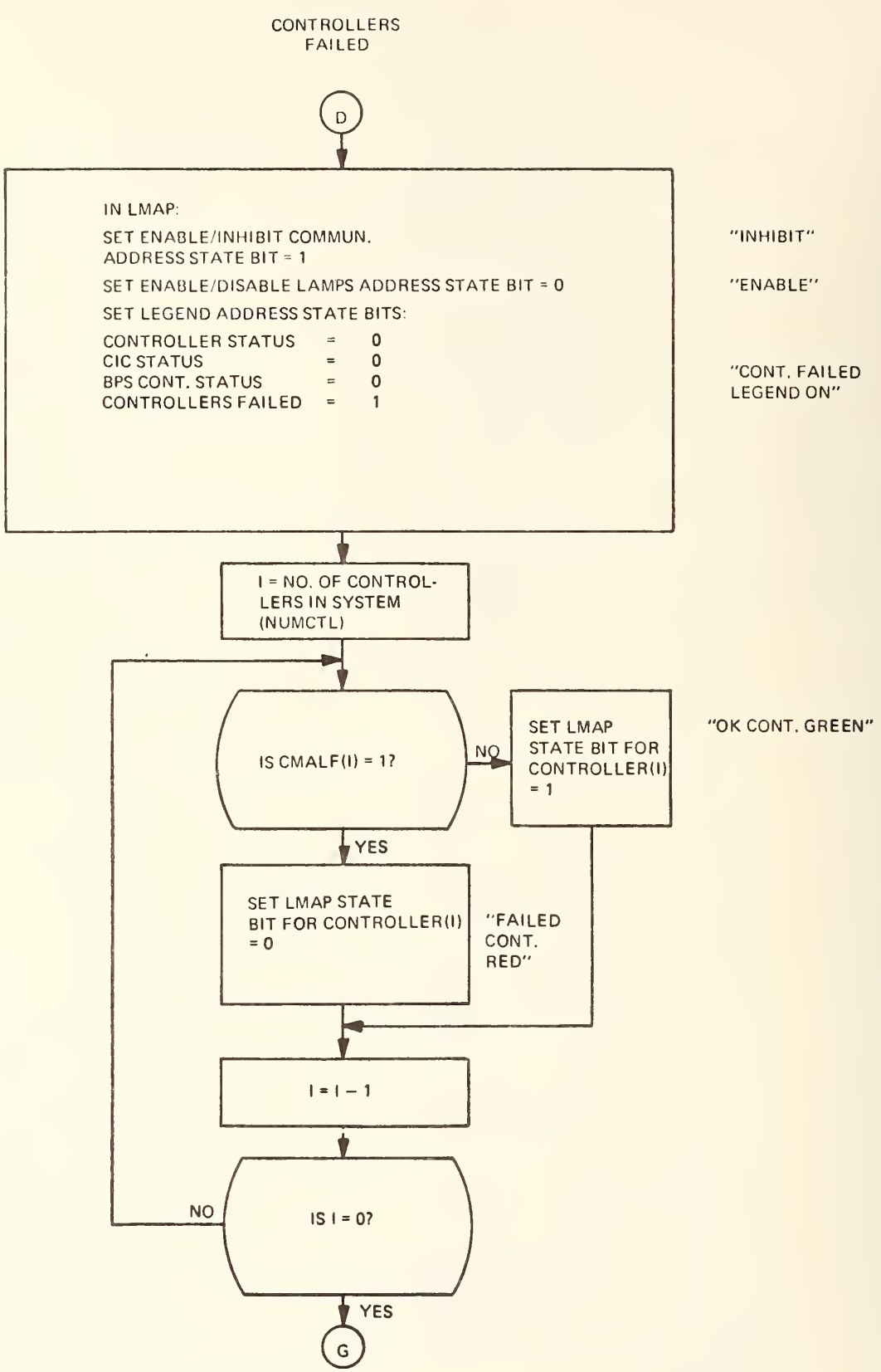


FIGURE 2.11.5.4. ROUTINE J SPECIFICATION

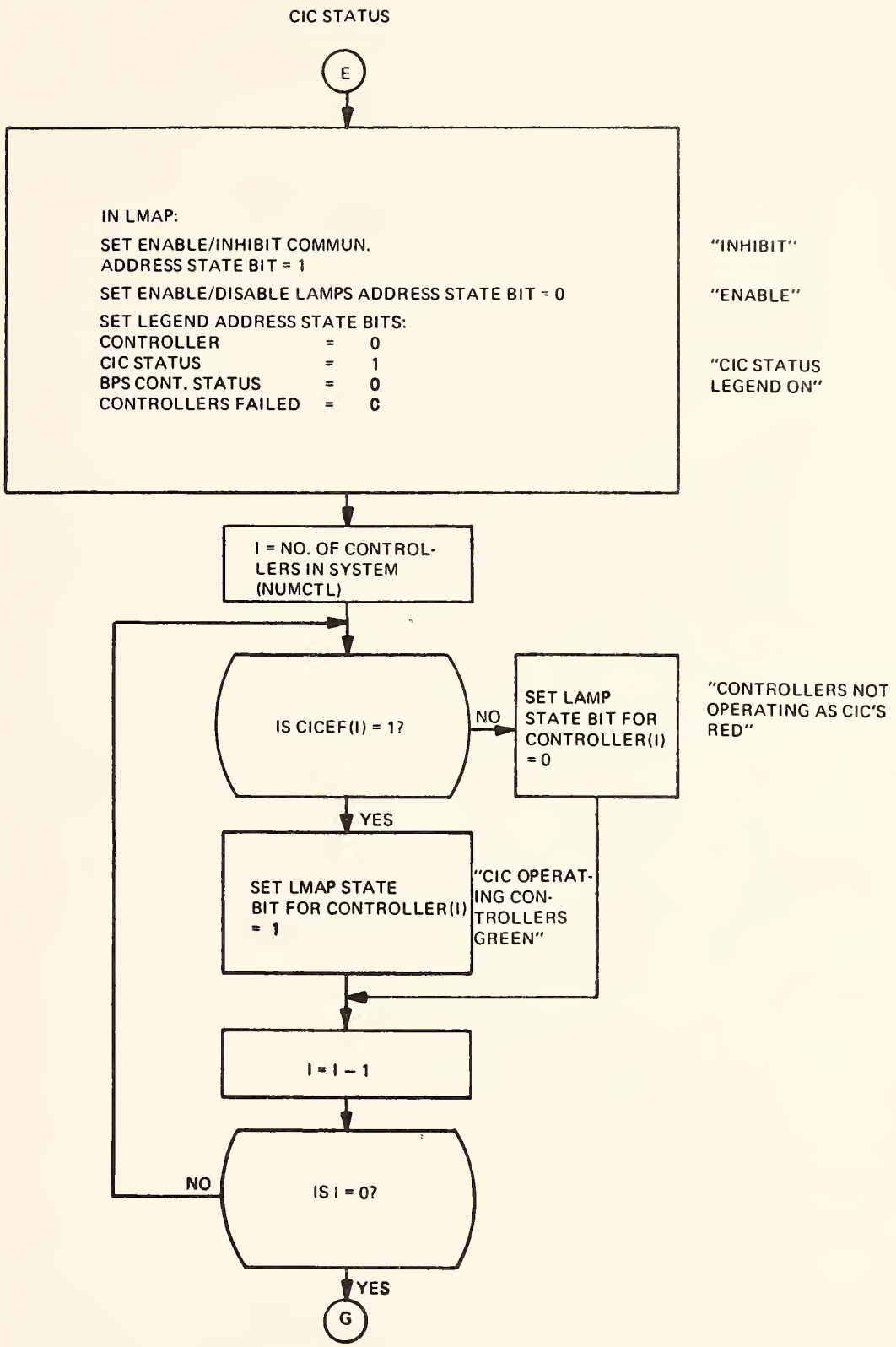


FIGURE 2.11.5.5. ROUTINE J SPECIFICATION

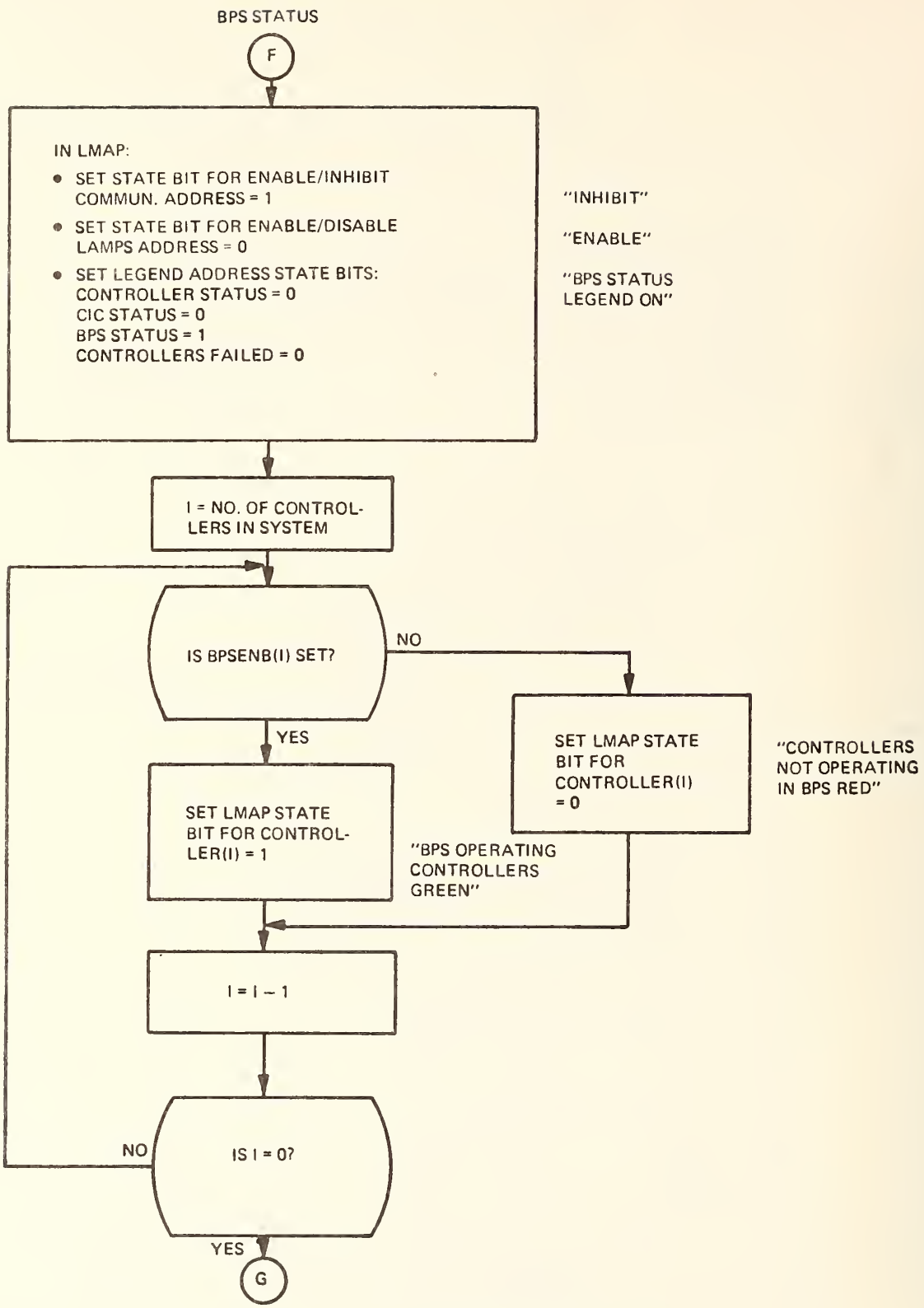


FIGURE 2.11.5.6. ROUTINE J SPECIFICATION

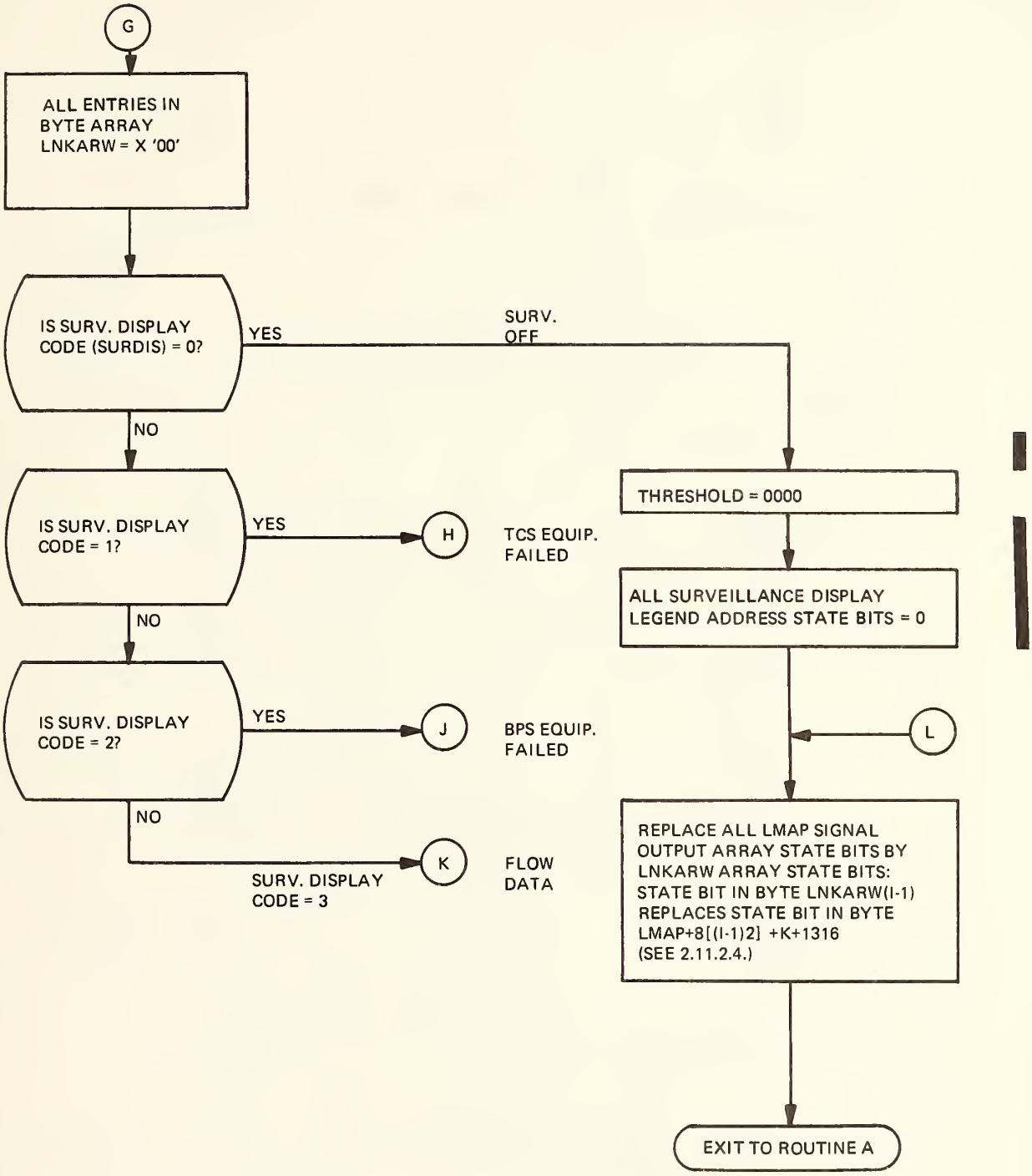


FIGURE 2.11.5.7. ROUTINE J FLOW CHART

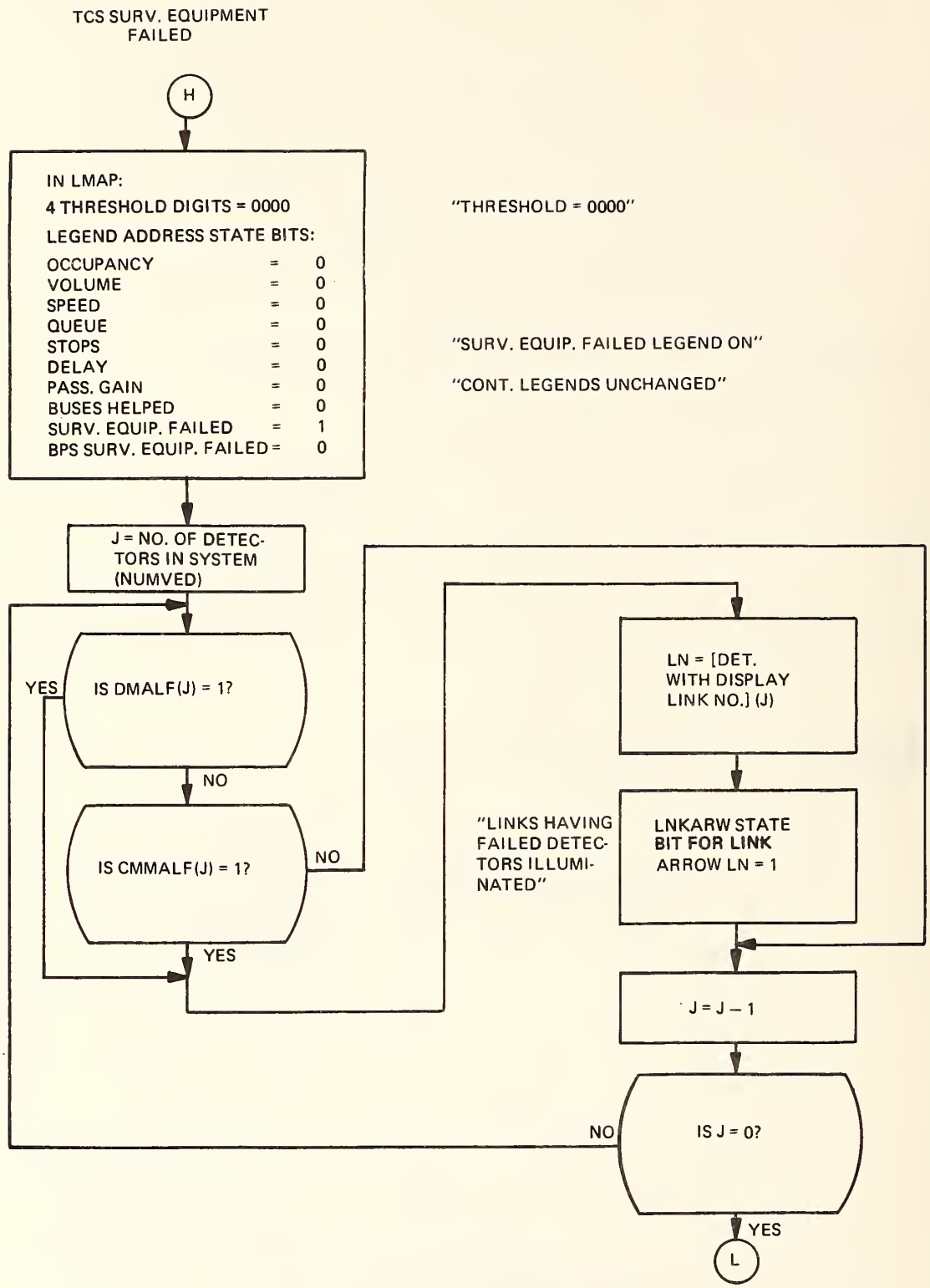


FIGURE 2.11.5.8. ROUTINE J FLOW CHART

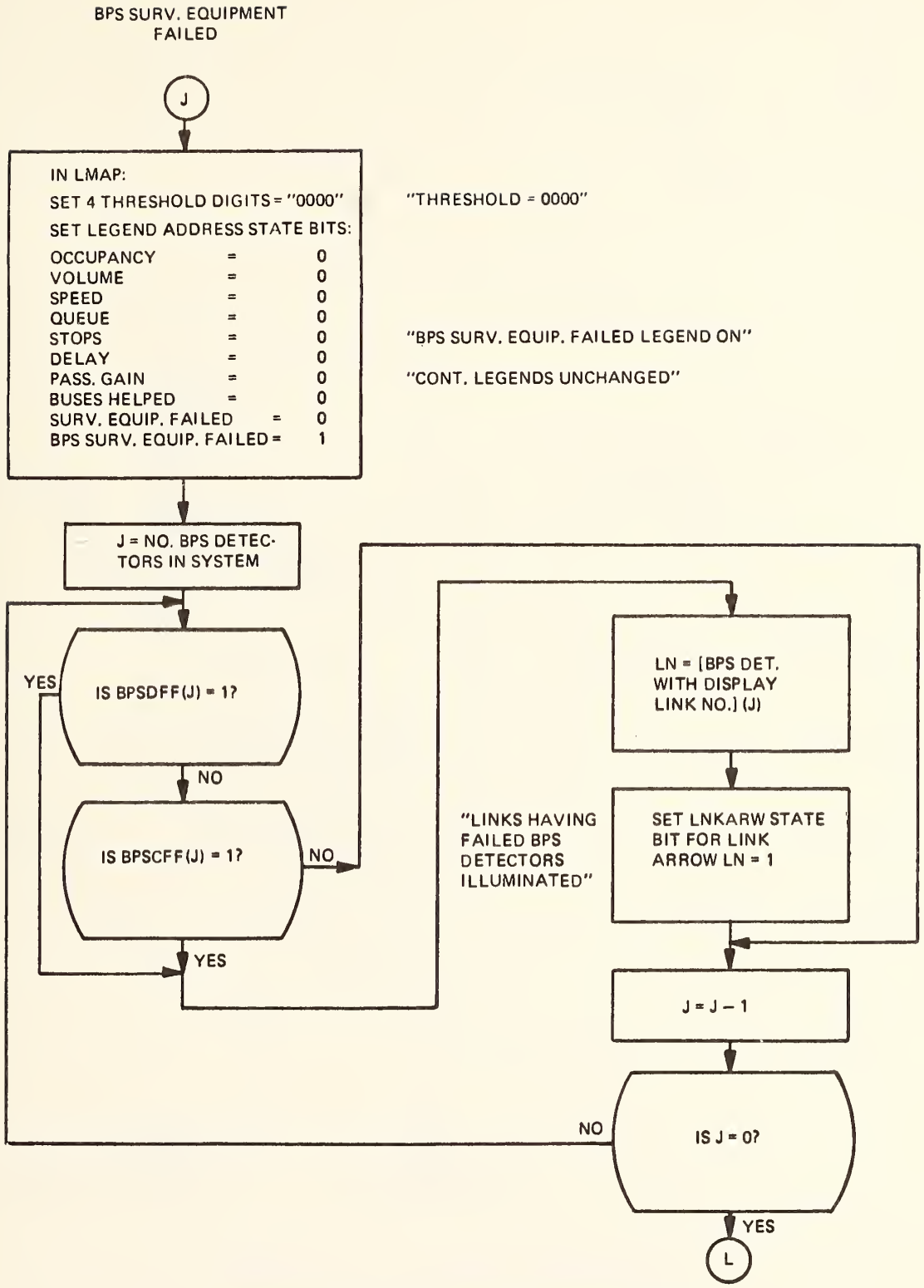


FIGURE 2.11.5.9. ROUTINE J SPECIFICATION

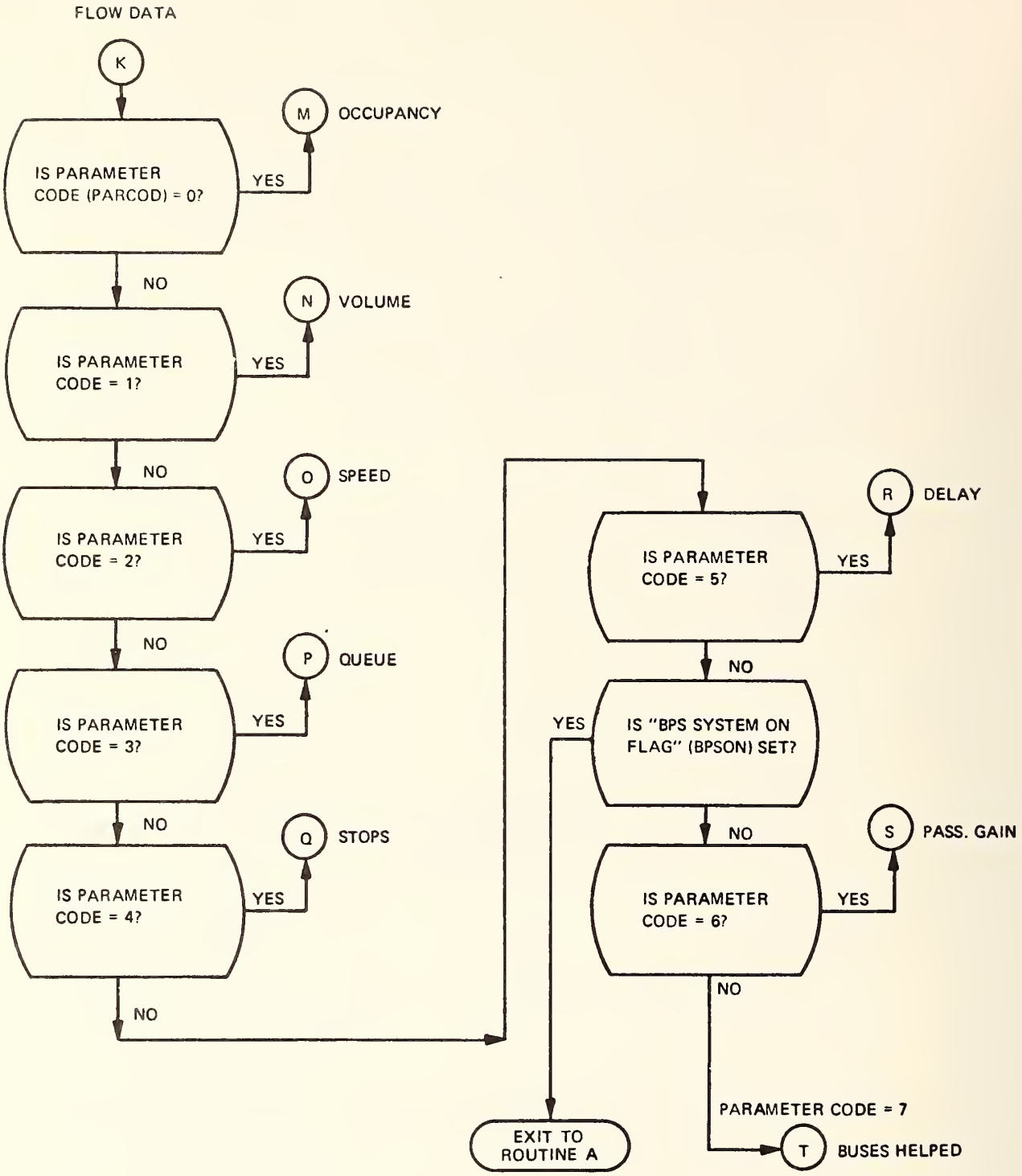


FIGURE 2.11.5.10. ROUTINE J SPECIFICATION

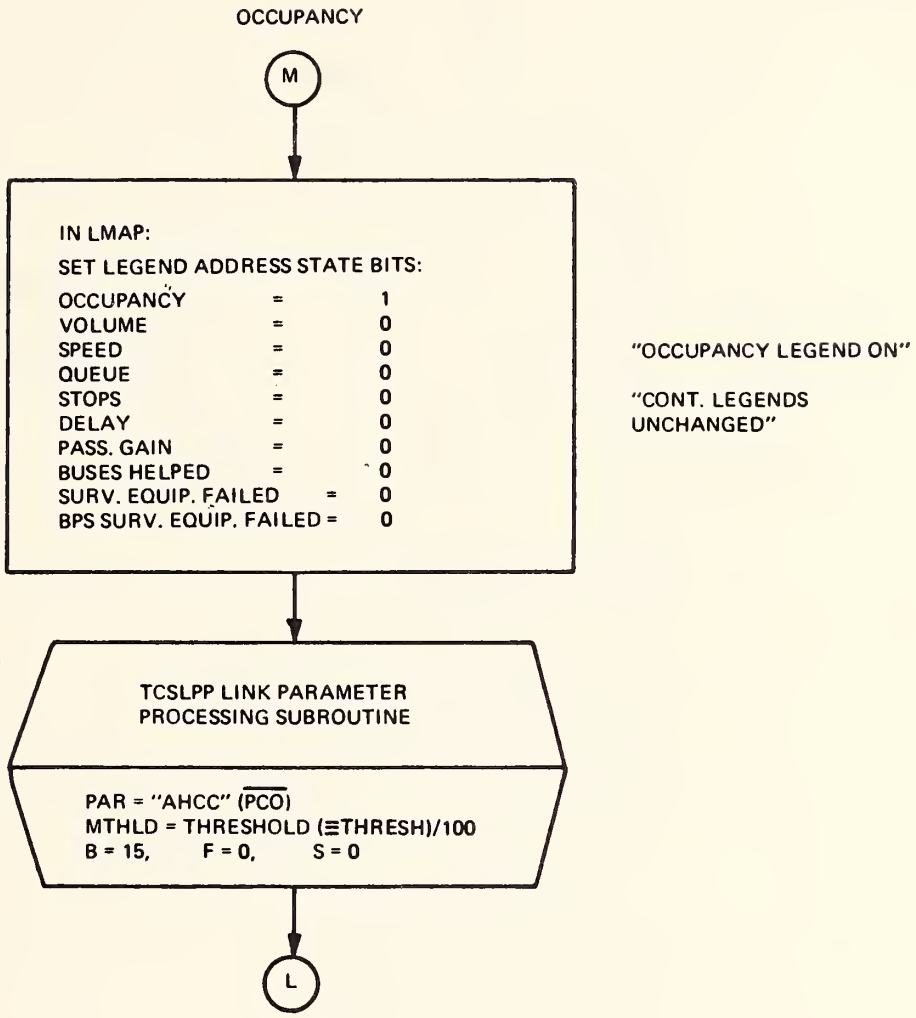


FIGURE 2.11.5.11. ROUTINE J SPECIFICATION

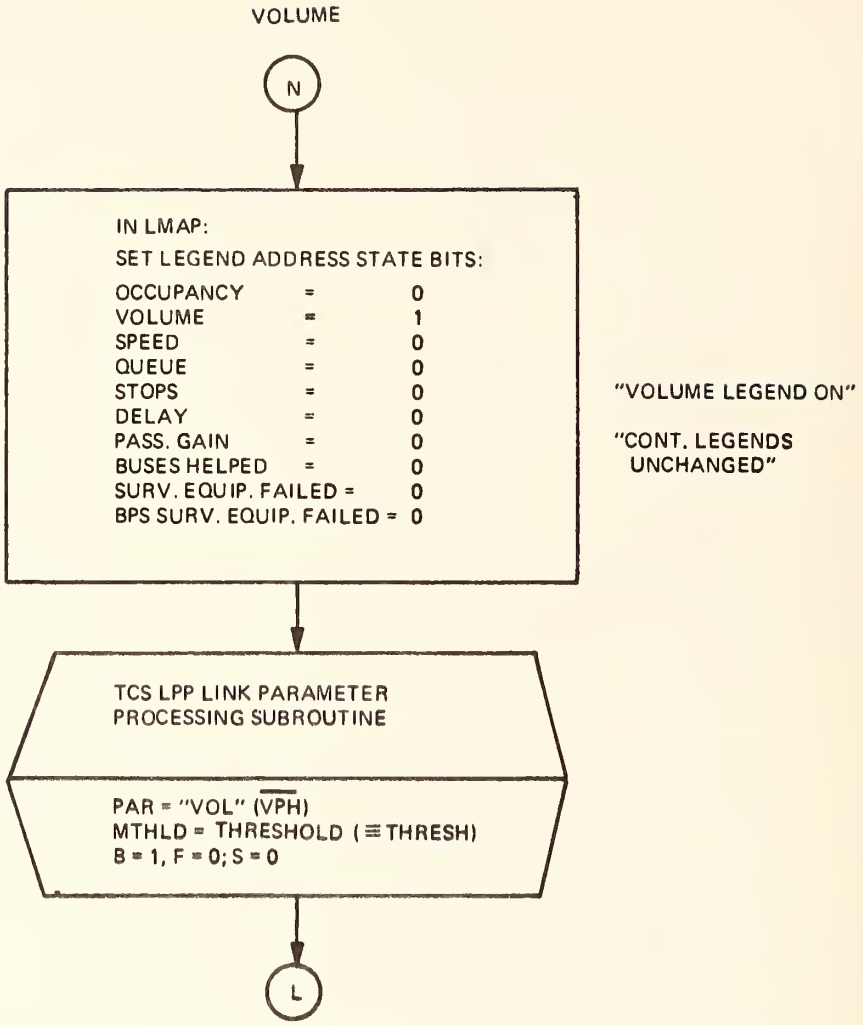


FIGURE 2.11.5.12. ROUTINE J SPECIFICATION

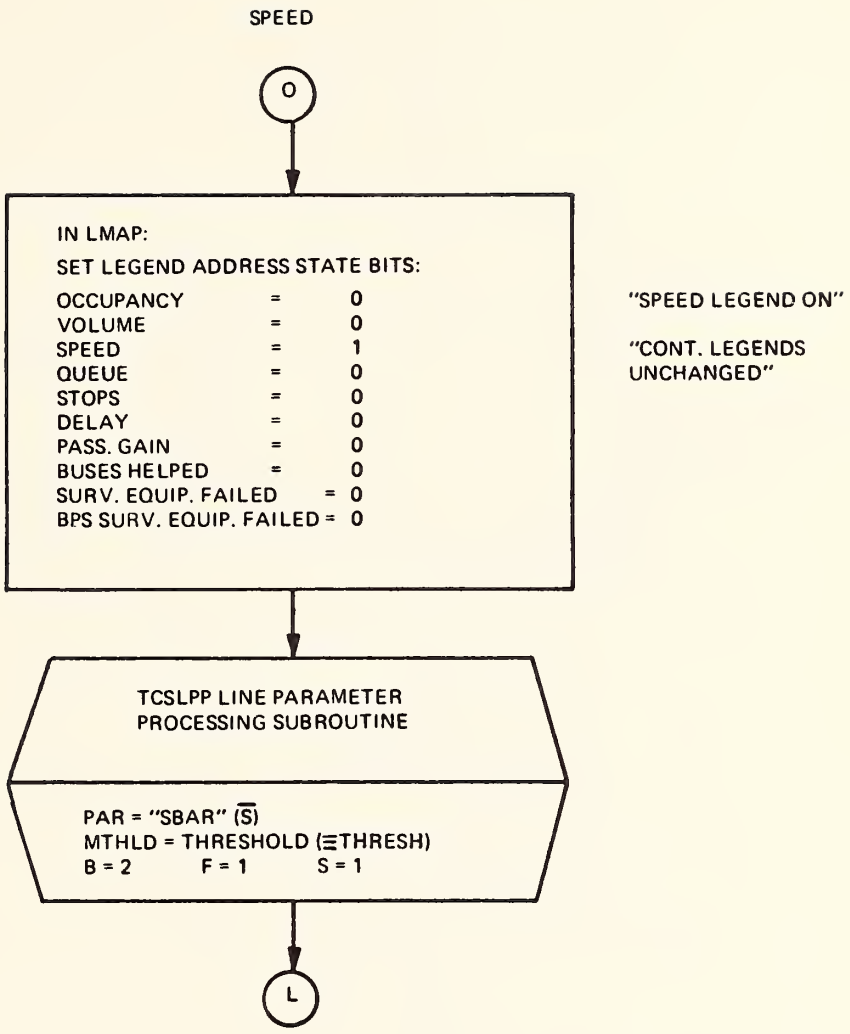


FIGURE 2.11.5.13. ROUTINE J SPECIFICATION

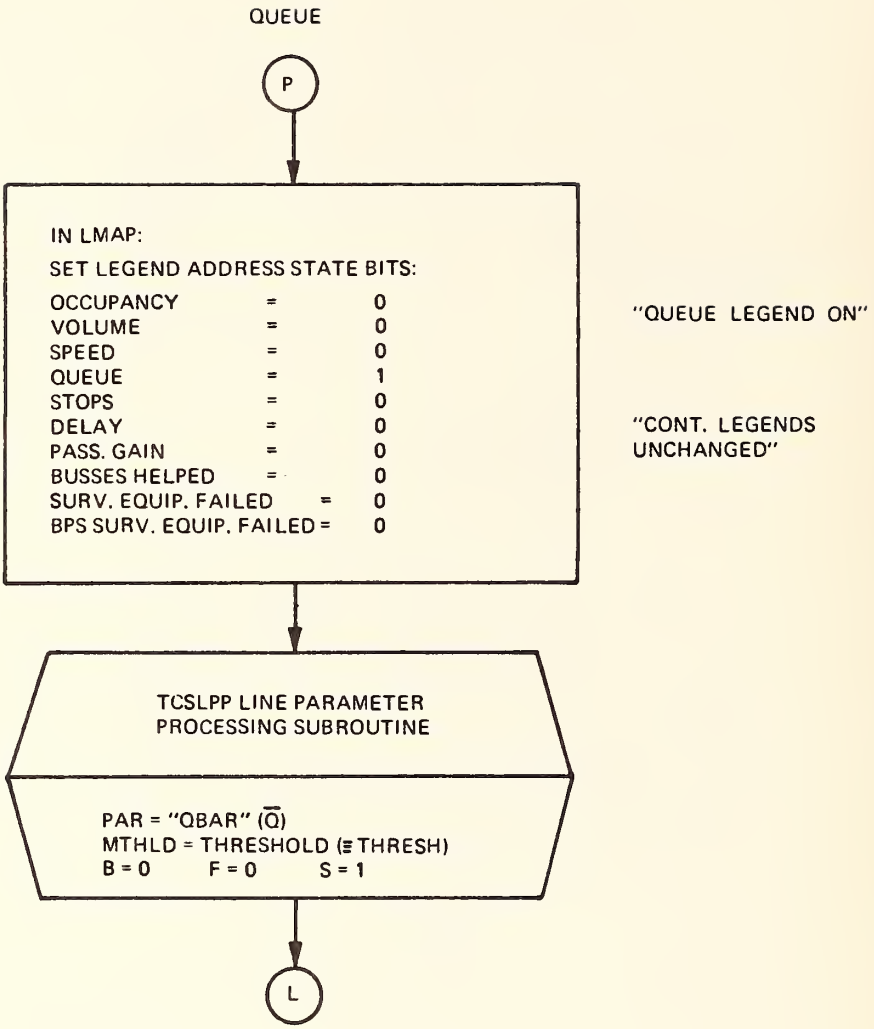


FIGURE 2.11.5.14. ROUTINE J SPECIFICATION

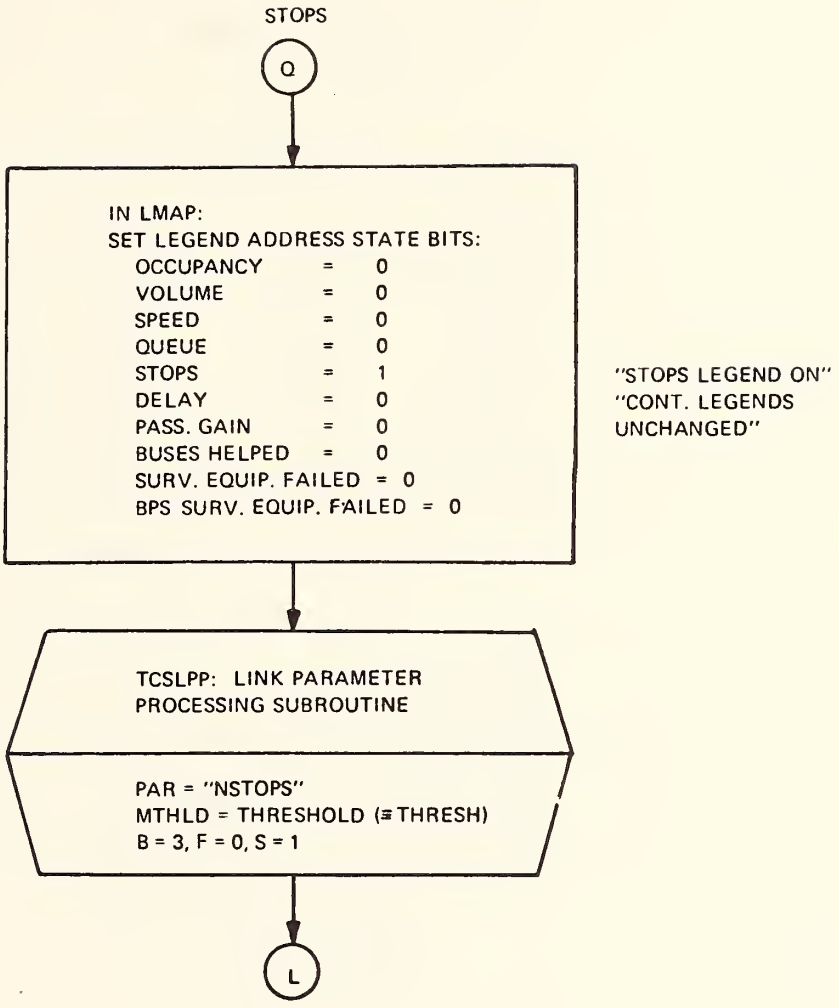


FIGURE 2.11.5.15. ROUTINE J SPECIFICATION

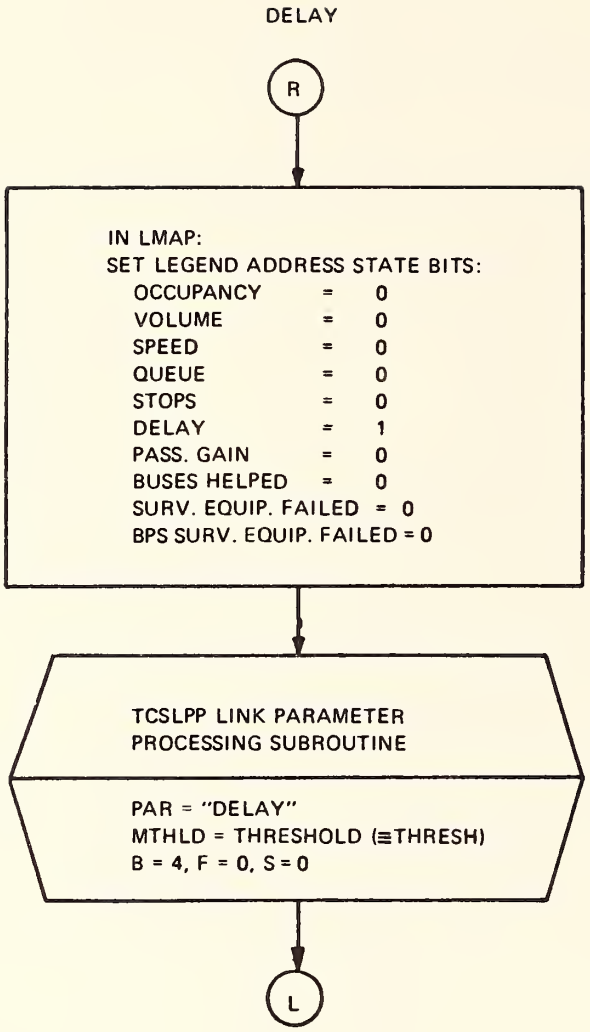


FIGURE 2.11.5.16. ROUTINE J SPECIFICATION

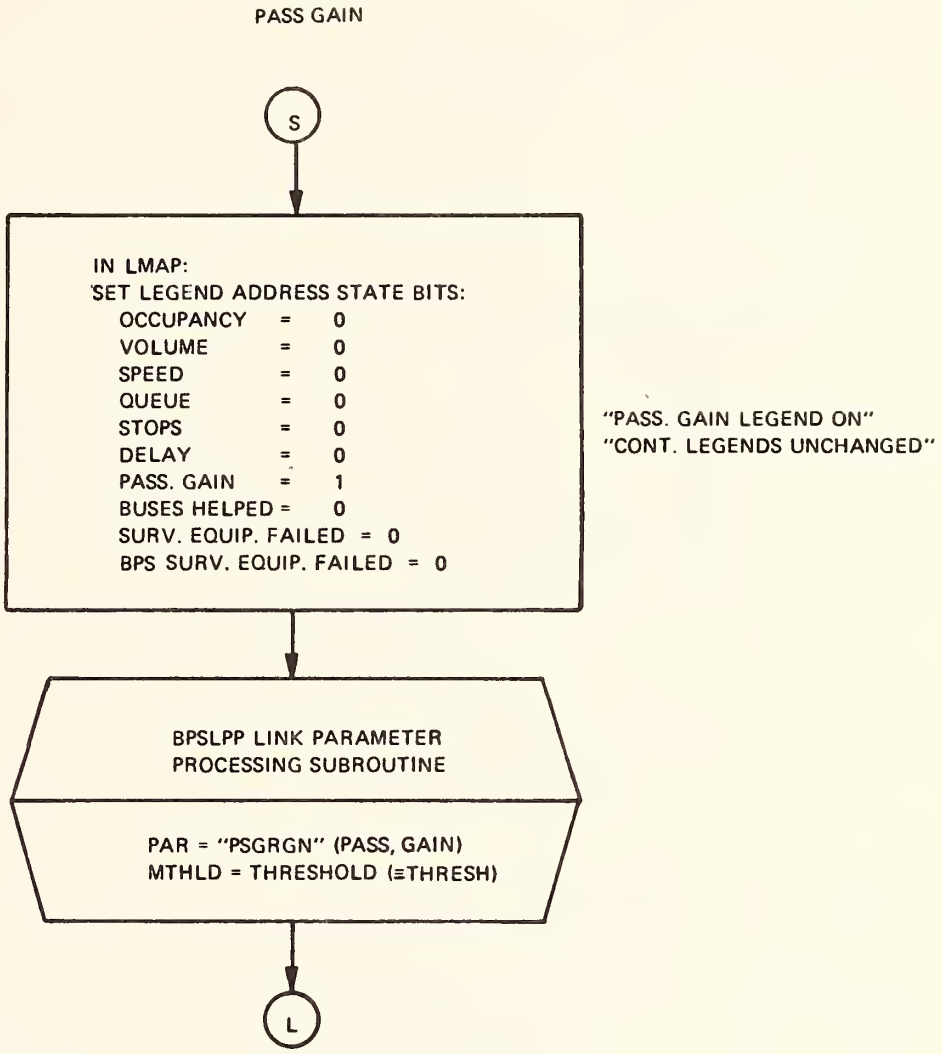


FIGURE 2.11.5.17. ROUTINE J SPECIFICATION

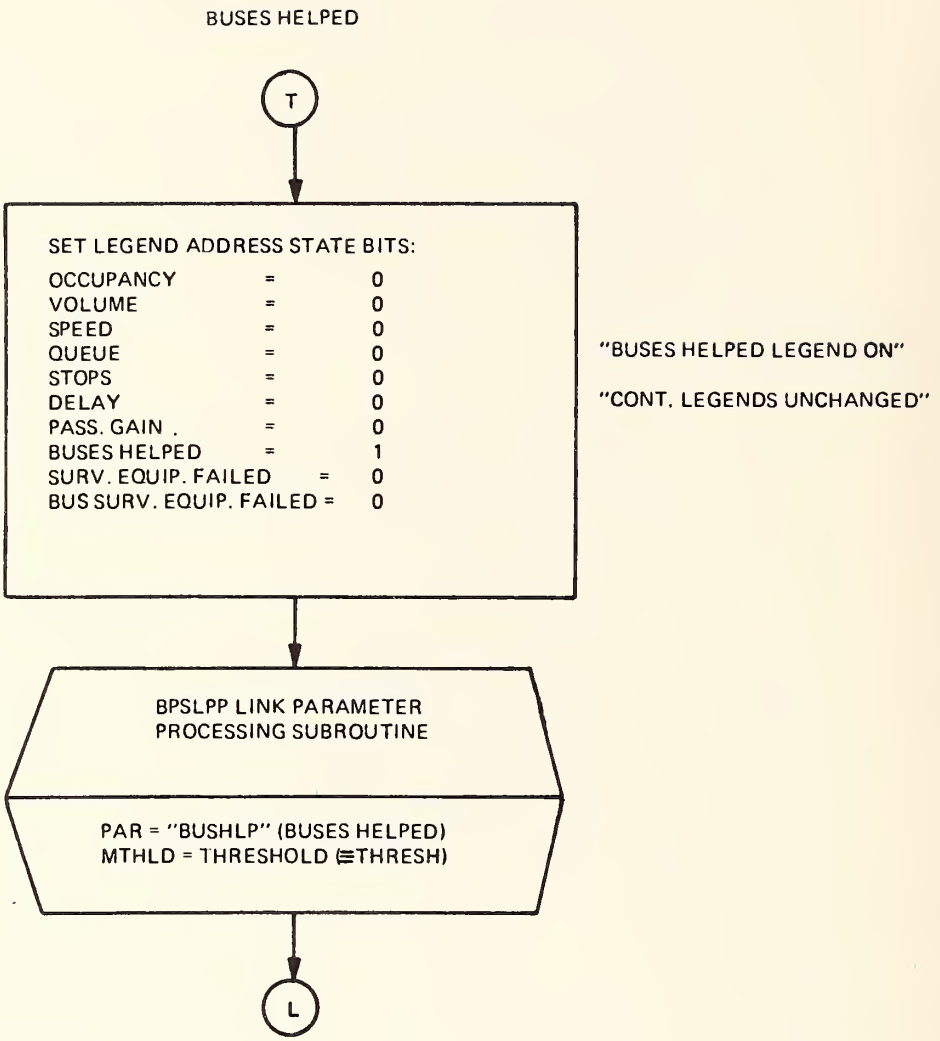


FIGURE 2.11.5.18. ROUTINE J SPECIFICATION

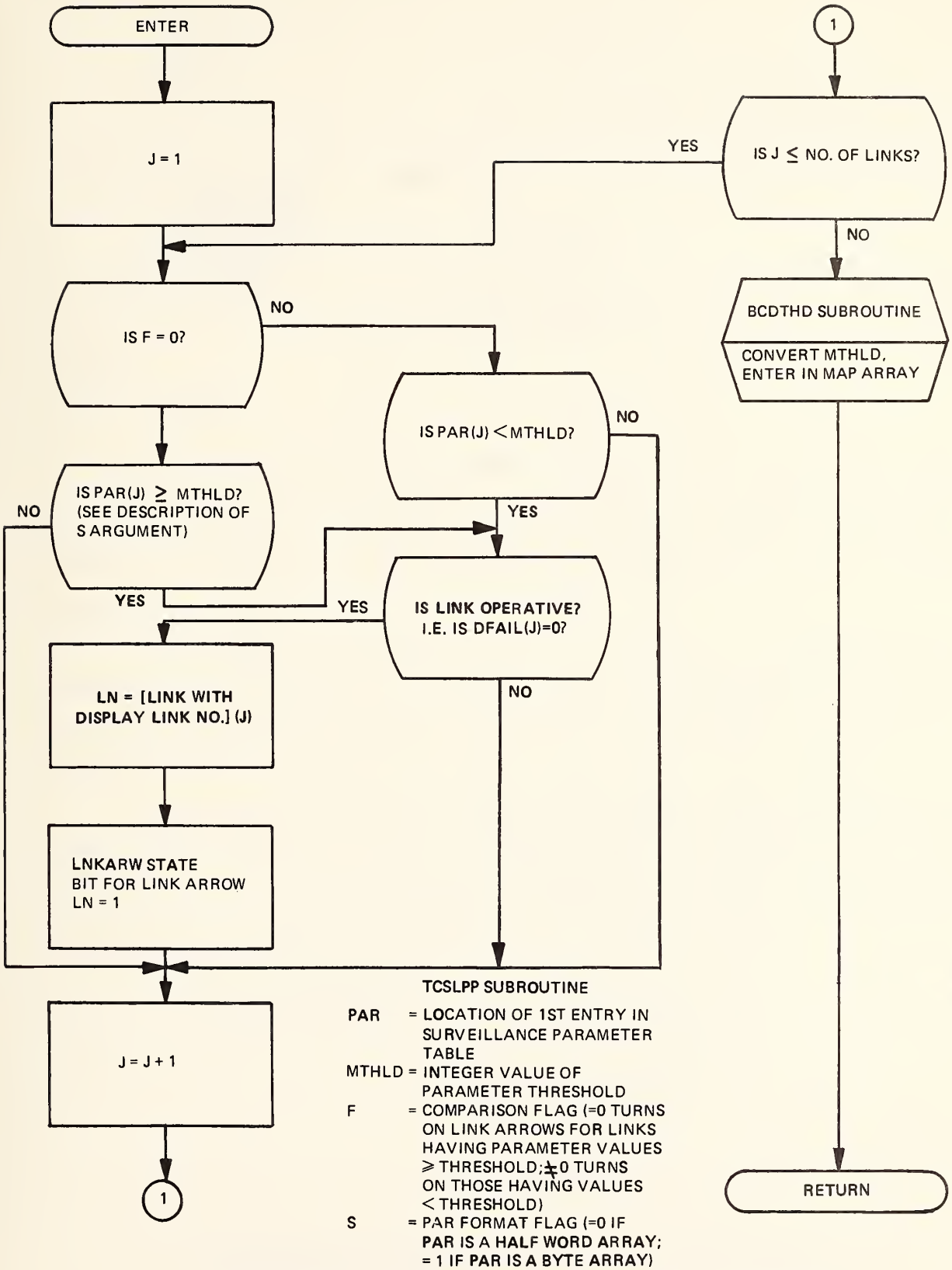


FIGURE 2.11.5.19. TCSLPP SUBROUTINE SPECIFICATION (ROUTINE J)

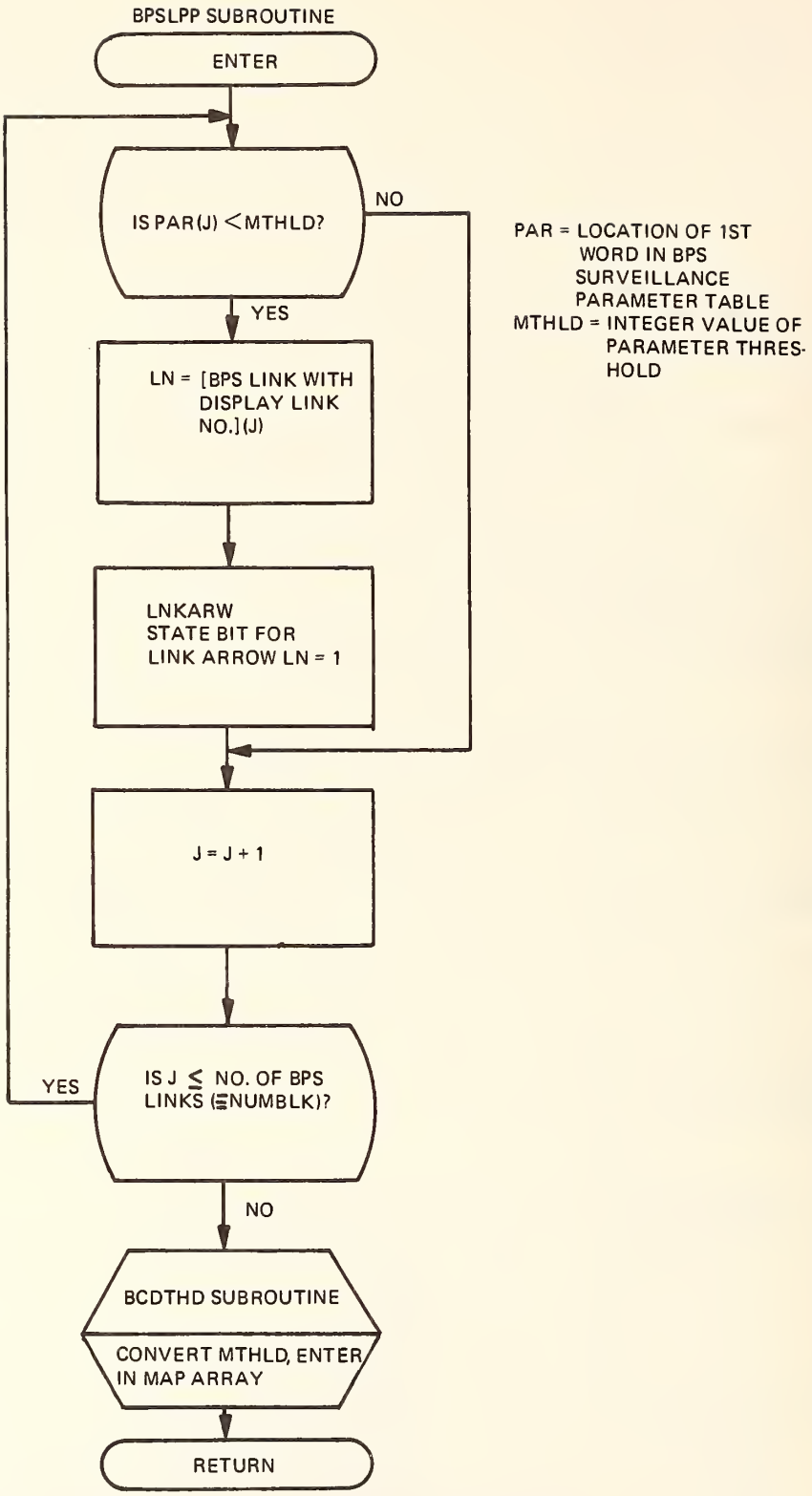


FIGURE 2.11.5.20. BPSLPP SUBROUTINE FLOW CHART (ROUTINE J)

2.12 Routine K (CRT Formatting Routine) Specification

2.12.1 Purpose

1. The CRT Control and Data Formatting Routine examines data and commands formatted in Routine M in accordance with the display controls set at the Operator's Control Panel. The routine executes these commands to cause the selected display to be presented by the CRT device.

2. The CRT Control and Data Formatting Routine Failure Table Updating function remains in core during system operation. This portion of the routine maintains the controller and detector failure tables up to date based on inputs from other operational routines.

2.12.2 Method

The Failure Status Display presents all the controller, detector, and communications failures currently recognized by the UTCS/BPS System. The type, equipment identification number, time and date, and acknowledge status of each failure are contained in the Failure Table which is updated by two subroutines of Routine K. See Figure 2.12.2.2.

The System Status Display presents, for each section in the Traffic Control System, its current operating mode and pattern, the time and desired mode of the latest valid operator mode change request, the numbers of CIC and BPS intersections in operation, and the numbers of detector and controller failures. See Figure 2.12.2.3.

The Controller Status Display lists the identification number and status for each Traffic System controller in standby, or designated as a CIC controller by the operator but inhibited from CIC operation because of the time-of-day, or currently operating as a CIC controller. Controllers operating under Traffic System control but which have not been designated as CIC controllers are not listed. See Figure 2.12.2.4.

The Detector Status Display lists all detectors in standby or which have failed. Detectors operating normally are not listed. See Figure 2.12.2.5.

The CRT Intersection Status display provides a variety of information on a selected intersection, the intersection being identified by its controller number. The information presented includes the number of the section of which the intersection is a member, the number of phases at the intersection, and the duration of the intervals in the controller cycle. The cycle length, offset value, and the lengths of the variable green intervals for A- and B- Phase are also displayed along with minimum values of A-Phase Green. The controller mode and pertinent link data completes the display. See Figure 2.12.2.6.

The BPS System Status display provides the required status information by section and by intersection. See Figure 2.12.2.7

Finally, the BPS Intersection Status display provides the pertinent bus data for each individual BPS intersection as requested. See Figure 2.12.2.8

In addition to the display functions performed by the CRT Control and Data Formatting Routine, two Failure Table Updating functions are also performed. These are (1) Add, and (2) Failure Acknowledge/Failure Repair.

The Add portion of the routine is entered whenever a failure is identified by one of the other operational routines. The routine is entered with the number of the failed component and a code designating the nature of the failure, whether controller, detector, communications, bus detector or bus communications. The Add function adds the component, along with present time, to the Failure Status table and increments the appropriate System Status failure list. The Audible Alarm and the appropriate warning light are turned on to alert the operator.

The Failure Acknowledge/Failure Repair portion of the routine is entered from the Manual Control Panel Processing Routine with the number of the equipment and its type. The table of failures is searched to locate the component in question. If it is not found, a Failure Error Flag (FLERFL) is set. If it is found, the appropriate code is added to the display table. If the Failure Repair function is required, the component is removed from the table and other components moved, where required, to close the gap in the table. The appropriate System Status failure list is decremented, the Audible Alarm is turned off, and the appropriate warning light is extinguished. Control is then returned to the Manual Control Panel Processing Routine.

Sample formats of the display pages are shown in Figures 2.12.2.2 through 2.12.2.8.

The CRT Control and Data Formatting Routine comprises three separate subprograms. Routine K proper generates a buffer of data for the specified status display and causes that buffer to be output to the appropriate CRT. Subroutines KFMT and KFTU update the Failure Table whose contents may be presented by the Failure Status Display.

Routine K is scheduled by the Manual Control Panel Routine (M) as a result of an operator status display request; by the Executive Routine (A) once per 25 seconds for updating current displays; and by the Start-Up Routine (Y) for displaying initial System Status. The Level 3 Executive Routine will then enter Routine K whenever there are no other higher priority Level 3 tasks to be reformed.

On the other hand, Subroutine KFMT (Acknowledge/Repair) is entered directly by its calling program, Routine M; KFTU is entered by scheduling Routine K and setting flags to tell Routine K that there are failures to be added to the failure table.

Both CRT's are updated each time a display request is made, unless an error condition exists on one of CRT lines. CRT 1 is updated first.

Routine K determines which display pages have been requested by examining the CRT Display Code (global variables CRTDC1 or CRTDC2). Display Code values of 1, 2, 3, 4, 5, 6, and 7 correspond respectively to Failure Status, System Status, Controller Status, Detector Status, Intersection Status, BPS System Status and BPS Intersection Status. Routine K branches to the appropriate program segment to obtain the data to be displayed, to format it, and to enter it in the output buffer for the selected CRT.

Utility subroutines are used to convert and format display data. For each display type, Routine K first initializes the buffer and generates a "boilerplate" display containing fixed formats, column headings, etc. It then converts the variable display data and enters them into the output buffer. All CRT characters are displayed in a protected mode to assure non-interference from the CRT keyboard.

After completing the output buffer for the CRT, Routine K stores the number of characters to be output from the buffer, sets the Output Channel Active Flag for the selected CRT and triggers the Level 4 interrupt (X'68'). The actual character-by-character transmission to the CRT is initiated by Routine CRTOUT. See Figure 2.12.5.10. The transfer is accomplished using RBM supplied Character Oriented Communications (COC) software. The output is transmitted over standard XDS Sigma 5 TTY interface.

Subroutine KFMT (T, U, V) Method (Failure Acknowledge/Repair)

Subroutines KFMT updates the Failure Table according to the Change Code (V) contained in global variable FMTCHG. If V specifies a failure acknowledge (V=11) indicating that the operator wishes to acknowledge the failure of the equipment designated by T and U, KFMT sets the acknowledge status indicator to one (YES) in the appropriate entry of the Failure Table, turns off the appropriate malfunction indicator on the Control Panel and turns off the audible alarm. The other possible value of V (V = 12) specifies a failure repair. KFMT then deletes the appropriate entry in the Failure Table and reduces the sectional equipment and total system failure counts by one. In both cases, KFMT determines the equipment Type (T) from global variable FMTTYP (=3 for controller, =4 for detector, =5 for communications, =6 for Bus Detector, =7 for Bus Communication) and the identification number (U) from FMTNUM. If no failure has been recorded in the Failure Table for the designated equipment, KFMT sets the Failure Error Flag non-zero (global variable FLERFL) to signal an illegal request.

Array Formats

Failure Table (FAILTB)

The Failure Table has a capacity of 200 entries. Each four-word entry has the format:

Word 1,	Byte 0:	Acknowledge status (0 for NO, 1 for YES)	
	Byte 1:	Equipment type code (3 for controller, 4 for detector, 5 for communications, 6 for bus detector, 7 for bus communication)	
	Byte 2, 3:	Equipment identification number (binary)	
Word 2,	Byte 0:	X'4'	
	Byte 1:	h	EBCDIC characters for time (hour and minute) of failure.
	Byte 2:	h	
	Byte 3:	m	
Word 3,	Byte 0:	m	

	Byte 1:	X'3'	
	Byte 2:	M	} EBCDIC characters for abbreviated month
	Byte 3:	M	
Word 4,	Byte 0:	M	
	Byte 1:	X'2'	
	Byte 2:	D	} EBCDIC characters for date
	Byte 3:	D	

Note that the EBCDIC character strings for the time and date of the failure can be obtained using the RBM TIME CAL and stored in the Failure Table in a suitable format.

Sectional Controller Failure Count Array (SECCFC)

The Sectional Controller Failure Count Array has a word capacity equal to the number of sections in the Traffic Control System (N_S). Each one-word entry contains, in binary, the number of failed controllers contained in the section.

SECCFC: Number of failed controllers in Section 1

SECCFC + 1: Number of failed controllers in Section 2

.
.
.

SECCFC +N_S - 1: Number of failed controllers in Section N_S

Sectional Detector Failure Count Array (SECDFC)

The Sectional Detector Failure Count Array has a word capacity equal to the number of sections in the Traffic Control System (N_S). Each one-word entry contains, in binary, the number of failed detectors contained in this section. Both vehicle and bus detector failures are included in these totals.

SECDFC: Number of failed detectors in Section 1

SECDFC +1: Number of failed detectors in Section 2

.
.
.

SECDFC +N_S -1: Number of failed detectors in Section N_S.

2.12.3 Repetition Rate

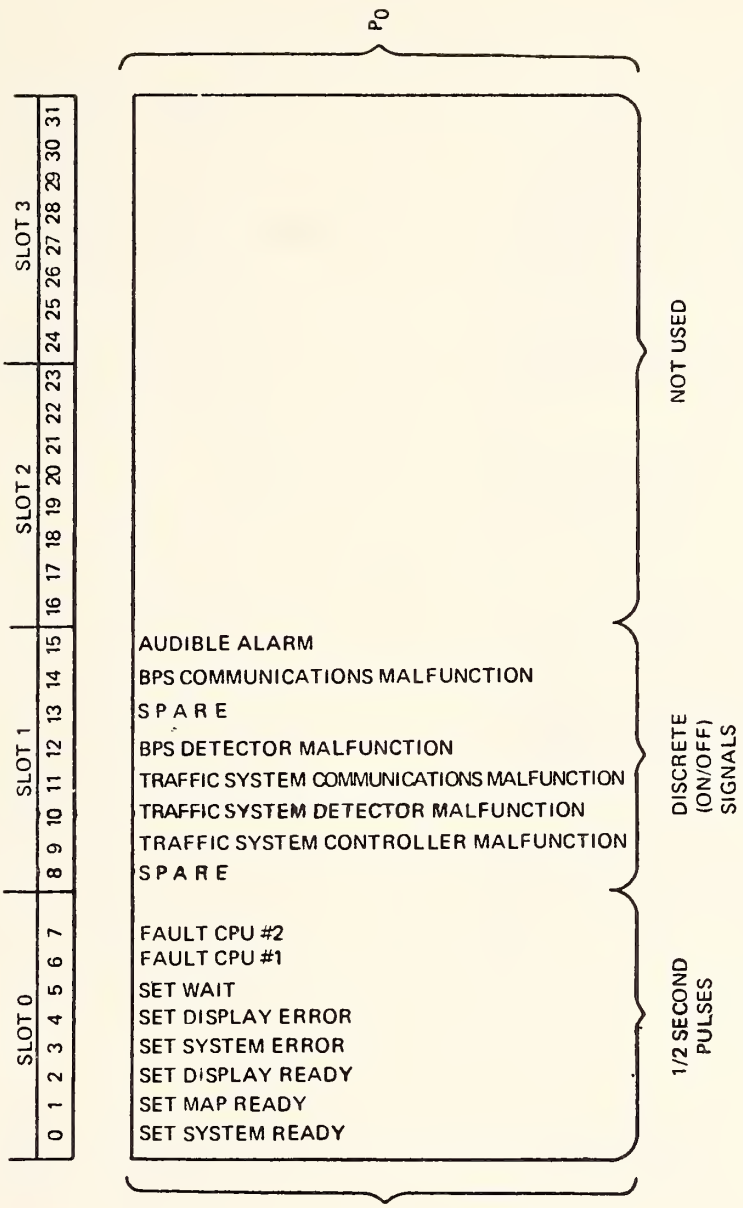
This routine is entered whenever the operator calls for a change and at 25 second intervals.

2.12.4 Cross Reference

The CRT Control and Data Formatting Routine is entered from the Level 3 Executive Routine.

The Failure Table Updating Add Function, Subroutine KFTU, is entered from Routine K through the use of indicator flags set by Routines P, E and BPS Routine BF.

The Failure Table Updating Failure Acknowledge/Failure Repair function, Subroutine KMFT, is entered from the Manual Control Panel Processing Routine.



NOTE: BIT 6 (CPU # 1 FAULT) MUST ALTERNATE STATES AT LEAST ONCE EVERY 2 SECONDS.

OUTPUT ON 7930-1, CONTROL CHANNEL 5

FIGURE 2.12.2.1. CONTROL PANEL OUTPUT BIT ASSIGNMENTS

PAGE DESCRIPTION: FAILURE STATUS
DISPLAY CODE: 1

NOTE: FAILURES ARE LISTED IN REVERSE CHRONOLOGICAL ORDER WITH THE RIGHT HALF ON THE PAGE A CONTINUATION OF THE LEFT HALF.

TIME: 12:24

FAILURE STATUS

TYPE①	NO.②	TIME③	MONTH④	DAY⑤	ACK⑥	TYPE	NO.	TIME	MONTH	DAY	ACK.
DET	126	0900	FEB	4	N	BCOM	12	1401	JAN	30	Y
CONT	64	0842	FEB	4	N	COMM	161	1400	JAN	30	Y
COMM	213	2231	FEB	3	N	DET	14	0958	JAN	30	N
DET	33	1827	FEB	1	Y	CONT	14	0936	JAN	29	N
BCOM	10	1710	JAN	30	Y	CONT	120	0903	DEC	25	Y
BDET	102	1603	JAN	30	Y	BDET	27	0601	DEC	25	Y
						BCOM	31	2347	DEC	24	Y

ALL NORMAL⑦

TRUNCATED LIST – TOTAL NUMBER⑧ = 53⑨

① TYPE: BYTE 1 OF FAILURE TABLE (FAILTB) ENTRY
TYPE CODES:
3 = CONT = CONTROLLER
4 = DET = DETECTOR
5 = COMM = COMMUNICATION
6 = BDET = BUS DETECTOR
7 = BCOM = BUS COMMUNICATION

② EQUIPMENT NO: BYTES 2 AND 3 OF FAILTB ENTRY

③ TIME OF FAILURE: BYTES 5, 6, 7 AND 8 OF FAILTB ENTRY

④ MONTH OF FAILURE: BYTES 10, 11, AND 12 OF FAILTB ENTRY

⑤ DAY OF FAILURE: BYTES 14 AND 15 OF FAILTB ENTRY

⑥ ACKNOWLEDGE CODE: BYTE 0 OF FAILTB ENTRY
0 = N = NO
1 = Y = YES

⑦ THIS MESSAGE IS DISPLAYED WHEN NO SYSTEM FAILURES ARE PRESENT

⑧ THIS MESSAGE IS DISPLAYED WHEN THE NUMBER OF SYSTEM FAILURES EXCEEDS CRT PAGE CAPACITY (38 FAILURES).

⑨ NUMBER OF SYSTEM FAILURES (NOFAIL).

FIGURE 2.12.2.2. FAILURE STATUS FORMAT

PAGE DESCRIPTION: SYSTEM STATUS
DISPLAY CODE: 2

TIME: 12:24

SYSTEM STATUS

HISTORY ON①

SECT.	TIME②	DESIRED③ MODE	ACTUAL④ MODE	PATTERN⑤ NO.	CIC⑦ IN OP.	BPS⑦ IN. OP.	FAILURES⑧ DET.	FAILURES⑧ CONT.
1	0905	TRSP	TRSP	7	2	1	0	0
2	1003	MAN	MAN	3	5	3	1	0
3	0905	TOD	TOD	5	14	12	10	2
4	1102	STBY	STBY	1⑥	6	2	3	0

① HISTORY CODE: (HRF)
0 = OFF
1 = ON

② TIME OF MODE CHANGE: (TIMMCH)

③ DESIRED MODE: (DMODE)
0 = STBY = STANDBY
1 = MAN = MANUAL
2 = TOD = TIME OF DAY
3 = TRSP = TRAFFIC RESPONSIVE
MODE REQUESTED BY OPERATOR AT TIME SHOWN.

④ ACTUAL MODE: (MODES)
CODES SAME AS ③
CURRENT OPERATING MODE OF SECTION.

⑤ PATTERN NUMBER: (PATNUM)
CURRENT PATTERN BEING IMPOSED OR TRANSITIONED TO.

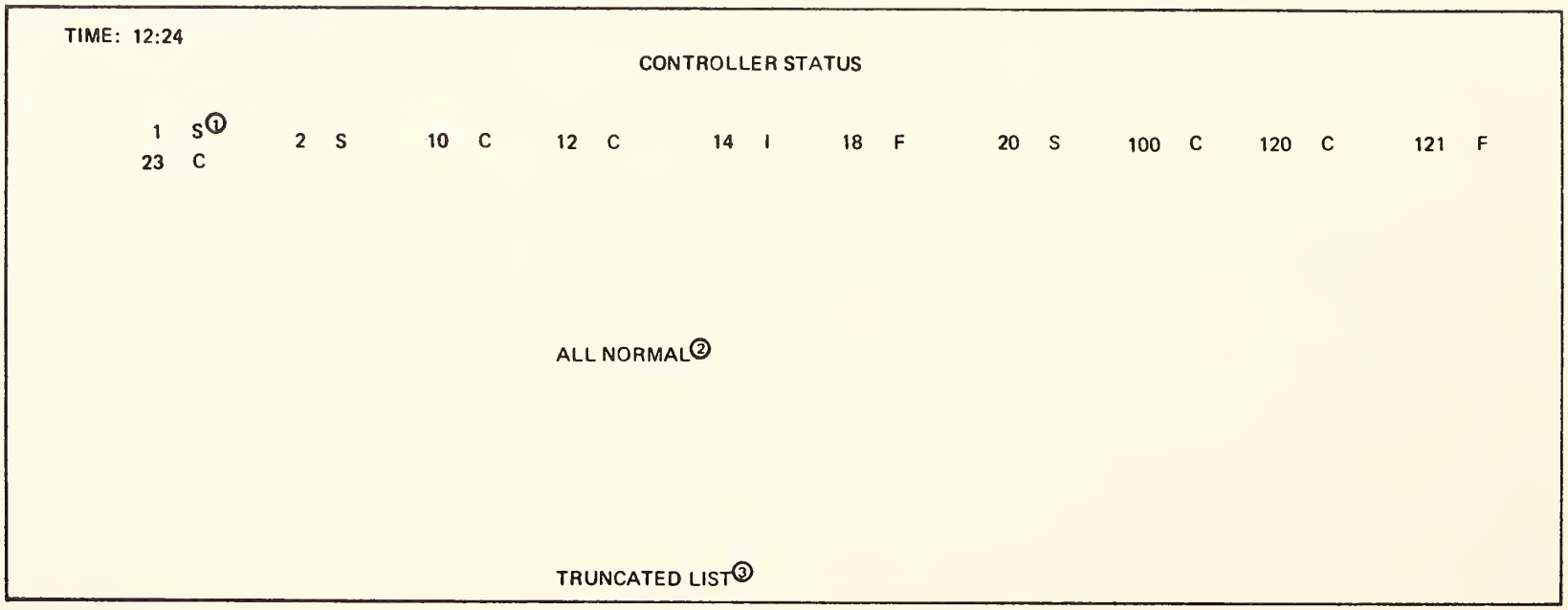
⑥ WHEN MODE IS STBY-PATTERN NUMBER INDICATES CURRENT VALID TOD PATTERN.

⑦ CIC AND BPS IN OPERATION:
VALUES ARE COMPUTED AT DISPLAY TIME. INDICATES ALL CONTROLLERS SELECTED FOR CIC OR BPS WHICH ARE NOT INHIBITED.

⑧ DETECTOR AND CONTROLLER FAILURES: (SECDFC AND SECCFC)
CURRENT NUMBER OF FAILURES IN EACH SECTION.
NOTE: DETECTOR FAILURES DISPLAYED INCLUDES BOTH VEHICLE AND BUS DETECTORS.

FIGURE 2.12.2.3. SYSTEM STATUS FORMAT

PAGE DESCRIPTION: CONTROLLER STATUS
DISPLAY CODE: 3



① CONTROLLER STATUS CODES:
S = STANDBY (HOLD)
F = FAILED (CMALF)
C = OPERATING CIC (CICEF)
I = INHIBITED CIC (CICSF ∩ $\overline{\text{CICEF}}$)

② MESSAGE DISPLAYED WHEN ALL CONTROLLERS ARE ON LINE AND NONE HAVE BEEN SELECTED FOR CIC

③ MESSAGE DISPLAYED WHEN NUMBEF OF ENTRIES EXCEEDS CRT PAGE CAPACITY (230 CONTROLLERS)

FIGURE 2.12.2.4. CONTROLLER STATUS FORMAT

PAGE DESCRIPTION: DETECTOR STATUS
DISPLAY CODE: 4

TIME: 12:24

DETECTOR STATUS

1	S①	3	S	5	S	13	D	27	C	106	S	412	C	461	D			

ALL NORMAL②

TRUNCATED LIST③

① DETECTOR STATUS CODES:
S = STANDBY (DIS)
D = DETECTOR FAILED (DMALF)
C = COMMUNICATION FAILED (CMMALF)

② MESSAGE DISPLAYED WHEN ALL DETECTORS ARE ON LINE

③ MESSAGE DISPLAYED WHEN NUMBER OF ENTRIES EXCEEDS CRT PAGE CAPACITY (230 DETECTORS)

FIGURE 2.12.2.5. DETECTOR STATUS FORMAT

PAGE DESCRIPTION: INTERSECTION STATUS
DISPLAY CODE : 5

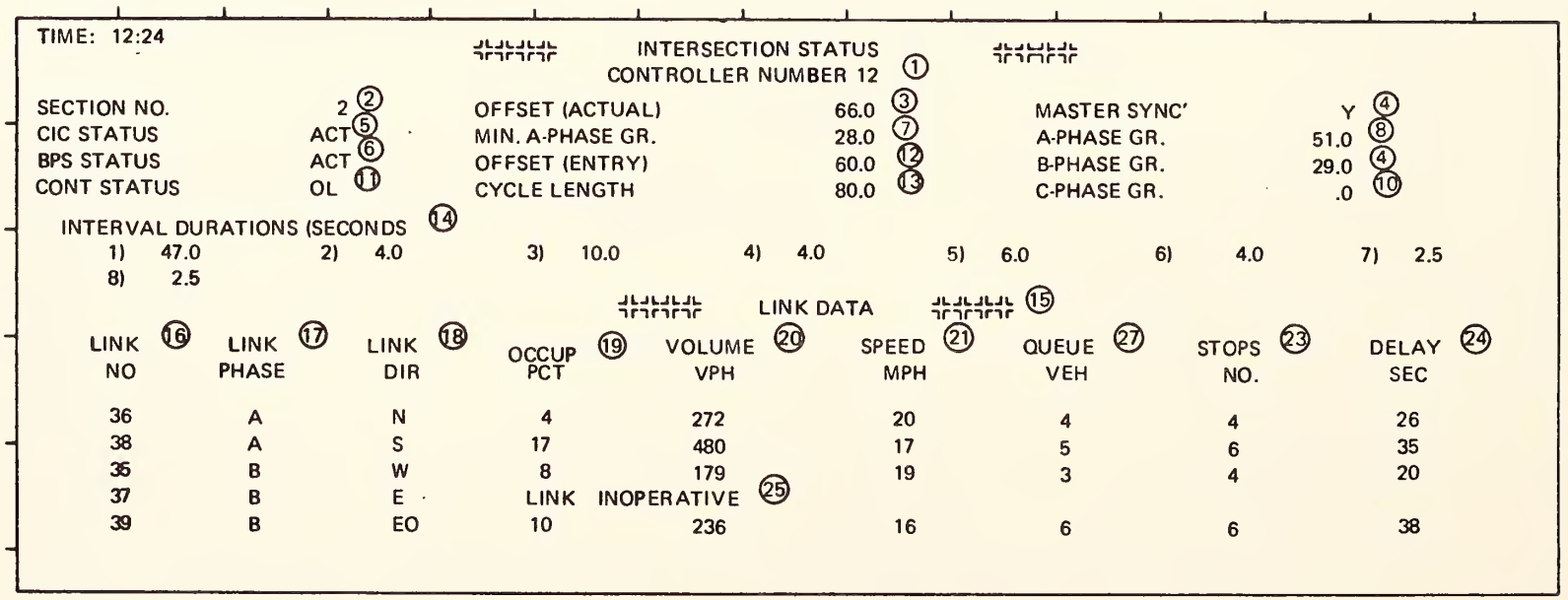


FIGURE 2.12.2.6. INTERSECTION STATUS FORMAT

(1) CONTROLLER NUMBER (INTRNUM)
LEGEND ABBREVIATION: I

(2) SECTION NUMBER (CONSEC(I))

(3) ACTUAL OFFSET (CUROFF(I))

(4) MASTER SYNC - SET TO "Y" IF BACKGROUND CYCLE CORRESPONDING TO CONTROLLERS' CYCLE LENGTH IS SYNCHRONIZED WITH COMPUTER CLOCK. BIT NO. CYCLC(I) OF KCTF = 1. OTHERWISE SET TO "N"

(5) C.I.C. STATUS:

STATUS	IF BIT I OF:
REL	CICSF = 0
INH	CICSF = 1, CICEF = 0
ACT	CICEF = 1, CICTF = 0
THLD	CICTF = 1
NI	CICSYS = 0

(6) BPS STATUS:

STATUS	IF B CODE (I) = :
REL	2
INH	3
ACT	0
PRE	1
NI	4

(7) MINIMUM A-PHASE GREEN DURATION: GMINABC4 (4•I)

(8) A-PHASE DURATION:
SUMABCT (4•I) + INTDUR (K)
WHERE K = 16•I + VARINT (4•I)

(9) B-PHASE DURATION:
SUMABCT (4•I + 1) + INTDUR(K)
WHERE K = 16•I + VARINT (4•I + 1)

(10) C-PHASE DURATION:
SUMABCT (4•I + 2) + INTDUR (K)
K = 16•I + VARINT (4•I + 2)

(11) CONTROLLER STATUS:

STATUS	IF BIT I, OF:
STBY	HOLD = 0
OL	HOLD = 1
FAIL	CMALF = 1

(12) ENTRY OFFSET: (ENTRYOFF (I))

(13) CYCLE LENGTH: KCL(K)
WHERE K = CYCLC (I)

(14) INTERVAL DURATIONS:
INTDUR (16•I + K) WHERE K RANGES FROM 0 TO A MAX OF 16. LAST INTERVAL IS DETERMINED BY A DURATION OF 0 IF LESS THAN 16 INTERVALS

(15) LINK DATA HEADER:
DISPLAYED AS SHOWN IN NORMAL OPERATIONS. IF CONTROLLER IS IN A TRANSITIONAL CYCLE, (MI (I) ≠ 0) HEADER IS REPLACED BY "CONTROLLER IN TRANSITION" AND THE LOWER SECTION OF THE PAGE IS BLANKED OUT.

(16) LINK NUMBER: LINK NUMBERS FROM CONTLN. FIRST LINK IS POINTED TO BY LSI(I) AND THE TERMINAL LINK NUMBER IS INDICATED BY THE NEXT SUCCEEDING POSITIVE VALUE OF LSI. IF LSI(I) = -1, CONTROLLER HAS NO LINKS, AND THE MESSAGE "NOT INSTRUMENTED" IS OUTPUTTED.
LEGEND ABBREVIATION: L

FIGURE 2.12.2.6. INTERSECTION STATUS FORMAT (Continued)

(17) LINK PHASE: (LNKPT(L) OR LINKPH(L))
CODES ARE:

0,1	=	A
2, 3	=	B
4	=	C
6	=	D

(18) LINK DIRECTION: (LINKDI(L))
CODES ARE:

0 = N = NORTH
1 = S = SOUTH
2 = E = EAST
3 = W = WEST
4 = NE = NORTHEAST
5 = NW = NORTHWEST
6 = SE = SOUTHEAST
7 = SW = SOUTHWEST
8 = EO = EAST OUTBOUND

(19) LINK OCCUPANCY: (AHCC(L)•100)

(20) LINK VOLUME = (VOL(L))

(21) LINK SPEED: (SBAR(L))

(22) QUEUE AT GREEN: (QBAR(L))

(23) NUMBER OF STOPS: (NSTOPS(L))

(24) DELAY (SEC/VEH): (DELAY (L)) UPDATED ON THE 15 MINUTE PERIOD BY RTN. H.

(25) MESSAGE OUTPUT WHEN A DETECTOR FAILURE ON THE LINK HAS OCCURRED

FIGURE 2.12.2.6. INTERSECTION STATUS FORMAT (Continued)

TIME: B:05

BPS SYSTEM STATUS – BY SECTION

SECTION	MODE ①	TIME ON ②	ACTIVE INTER. ③	FAILURES ④
1	ACT	1517	1	0
2	ACT	1517	3	1
3	ACT	1517	15	0
4	ACT	1517	2	0

BPS SYSTEM STATUS – BY INTERSECTION

10B ⑤	12I	17B	40I	42I	45I	49I	54B	55B	57B
59B	60I	66I	68B	70B	72B	73B	76B	77B	B2B
B4B	B5B	8BI	91B	93B	94P	97I	99I	115B	120X
121B	123B								

① BPS SECTION MODE: (BMODE)
CODES ARE:
0 = ACT = ACTIVE
2 = REL = RELEASED

② TIME ON: (BTIMEON)

③ ACTIVE BPS INTERSECTIONS: (NAI)
COMPUTED AT PREVIOUS DISPLAY OF THIS PAGE. NUMBER REPRESENTS THOSE INTERSECTIONS WHICH HAVE BEEN SELECTED FOR BPS AND ARE NOT INHIBITED. (BPSENB $\cap$ CICEF $\cap$ $\overline{\text{CICTF}}$)

④ BPS DETECTOR FAILURES: (NBFAIL)

⑤ INTERSECTION STATUS: (BCODE)
CODES ARE:
0 = B = ACTIVE BPS
1 = P = INTERSECTION PREEMPTED
2 = X = RELEASED
3 = I = INHIBITED

FIGURE 2.12.2.7. BPS SYSTEM STATUS DISPLAY

TIME: 10:12

BPS INTERSECTION NO. 82 (1)

ZONE NO (2)	DIREC. (3)	LOAD TIME SEC (4)	PSG LOAD (5)	EXT. SEC. (6)	PREEMPT EXT. (7)
45	N	20	30	10	OFF
46	S	20	30	10	OFF

BPS PERFORMANCE DATA

ZONE NO (2)	NUMBER CYCLES (8)	EXT. GNT. (9)	VOLUME (10) STOP	VOLUME (10) THRU	ELIGIBLE (11) STOP	ELIGIBLE (11) THRU	HELPED (12) STOP	HELPED (12) THRU	PSG-MIN SAVED (13)
45	6	3	4	7	2	5	2	4	93
46	6	2	2	2	1	2	1	1	27

(1) INTERSECTION NUMBER; (INTRNUM)
LEGEND ABBREVIATION: I

(2) ZONE NUMBER: ZONE NUMBERS FROM CONTZN. FIRST ZONE IS POINTED TO BY ZSI(I) AND TERMINAL ZONE BY ZSI(I+1).
LEGEND ABBREVIATION: Z

(3) ZONE DIRECTION: (ZONELNK AND LINKDI)

(4) PASSENGER LOAD TIME: (PLT(12Z+BLINDEX)) WHERE BLINDEX IS A FIXED INDEX COMPUTED IN THE BPS EXECUTIVE.

(5) BUS PASSENGER LOAD: (BL(12Z+BLINDEX))

(6) WORKING BUS EXTENSION: (TEW)

(7) ZONE PREEMPT: (PREMPFG)
0 = OFF
1 = ON

(8) NUMBER OF CYCLES: NUMBER OF CYCLE LENGTHS (KCL(CYCLC(I))) ELAPSED SINCE THE LAST 15 MINUTE MARK.

(9) EXTENSIONS GRANTED: (EG15)

(10) STOP/THRU BUS VOLUME: (SBV15, TBV15)

(11) STOP/THRU ELIGIBLE BUSES: (ESB15, ETB15)

(12) STOP/THRU HELPED BUSES: (HSB15, HTB15)

(13) PASSENGER MINUTES SAVED: (IG15)

FIGURE 2.12.2.8. BPS INTERSECTION STATUS DISPLAY

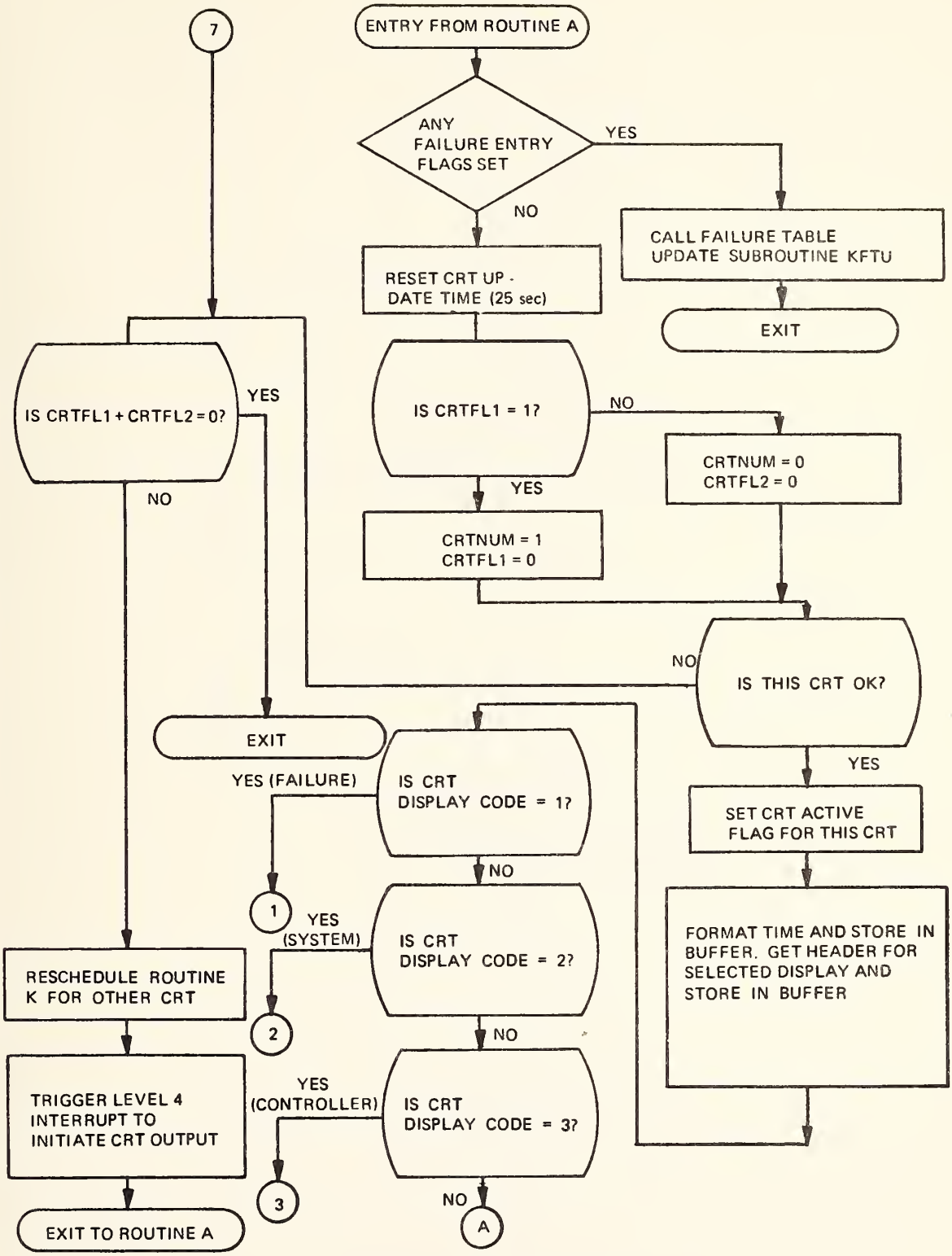


FIGURE 2.12.5.1. ROUTINE K

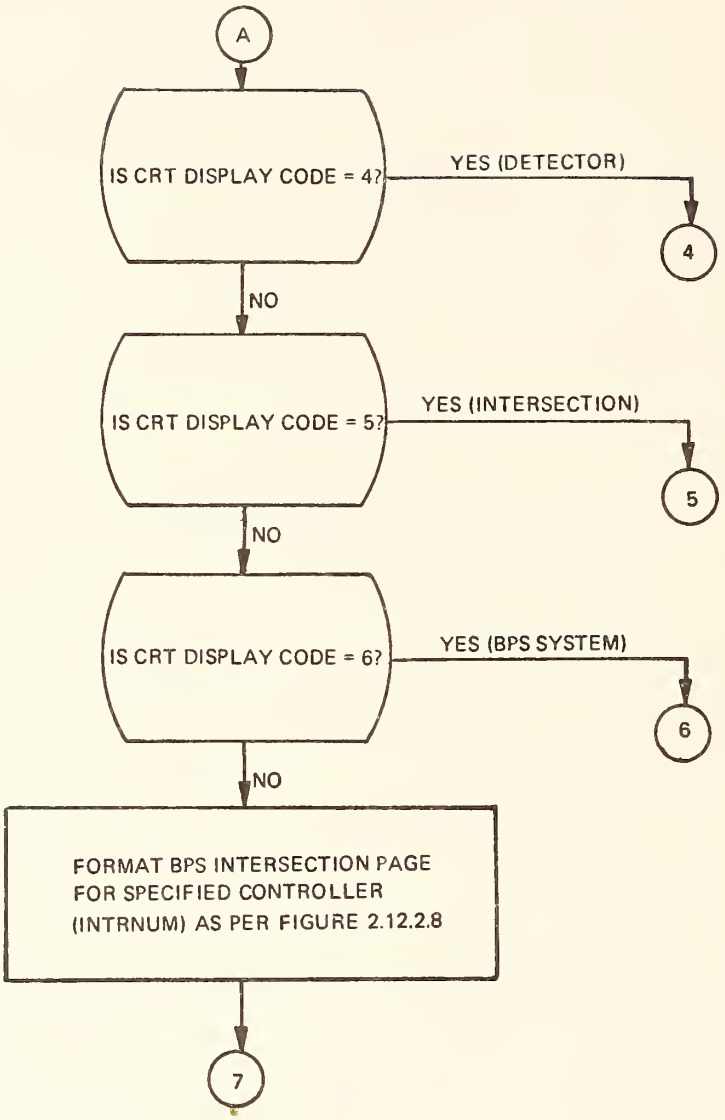


FIGURE 2.12.5.2. ROUTINE K

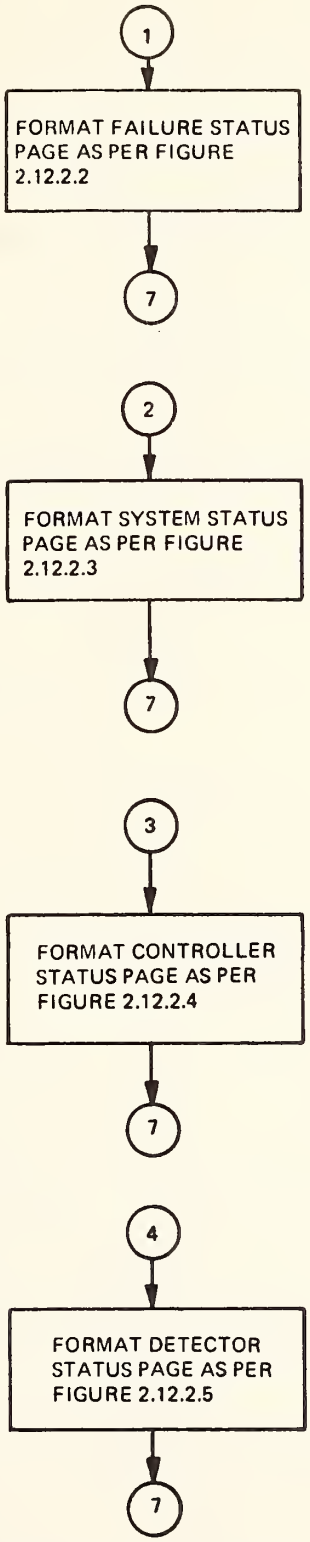


FIGURE 2.12.5.3. ROUTINE K

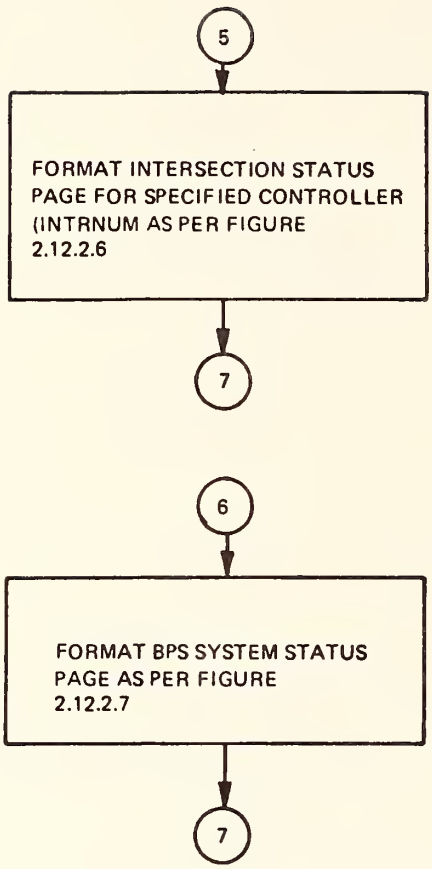


FIGURE 2.12.5.4. ROUTINE K

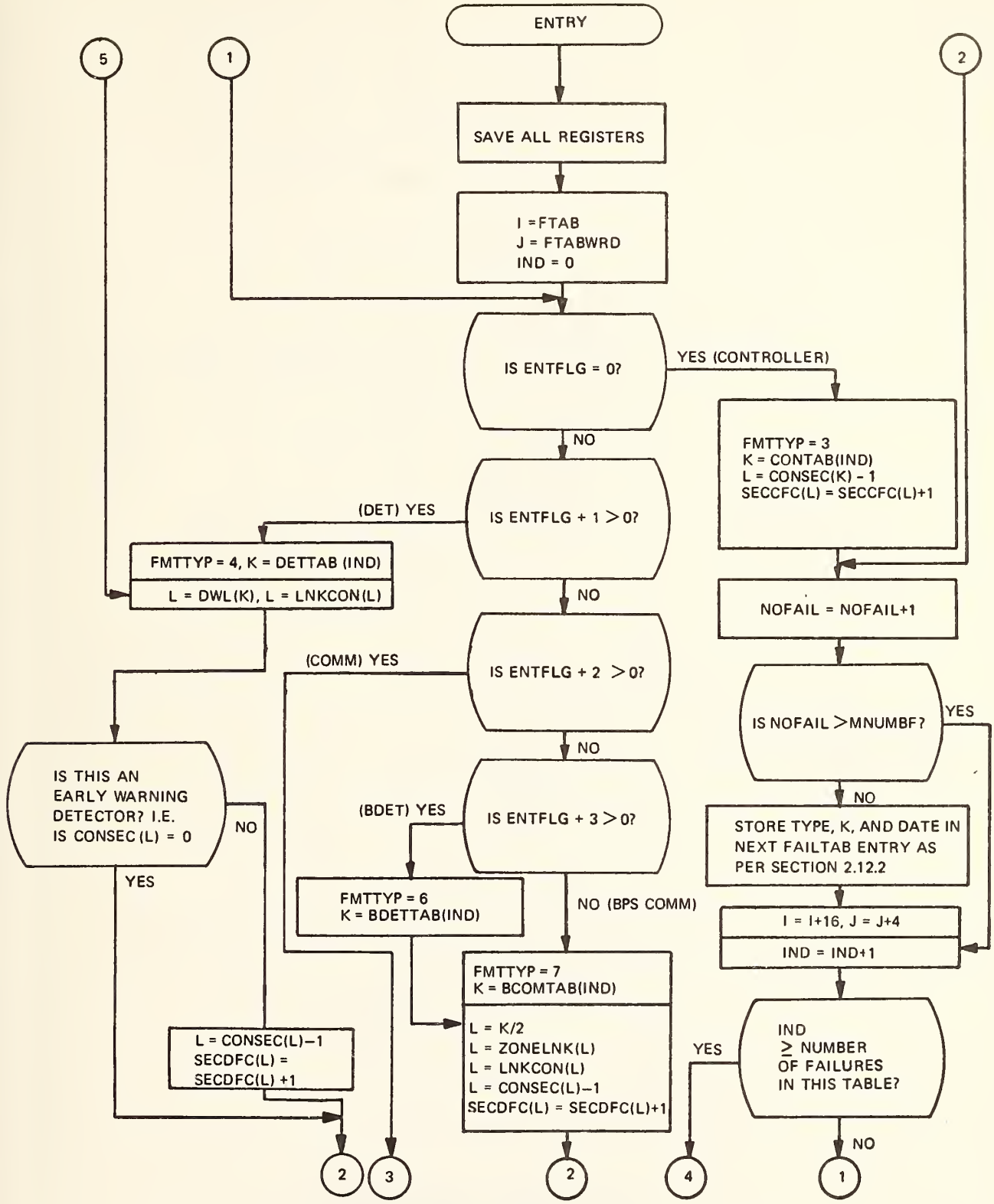


FIGURE 2.12.5.5. SUBROUTINE KFTU

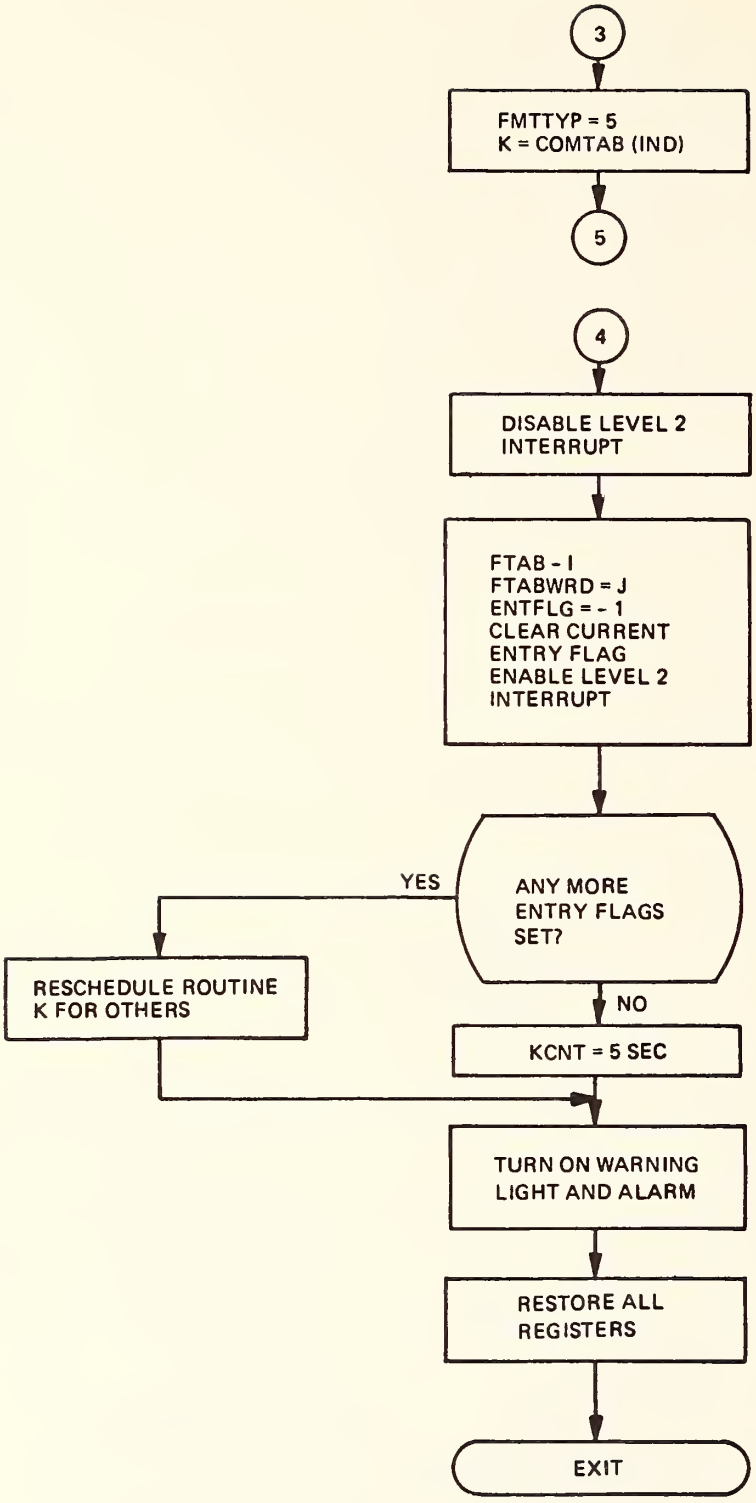


FIGURE 2.12.5.6. SUBROUTINE KFTU

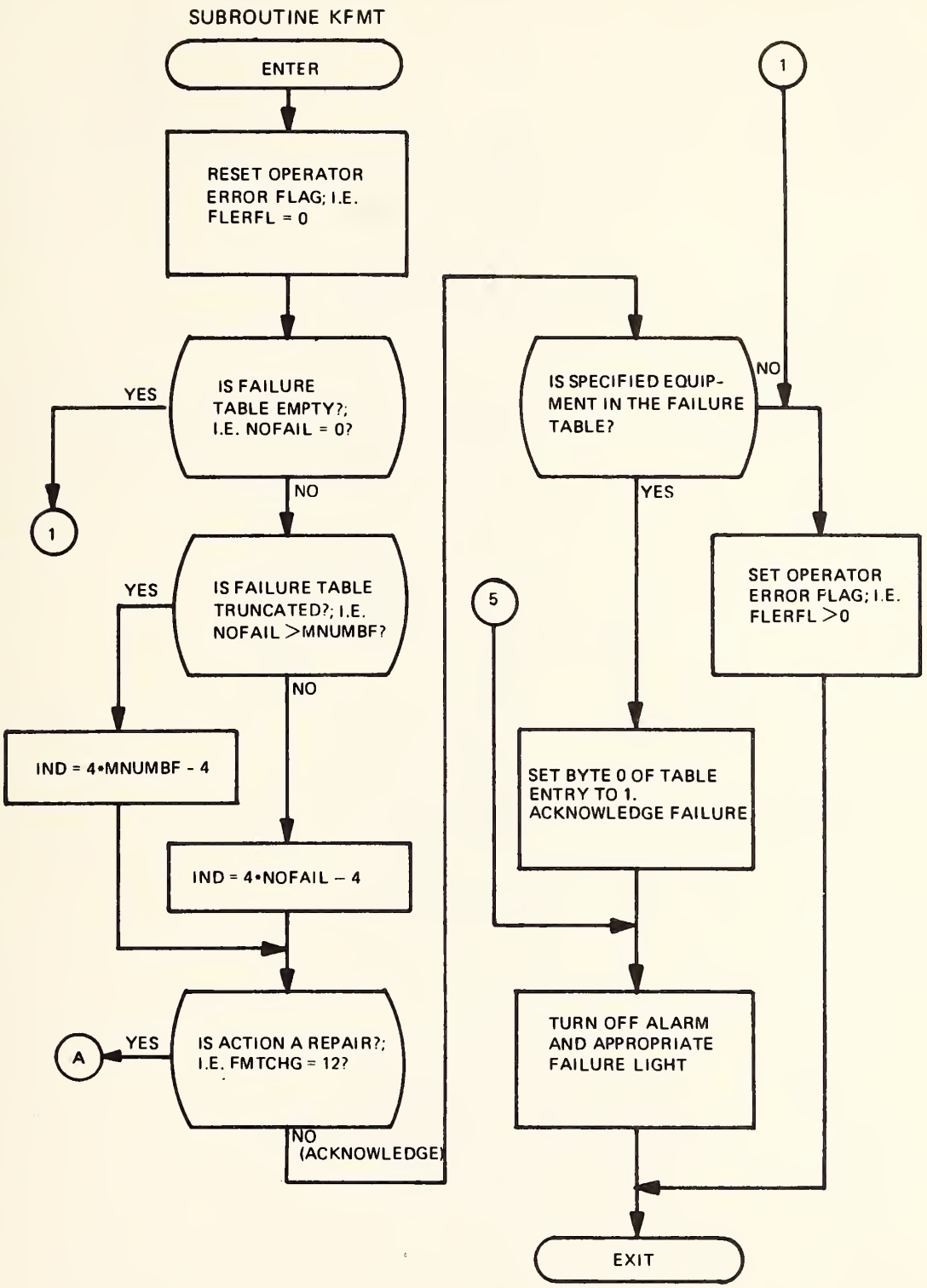


FIGURE 2.12.5.7. SUBROUTINE KFMT
FLOW CHART

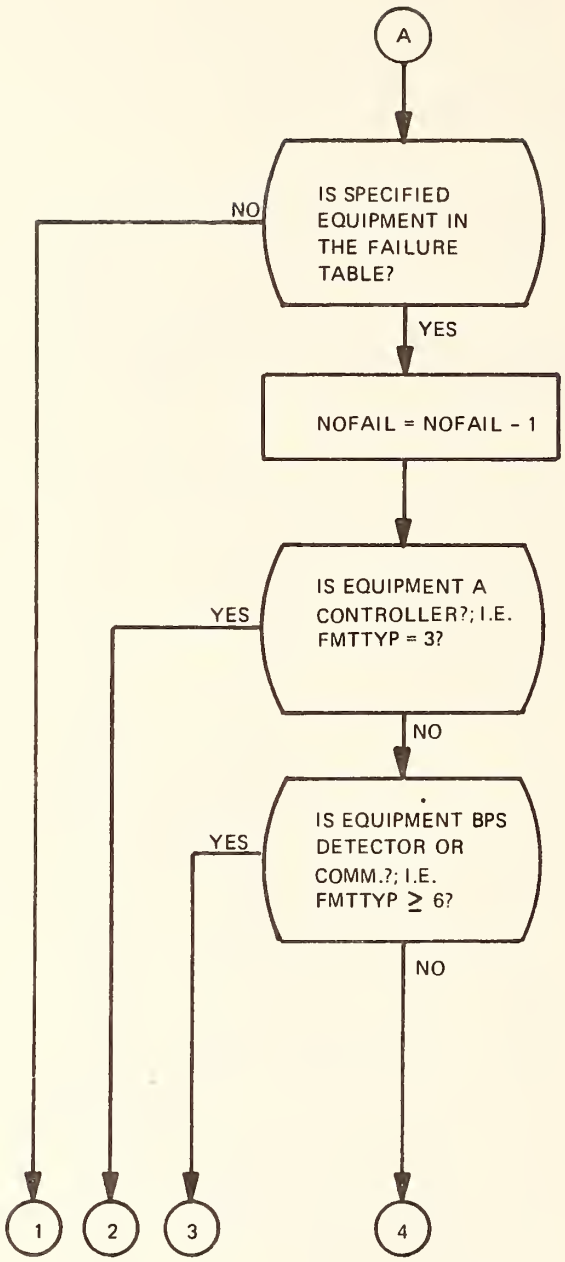


FIGURE 2.12.5.7. SUBROUTINE KFMT
FLOW CHART

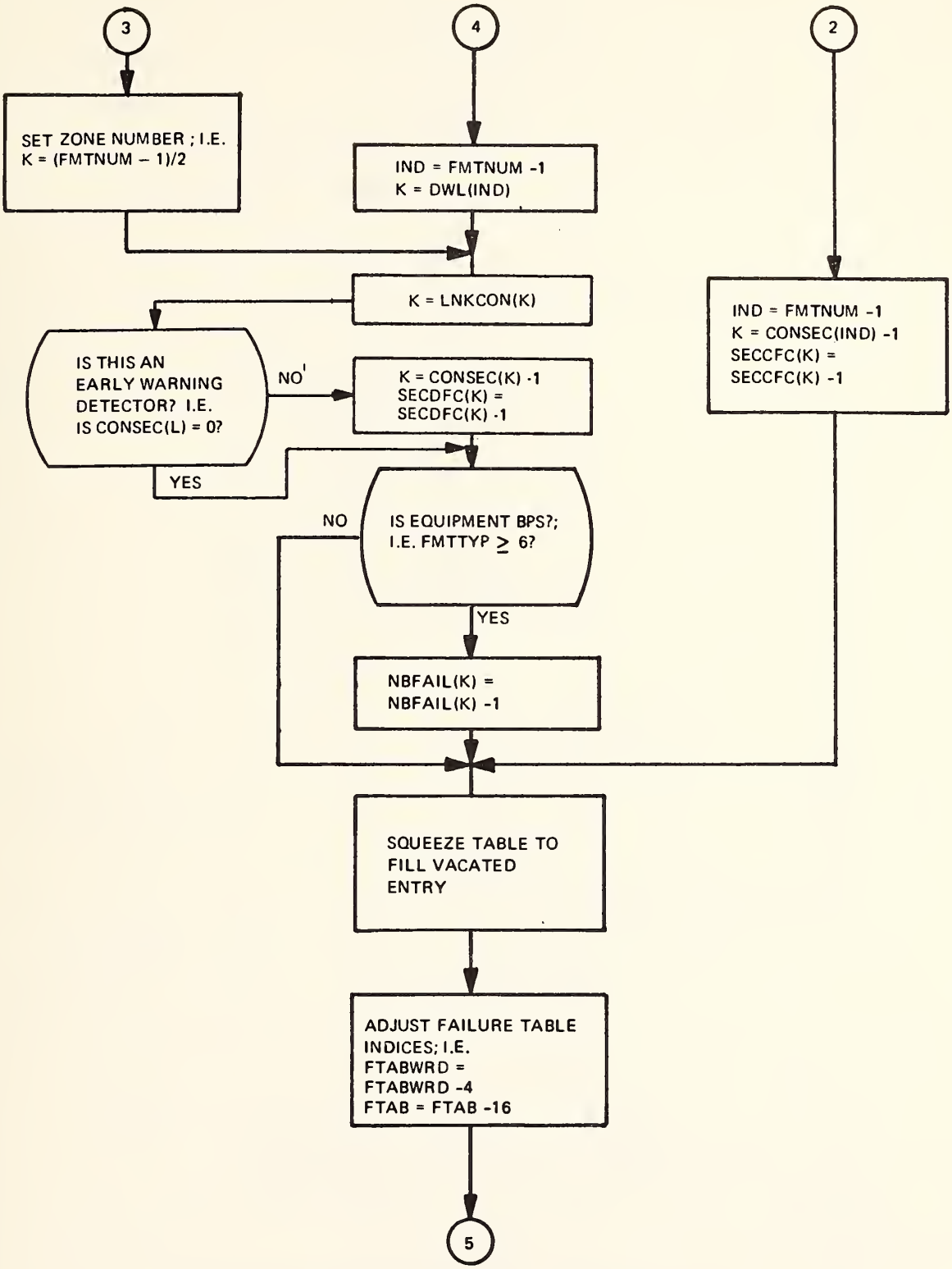


FIGURE 2.12.5.8. SUBROUTINE KFMT

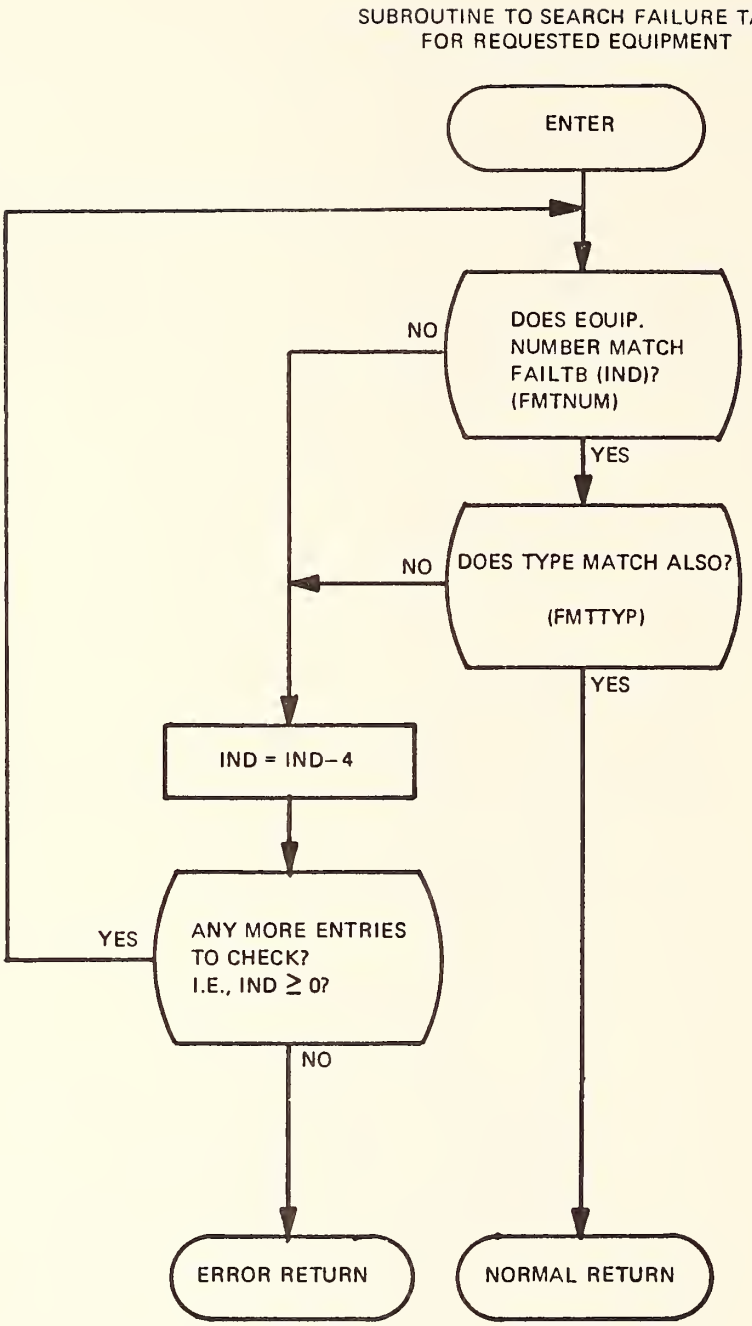


FIGURE 2.12.5.9. FAILURE TABLE SEARCH SUBROUTINE

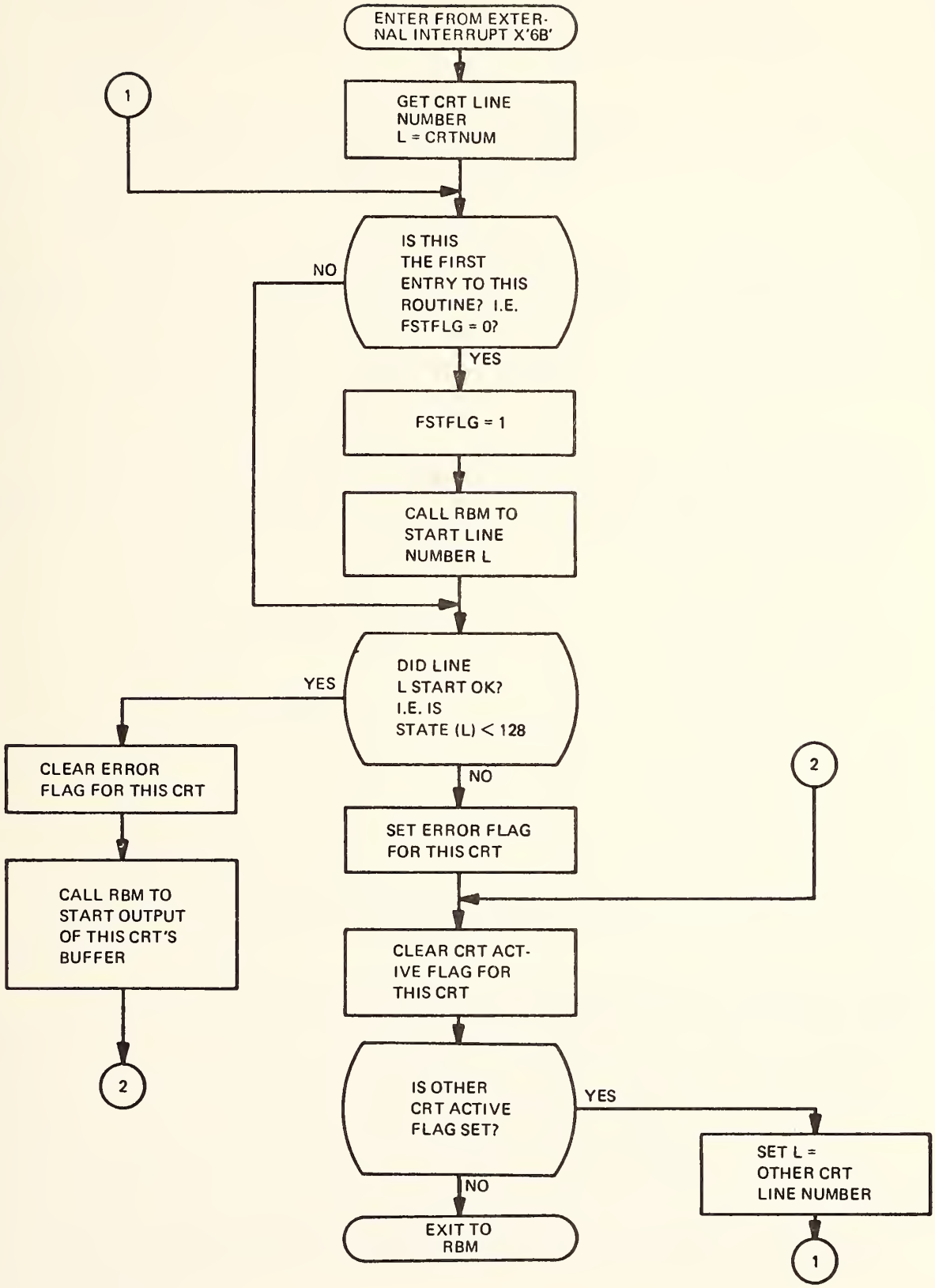


FIGURE 2.12.5.10 CRT OUTPUTTING ROUTINE

2.13 Routines L and BJ (Computer Performance Evaluation) Specifications

2.13.1 Purpose

The Computer Performance Evaluation Routine tests memory access and instruction operations of the UTCS Central Computer Processors for failures.

2.13.2 Method

The performance of the computer is evaluated by playing the two CPU's against one another. Each CPU performs the same set of operations on a shared data base. After the instruction repertoire has been executed, answers are compared. If there is an agreement, evaluation continues. If there is a discrepancy, the operator is notified and the system attempts a graceful shutdown.

The instruction repertoire is tested in three distinct sets. First, doubleword instructions are executed; second, halfword and byte instructions are tested; and finally whole word instructions are executed. The following is a list of operations performed:

- Load/store
- Fixed point arithmetic
- Comparisons
- Analyze and interpret
- Logical
- Shift
- Execute and branch

Push down, call, control, floating point arithmetic and Input/Output instructions are not tested by this routine.

Testing is controlled by both the UTCS Executive and the BPS evaluation routine as follows: The Executive initially sets the one minute flag (WMINF) to schedule Routine BJ in BPS. If BPS is up, Routine BJ clears WMINF, sets up a dynamic data base, executes the repertoire and schedules Routine L in UTCS. Routine L then performs the same calculations, compares the answers and takes the necessary action. If BPS is not up, the Exec senses WMINF has not been cleared when the next scheduling mark comes. It then sets CPFLG and enters the single computer evaluation mode. Once this mode is engaged it is maintained (regardless of the state of the BFS computer) until the entire system is restarted at startup.

2.13.3 Repetition Rate

This routine is entered every 1/2 second.

2.13.4 Cross Reference

This routine is called at 1/2 second intervals by the Executive Routine as part of the Level 2 routines. It exits to the Executive Routine, Routine A.

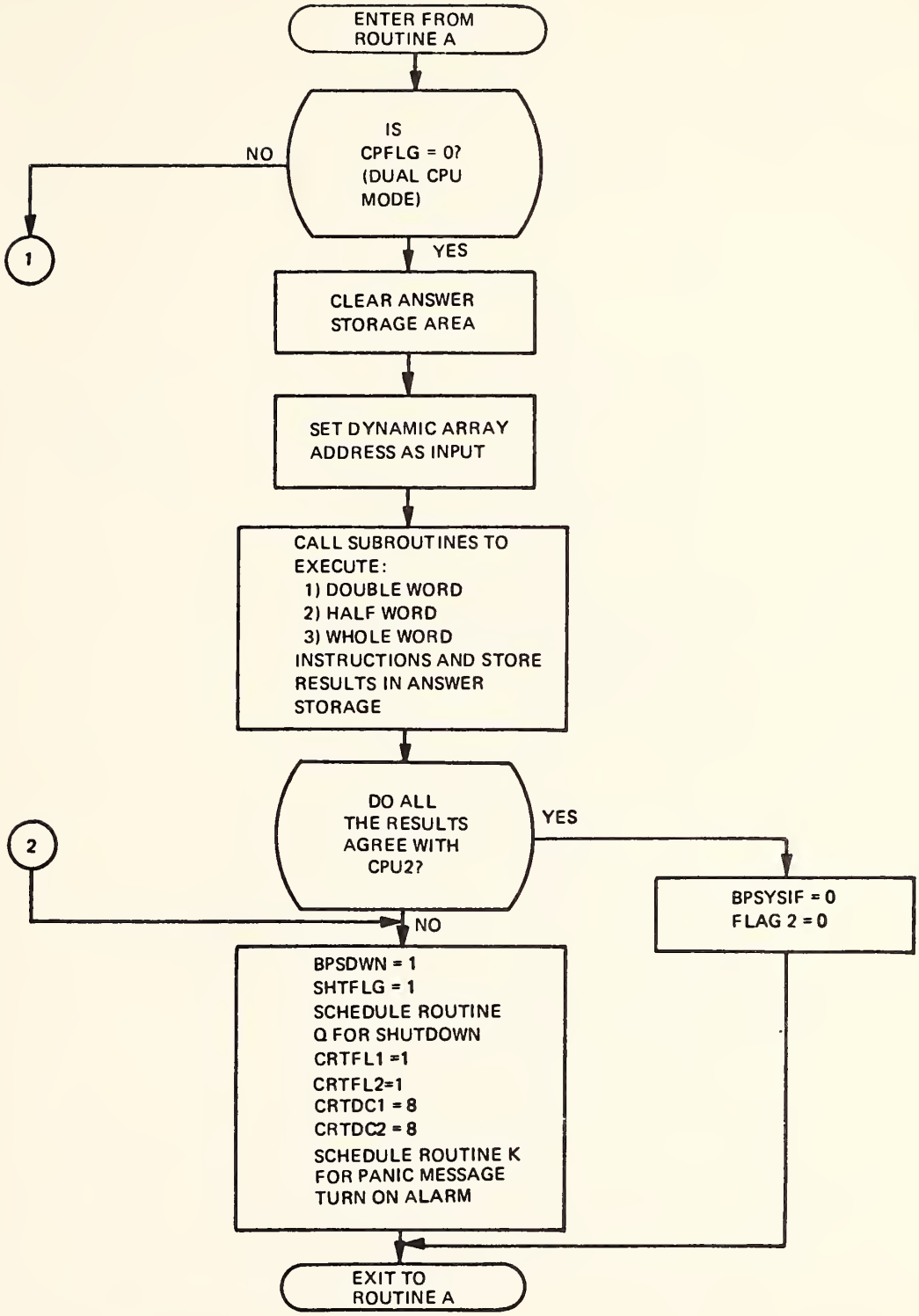


FIGURE 2.13.5.1. ROUTINE L SPECIFICATION

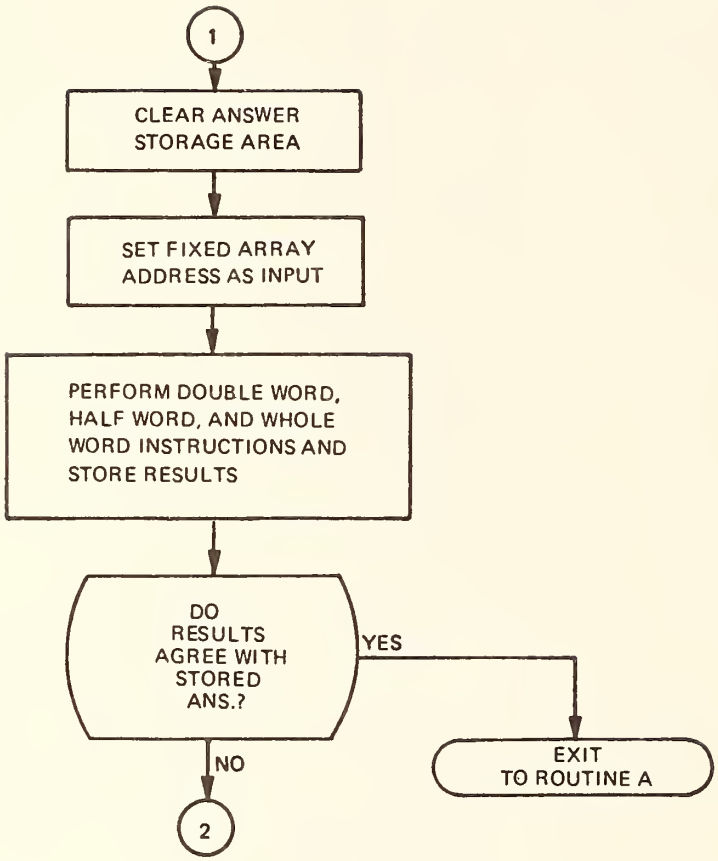


FIGURE 2.13.5.2. ROUTINE L SPECIFICATION

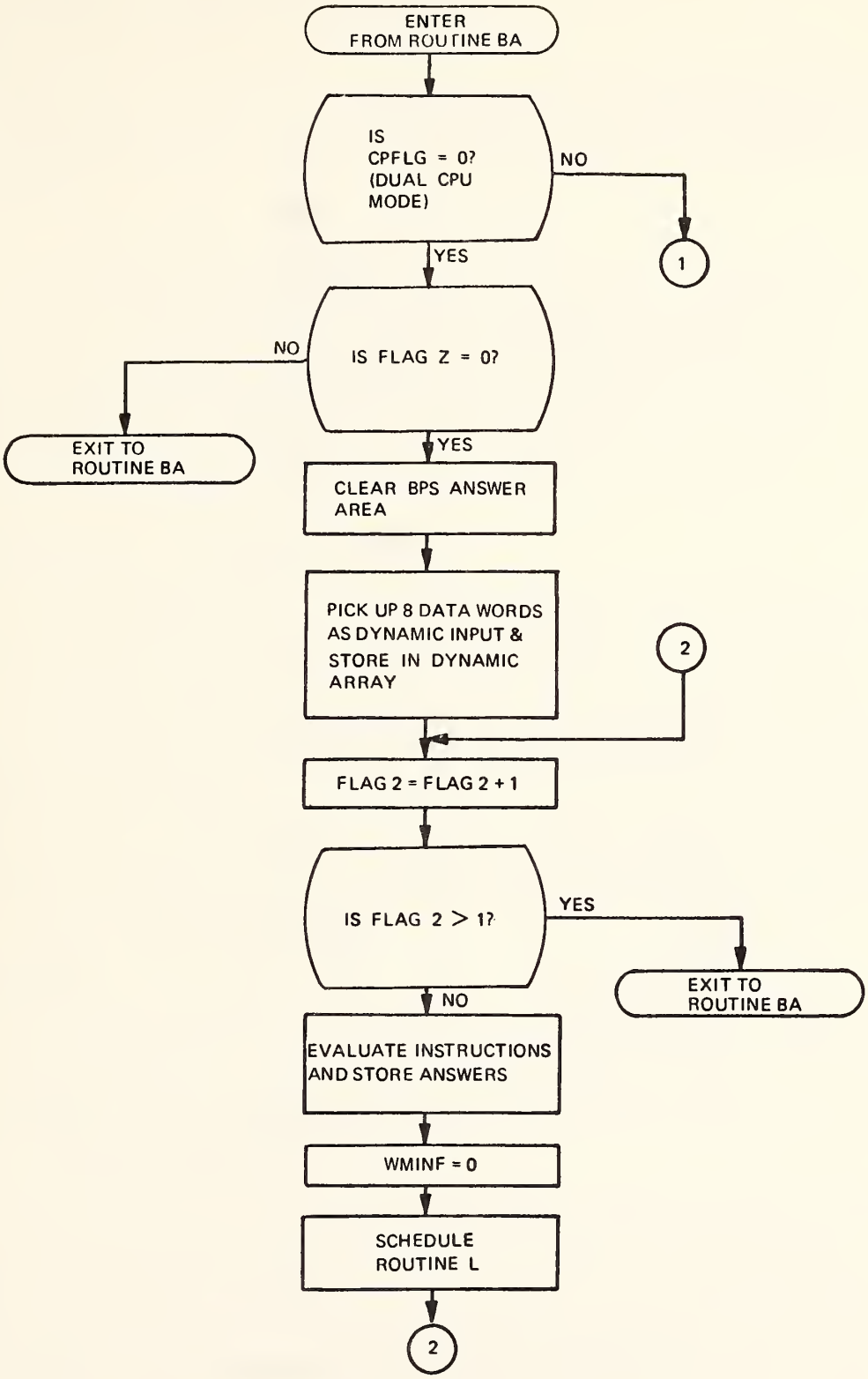


FIGURE 2.13.5.3. ROUTINE BJ SPECIFICATION

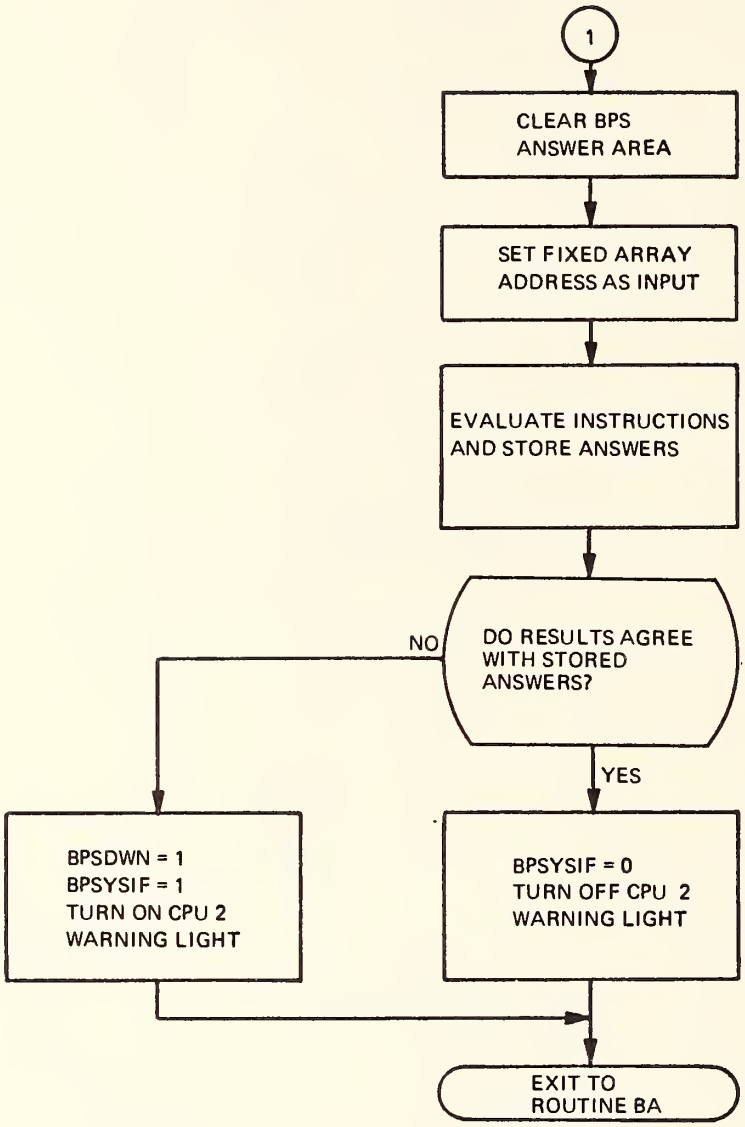


FIGURE 2.13.5.4. ROUTINE BJ SPECIFICATION

2.14 Routine M (Manual Control Panel) Specification

2.14.1 Purpose

The Manual Control Panel Processing Routine evaluates the control panel inputs for reasonableness and stores the data and flags required by other routines to perform the requested operations.

2.14.2 Method

Upon entry, Routine M resets the first five bits of the control panel output word (CPANOUT) (FIG. 2.14.5.1). A check is made of the SUPPRESS PRINTOUT button (CPANIN, WORD2, BIT 10) (FIG. 2.14.5.2) and if it is set, Routine M sets the 15-minute report flag (PRTFLG). If it is not set Routine M resets the 15-minute report flag. Next a check is performed to see if any of the enter bits (CPANIN, WORD1, BITS 0-2) are set. If none are set, Routine M exits.

SYSTEM ENTER

If the system enter bit (CPANIN, WORD1, BIT 0) is set, the system ready bit of the control panel output word (CPANOUT, BIT 0) is set. The shutdown flag (SHTFLG) is checked. If it is set, the error exit is taken. This prevents system entries during shutdown. At the error exit the system error bit of the control panel output word (CPANOUT, BIT 3) is set. If the shutdown flag is not set, a check is made to see if this is a shutdown request (CPANIN, WORD2, BIT 1). If it is, the shutdown flag is set, Routine H is scheduled and Routine M exits. If it is not shutdown, the bus priority bit (CPANIN, WORD3, BIT 2) traffic control bit (CPANIN, WORD3, BIT 0), and CIC bit (CPANIN, WORD3, BIT 1) are checked If none are set, Routine M takes the error exit.

BUS PRIORITY

The system bit (CPANIN, WORD3, BIT 3), the section bit (CPANIN, WORD3, BIT 4), the controller bit (CPANIN, WORD3, BIT 5), the bus zone bit (CPANIN, WORD2, BIT 0), the detector bit (CPANIN, WORD3, BIT 6), and the communications bit (CPANIN, WORD3, BIT 7) are checked and if none are set Routine M takes the error exit.

If the system bit is set, the pre-empt on bit (CPANIN, WORD2, BIT 2) is checked. If it is set, the BPS pre-empt flag array (PREMPFG) is set and the BPS enable flags (BPSENB) are set for all BPS controllers that have not failed. The BPS system status mode (BMODE) is set to 1 (pre-empt on) and the time of present mode (BTIMEON) is set to time of day (TOD). The change table formatting routine (HFMT - see Routine H for description) is called to log the change and Routine M exits. If the pre-empt on bit is not

set, the pre-empt off bit (CPANIN, WORD2, BIT 3) is checked. If it is set the BPS pre-empt flag array (PREMPFG) is cleared. The BPS system status mode (BMODE) is set to 0 (BPS on) and the time of the present mode (BTIMEON) is set to time of day (TOD). The change table formatting routine (HFMT) is called to log the change and Routine M exits. If the pre-empt off bit is not set, the system activate bit (CPANIN, WORD3, BIT 10) is checked. If it is set, the BPS start-up flag (BPSSIF) is checked to see if this is the first time. If it is set, the flag is cleared and the time of the present mode (BTIMEON) is entered with the time of day (TOD) and Routine M exits. If it is not the first time, all the BPS enable flags (BPSENB) are set for all BPS controllers that have not failed. The BPS system status mode (BMODE) is set to 0 (BPS on) and the time of the present mode (BTIMEON) is set to time of day (TOD). The change table formatting routine (HFMT) is called to log the change and Routine M exits. If the system activate bit is not set, the system release bit (CPANIN, WORD3, BIT 11) is checked. If it is not set, Routine M takes the error exit. If it is set, the BPS enable flag array (BPSENB) is cleared, the BPS system status mode (BMODE) is set to 2 (BPS off) and the time of the present mode (BTIMEON) is set to the time of day. The change table formatting routine (HFMT) is called to log the change and Routine M exits.

If the section bit is set, the section number is obtained from CPANIN, WORD3, BITS 16-31. If too large a number is inserted, Routine M takes the error exit. The activate bit (CPANIN, WORD3, BIT 10) is then checked. If it set, the BPS system status (BMODE) is set for this section to 0 (BPS on) and the time of the present mode (BTIMEON) is set for this section to the time of day (TOD). The BPS enable flags (BPSENB) are set for each BPS controller in the section that have not failed. The change table formatting routine (HFMT) is called to log the change and Routine M exits. If the activate bit is not set, the release bit (CPANIN, WORD3, BIT 11) is checked. If it is not set, Routine M takes the error exit. If it is set, the BPS system status (BMODE) is set to 2 (BPS off) for this section and the time of the present mode (BTIMEON) is set to the time of day (TOD) for this section. The BPS enable flags (BPSENB) are cleared for each BPS controller in the section that have not failed. The change table formatting routine (HFMT) is called to log the change and Routine M exits.

If the controller bit is set, the controller number is obtained from CPANIN, WORD3, BITS 16 - 31. If too large a number is inserted, Routine M takes the error exit. It also takes the error exit if the controller is not instrumented (BCODE $\neq$ 0), if it is not a BPS controller, if the operator has not selected activate (CPANIN WORD 3 BIT 10) or release (CPANIN, WORD3, BIT 11), or if the operator is trying to activate a failed controller. If the

activate bit is set and the controller has not failed, the CIC selected flag (CICSF) and the BPS enable flag (BPSENB) for this controller are set. If the release bit is set, the BPS enable flag (BPSENB) is reset for the controller. The change table formating routine enable flag (BPSENB) is reset for the controller. The change table formatting routine (HFMT) is called to log the change and Routine M exits.

If the bus zone bit is set, the bus zone number is obtained from CPANIN, WORD3, BITS 16 - 31 and the extension is obtained from CPANIN, WORD4, BITS 4 - 15. Routine M takes the error exit if the bus zone number is too large, if the pre-empt on bit (CPANIN WORD2, BIT 2), pre-empt off bit (CPANIN, WORD2, BIT 3) or time extension bit (CPANIN, WORD4, BIT 3) are not set, or if the inserted extension is greater than the max (TEWM). If the pre-empt on bit is set, the pre-empt flag (PREMPFG) for this zone is set. If the pre-empt off bit is set, the pre-empt flag (PREMPFG) for this zone is reset. If the time extension bit is set, the time is placed into TEW for this zone. The change table formatting routine (HFMT) is called to log the change and Routine M exits.

If the detector bit or communication bit is set, the detector number is obtained from CPANIN, WORD3, BITS 16 - 31. Routine M takes the error exit if the detector number inserted is too large, if the acknowledge failure bit (CPANIN, WORD3, BIT 13) or the failure repair bit (CPANIN, WORD3, BIT 15), is not set, or if the detector is not listed in the failure table (FAILTAB). If the acknowledge failure bit is set, the acknowledge/repair failure table routine (KFMT) is called to log the acknowledge. If the failure is not in the table FLERFL is set and Routine M takes the error exit. If the repair failure bit is set, the acknowledge/repair failure table routine (KFMT) is called to log the repair. Again if the failure is not in the table, FLERFL is set and Routine M takes the error exit. After a repair BPS failure flags (BPSCFF, BPSCFFL for communications and BPSDFF, BPSDFFL for detector) are cleared. A check is performed to see if there are any other failed detectors on the same zone. If not the corresponding BPS intersection failure flag (BPSIFF) is cleared. The change table formatting routine (HFMT) is called to log the change and Routine M exits.

TRAFFIC CONTROL

The system bit (CPANIN, WORD3, BIT 3), the section bit (CPANIN, WORD3, BIT 4), the controller bit (CPANIN, WORD3, Bit 5), the detector bit (CPANIN, WORD3, BIT 6), and the communications bit (CPANIN, WORD3, BIT 7) are checked. If none are set Routine M takes the error exit.

If the system bit is set, the on-line bit (CPANIN, WORD3, BIT 10) is checked. If it is set, the first start flag (FSTFLG) is checked and if set Routine M takes the error exit. If the flag is not set, it is now set, the 15-minute section flag (FMSECF) and the 15-minute system flag (FMSYSF) are set, and Routine W is scheduled. If the on-line bit is not set, FSTFLG is checked to see if it is set. If it isn't, Routine M takes the error exit. If the flag is set, the traffic responsive bit (CPANIN, WORD3, BIT 8) is checked and if set the 15-minute section flag (FMSECF) is checked. If the flag is set, the wait bit of the control panel output word (CPANOUT, BIT 5) is set and Routine M exits. If the flag is not set, the mode change desired flags (MCDF) are set for all sections and the desired mode flags (DMODE) are set to traffic responsive for all sections. If the traffic responsive bit is not set, the time of day bit (CPANIN, WORD3, BIT 9) is checked and if it is set the 15-minute section flag (FMSECF) is checked. If the flag is set, the wait bit of the control panel output word (CPANOUT, BIT 5) is set and Routine M exits. If the flag is not set, the single section flag (SSFW) is reset, the mode change desired flags (MCDF) are set for all sections, the desired mode flags (DMODE) are set to time of day for all sections, the 15-minute section flag (FMSECF) is set, the section number (JJ) is set to zero and Routine W is scheduled. If the time of day bit is not set, the standby bit (CPANIN, WORD3, BIT 11) is checked and if set the mode (MODES) and desired mode flags (DMODE) are set to standby for all sections, the automatic control desired flags (AUTOF) are reset for all controllers, the standby desired flags (STBYD) and BPS inhibit flags (BPSIF) are set for all controllers. If the standby bit is not set, the record history on bit (CPANIN, WORD3, BIT 12) is checked and if set the record history flag (HRF) is set. If the record history on bit is not set, the record history off bit (CPANIN, WORD3, BIT 14) is checked and if set the record history flag (HRF) is cleared. If none of the bits are set, Routine M takes the error exit. The change table formatting routine (HFMT) is called to log the change and Routine M exits.

If the section bit is set, the first start flag (FSTFLG) is checked and if not set Routine M takes the error exit. If the flag is set, the section number is obtained from CPANIN, WORD3, BITS 16 - 31. If the section number is greater than the number of sections in the system (NUMSCT), Routine M takes the error exit. The traffic responsive bit is checked (CPANIN, WORD3, BIT 8) and if it is set the 15-minute section flag (FMSECF) is checked. If the flag is set, the wait bit of the control panel output word (CPANOUT, BIT 5) is set and Routine M exits. If the flag is not set, the mode change desired flags (MCDF) are set for the section and the desired mode flags (DMODE) are set to traffic responsive for the section. If the traffic responsive bit is not set, the time of day bit (CPANIN, WORD3, BIT 9)

is checked and if it is set the 15-minute section flag (FMSECF) is checked. If the flag is set, the wait bit of the control panel output word (CPANOUT, BIT 5) is set and Routine M exits. If the flag is not set, the single section flag (SSFW) is set, the mode change desired flags (MCDF) are set for the section, the desired mode flags (DMODE) are set to time of day for the section, the 15-minute section flag (FMSECF) is set, the section number (JJ) is set equal to the inputted section number minus 1, and Routine W is scheduled. If the time of day bit is not set, the manual pattern bit (CPANIN, WORD4, BIT 0) is checked and if it is set the pattern number is obtained from CPANIN, WORD4, BITS 4 - 15. A check is made to see if this is a valid pattern number for this time of day. If it isn't Routine M takes the error exit. If it is the 15-minute section flag (FMSECF) is checked. If the flag is set, the wait bit of the control panel output word (CPANOUT, BIT 5) is set and Routine M exits. If the flag is not set, the mode change desired flags (MCDF) is set for this section, the desired mode flags (DMODE) are set to manual pattern for this section, the desired pattern number (DPATNUM) is set equal to the inputted pattern number minus one, the 15-minute section flag (FMSECF) is set, the section number (JJ) is set equal to the inputted section number minus 1, and Routine W is scheduled. If the manual pattern bit is not set, the standby bit (CPANIN, WORD3, BIT 11) is checked and if it is set the mode (MODES) and desired mode flags (DMODE) are set to standby for this section, the automatic control desired flags (AUTOF) are reset for all controllers in section and the standby desired flags (STBYD) are set for all controllers in section. If none of the bits are set, Routine M takes the error exit. The change table formatting routine (HFMT) is called to log the change and Routine M exits.

If the controller bit is set, the controller number is obtained from CPANIN, WORD3, BITS 16-31. If the inserted number is greater than the number of controllers in the system (NUMCTL), Routine M takes the error exit. The failure repair bit (CPANIN, WORD3, BIT 15) is checked and if it is set the acknowledge/repair failure table routine (KFMT) is called to log the repair. If the failure is not in the table (FAILTAB), Routine M takes the error exit. After the repair is logged, the controller malfunction flag (CMALF) is cleared for this controller. If the failure repair bit is not set, the first start flag (FSTFLG) is checked. If the flag is not set, Routine M takes the error exit. If the flag is set, the on-line bit (CPANIN, WORD3, BIT 10) is checked and if it is set the section containing this controller is checked to see if the section is in standby. If it is, Routine M takes the error exit. Next a check is performed to see if this controller's malfunction flag (CMALF) is set. Again Routine M takes the error exit if the flag is set. Finally a check is made to see if the controller is in standby (HOLD) and if it is not Routine M takes the error exit. If all the tests

are passed, the automatic desired flag (AUTOF) for this controller is set. If the on-line bit is not set, the standby bit (CPANIN, WORD3, BIT 11) is checked and if it is set the standby desired flag (STBYD) is set for this controller and the automatic desired flag (AUTOF) is reset for this controller. If the on-line bit is not set, the failure acknowledge bit (CPANIN, WORD3, BIT 13) is checked and if this bit is set the acknowledge/repair failure table routine (KFMT) is called to log the acknowledge. If the failure is not in the failure table (FAILTAB), Routine M takes the error exit. If the failure acknowledge bit is not set the A-Phase Green bit (CPANIN, WORD4, BIT 1) is checked and if set the controller in standby flag (HOLD) is checked for this controller. If this controller is in standby, Routine M takes the error exit. If this controller is not in standby, a check is performed to see if it is currently operating as a CIC controller (CICEF = 1). If it is, Routine M takes the error exit. The request must wait if the controller is to be placed into transition (TRANSF = 1), is in transition (MI ≠ 0) or the 15-minute section flag (FMSECF) is set. If the request must wait, the wait bit of the control panel output word (CPANOUT BIT 5) is set and Routine M exits. If the request is to be handled now, the A-Phase Green is obtained from CPANIN WORD4, BITS 4-15. If the inserted A-Phase Green is less than the min (GMINABC4) allowed for this controller, Routine M takes the error exit. Using the inserted A-Phase Green a new B-Phase Green is computed, if this is less than the min (GMINABC4) allowed for this controller, Routine M takes the error exit. If the inserted value is good, the operator adjusted A-Phase Green (GAWTEMP) and the operator adjusted B-Phase Green (GBWTEMP) are stored for this controller. The operator split change flag (SPLCHG) is set for this controller. If the A-Phase Green bit is not set, the offset bit (CPANIN, WORD4, BIT 2) is checked and if it is set the controller in standby flag (HOLD) is checked for this controller. If this controller is in standby, Routine M takes the error exit. If the controller is not in standby, a check is performed (just like in the A-Phase Green case above) to see if the controller is in transition, about to be placed in transition or the 15-minute section flag (FMSECF) is set. If any of these conditions are met, the request must wait. The offset value is obtained from CPANIN, WORD4, BITS 4-15. If the inserted offset is greater or equal to the cycle length (KCL), Routine M takes the error exit. If it is a valid offset, it is stored as the working offset (WRKOFF) for this controller and the offset change flag (FSETCF) is set for this controller. If none of the bits are set, Routine M takes the error exit. The change table formatting routine (HFMT) is called to log the change and Routine M exits.

If the detector bit was set, the detector number is obtained from CPANIN, WORD3, BITS 16-31. If the detector number that is inserted is greater than the number of detectors in the

system (NUMVED), Routine M takes the error exit. If the inserted detector number is valid, the on-line bit (CPANIN, WORD3, BIT 10) is checked and if it is set the detector failure flag (DMALF) and the communications failure flag (MMALF) is checked for this detector. If either are set, Routine M takes the error exit. If the detector is operating, the detector standby flag (DIS) is cleared for this detector. If the on-line bit is not set, the standby bit (CPANIN, WORD3, BIT 11) is checked and if set the detector standby flag (DIS) is set for this detector. If the detector in standby bit is not set, the failure repair bit (CPANIN, WORD3, BIT 15) is checked and if set the acknowledge/repair failure table routine (KFMT) is called to log the repair. If the failure is not in the table (FAILTAB), Routine M takes the error exit. After the repair is logged, the detector failure flag (DMALF) is cleared for this detector. If the failure repair bit is not set, the failure acknowledge bit (CPANIN, WORD3, BIT 13) is checked and if it is set a check is made of the first start flag (FSTFLG). If this flag is not set, Routine M takes the error exit. If the flag is set, the acknowledge/repair failure table routine is called to log the acknowledge. If the failure is not in the table (FAILTAB), Routine M takes the error exit. If none of the bits are set, Routine M takes the error exit. The change table formatting routine (HFMT) is called to log the change and Routine M exits.

If the communications bit was set, the logic is exactly the same as for detector except that the only valid requests are for failure repair and failure acknowledged, and on a failure repair the corresponding communications failure flag (CMMALF) is cleared.

CIC

The system bit (CPANIN, WORD3, BIT 3), the section bit (CPANIN, WORD3, BIT 4), and the controller bit (CPANIN, WORD3, BIT 5) are checked and if none are set Routine M takes the error exit.

If the system bit is set, the activate bit (CPANIN, WORD3, BIT 10) is checked and if it is set the CIC selected flags (CICSF) are set for all CIC controllers in the system (CICSYS). If the activate bit is not set, the release bit (CPANIN, WORD3, BIT 11) is checked and if it is set all the CIC selected flags (CICSF) are cleared for all CIC controllers in the system (CICSYS). If none of the bits are set, Routine M takes the error exit. The change table formatting routine (HFMT) is called to log the change.

If the section bit is set, the section number is obtained from CPANIN, WORD3, BITS 16-31. If the inserted number is greater than the max number of sections (NUMSEC), Routine M takes the error exit. If the inserted section number is valid, the activate bit

and release bit are checked and processed just as in system entry, except now the CIC selected flags (CICSF) are processed only for the section.

If the controller bit is set, the controller number is obtained from CPANIN WORD 3, BITS 16-31. If the inserted number is greater than the max number of controllers (NUMCTL), Routine M takes the error exit. If the inserted number is valid, the activate bit (CPANIN, WORD3, BIT 10) is checked and if it is set the possible CIC flag (CICSYS) associated with controller is checked. If this is not a CIC controller, Routine M takes the error exit. If it is a CIC controller, the CIC selected flag (CICSF) associated with this controller is set. If the activate bit is not set, the release bit (CPANIN, WORD3, BIT 11) is checked and if set the CIC selected flag (CICSF) associated with this controller is cleared. If none of the bits are set, Routine M takes the error exit. The change table formatting routine (HFMT) is called to log the changes.

MAP ENTER

If the map enter bit (CPANIN, WORD1, BIT 1) is set, the map ready bit of the control panel output word (CPANOUT, BIT 1) is set. Routine M then begins to format the inputs from the control panel and stores them away for Routine J (Map Control Routine). The controller display code (CONDIS) is set for Routine J. If the A-Phase Green bit (CPANIN, WORD1, BIT 12) is set, then CONDIS = 0 (CONTROLLER DISPLAY ON). If the controller display off bit (CPANIN, WORD1, BIT 15) is set, then CONDIS = 1 (CONTROLLER DISPLAY OFF). Next the surveillance off bit (CPANIN, WORD1, BIT 11 is checked and if it is set the surveillance display code (SURDIS) is set to zero (SURVEILLANCE OFF) for Routine J.

After checking the three bits mentioned above and making changes to CONDIS and SURDIS, if necessary, the traffic control bit (CPANIN, WORD1, BIT 5), the BPS bit (CPANIN, WORD1, BIT 7), the CIC bit (CPANIN, WORD1, BIT 6), and the controller status bit (CPANIN, WORD1, BIT 13) are checked. If none of the bits are set, Routine J is scheduled and Routine M exits.

If the traffic control bit is set, the flow data bit (CPANIN, WORD1, BIT 8) is checked and if set the flow parameter is found by checking bits 16-21 of CPANIN, WORD1. The selected threshold is obtained from CPANIN, WORD1, BITS 22-31. A corresponding threshold value is obtained from a fixed internal table (THRVAL) and stored into the flow data threshold array (THRESH) for Routine J. The flow parameter code is stored into the flow data parameter code array (PARCOD) for Routine J. These codes are:

0 - Occupancy

1 - Volume

2 - Queue

3 - Stops

4 - Speed

5 - Delay

The surveillance display code (SURDIS) is set to 3 (FLOW DATA). Next the controller status bit (CPANIN, WORD1, BIT 13) is checked and if set the controller display code (CONDIS) is set to 2 (CONTROLLER STATUS). If the controller status bit is not set, the failed bit (CPANIN, WORD1, BIT 14) is checked and if set the controller display code (CONDIS) is set to 3 (CONTROLLERS FAILED). Routine J is scheduled and the Routine M exits.

If the flow data bit is not set, it is not necessary to look for flow data parameters and threshold values. Instead the equipment failed bit (CPANIN, WORD1, BIT 10) is checked and if set the surveillance display code (SURDIS) is set to 1 (TCS EQUIPMENT FAILED). Next the program checks the controller status bit and proceeds exactly as above when flow data was selected.

If the BPS bit is set, the logic is quite similar to the traffic control described above. The following are the only differences:

- Only two flow parameters may be chosen
  6 - passenger gain
  7 - buses helped
- If controller status is chosen, the controller display code (CONDIS) is set to 5 (BPS CONTROLLER STATUS).
- If controller status is not chosen, no further check is made to see if the failed bit is set.
- If the equipment failed is selected, the surveillance display code (SURDIS) is set to 2 (BPS EQUIPMENT FAILED).

If both CIC and controller status bits are set the controller display code (CONDIS) is set to 4 (CIC STATUS).

DISPLAY ENTER

If the display enter bit (CPANIN, WORD1, BIT 2) is set, the display ready bit of the control panel output word (CPANOUT, BIT 2) is set. A check is made to see which CRT has been selected. If neither, Routine M takes the error exit. At the error exit the display error

bit of the control panel output word (CPANOUT, BIT 4) is set. If CRT number 1 is chosen (CPANIN, WORD2, BIT 8), then the CRT number 1 flag (CRTFL1) is set. If CRT number 2 is chosen (CPANIN, WORD2, BIT 9), then the CRT number 2 flag (CRTFL2) is set. In either case the program then proceeds to get the CRT display code for Routine K. If the traffic failure bit (CPANIN, WORD2, BIT 11), the traffic system bit (CPANIN, WORD2, BIT 12), the controller bit (CPAN, WORD2, BIT 13), traffic system detector bit (CPAN, WORD2, BIT 14), or the traffic system intersection bit (CPANIN, WORD2, BIT 15) are set the corresponding CRT display codes are placed into CRTDC1 (for CRT 1 selected) or CRTDC2 (for CRT 2 selected) for Routine K. These codes are as follows:

1 - Traffic Failure
2 - Traffic System
3 - Controller
4 - Traffic System Detector
5 - Traffic System Intersection

If traffic system interesection is selected, the intersection number is obtained from bits 20-31 of CPANIN, WORD2. If the inserted number is greater than the number of controllers in the system (NUMCTL), Routine M takes the error exit. After the display code is stored a check is made to see if it has been more than 6 seconds since Routine K was scheduled. If it has, Routine K is scheduled and Routine M exits. If it has not been that long Routine M exits without scheduling Routine K.

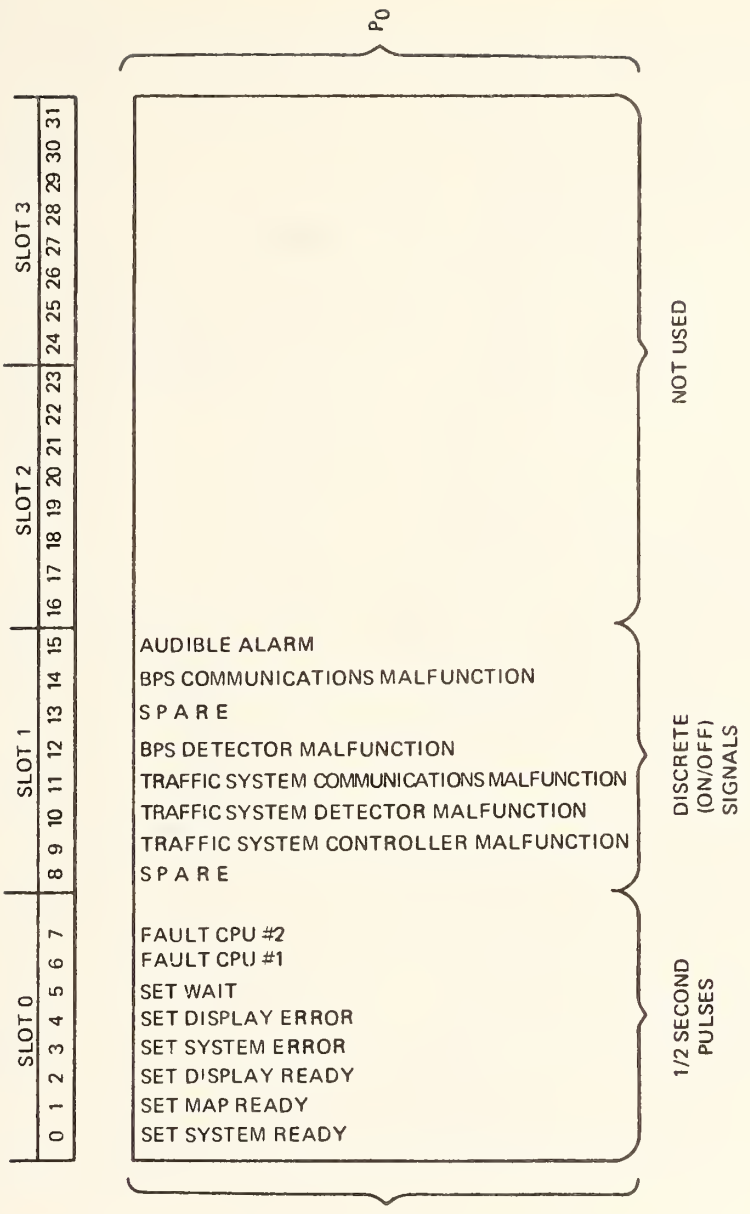
If none of the above bits are set, the routine checks to see if it is a BPS status request. The BPS intersection bit (CPANIN, WORD2, BIT 18) is checked. If it is set, the program proceeds exactly as in traffic system intersection above, except the CRT display code is 7 and if the inserted intersection number is a non-instrumented intersection, the program takes the error exit. If the BPS intersection bit is not set, the BPS system bit (CPANIN, WORD2, BIT 17) is checked and if not set, Routine M takes the error exit. If it is set, it is processed just like traffic system select, except that the CRT display code is 6.

2.14.3 Repetition Rate

This routine is entered at half-second intervals whenever time remains after the completion of higher priority routines.

2.14.4 Cross Reference

This routine is called at approximately half-second intervals by the Executive Routine, Routine A, as part of the Level 3 Priority functions.



NOTE: BIT 6 (CPU # 1 FAULT) MUST ALTERNATE STATES AT LEAST ONCE EVERY 2 SECONDS.

OUTPUT ON 7930-1, CONTROL CHANNEL 5

FIGURE 2.14.5.1. CONTROL PANEL OUTPUT BIT ASSIGNMENTS

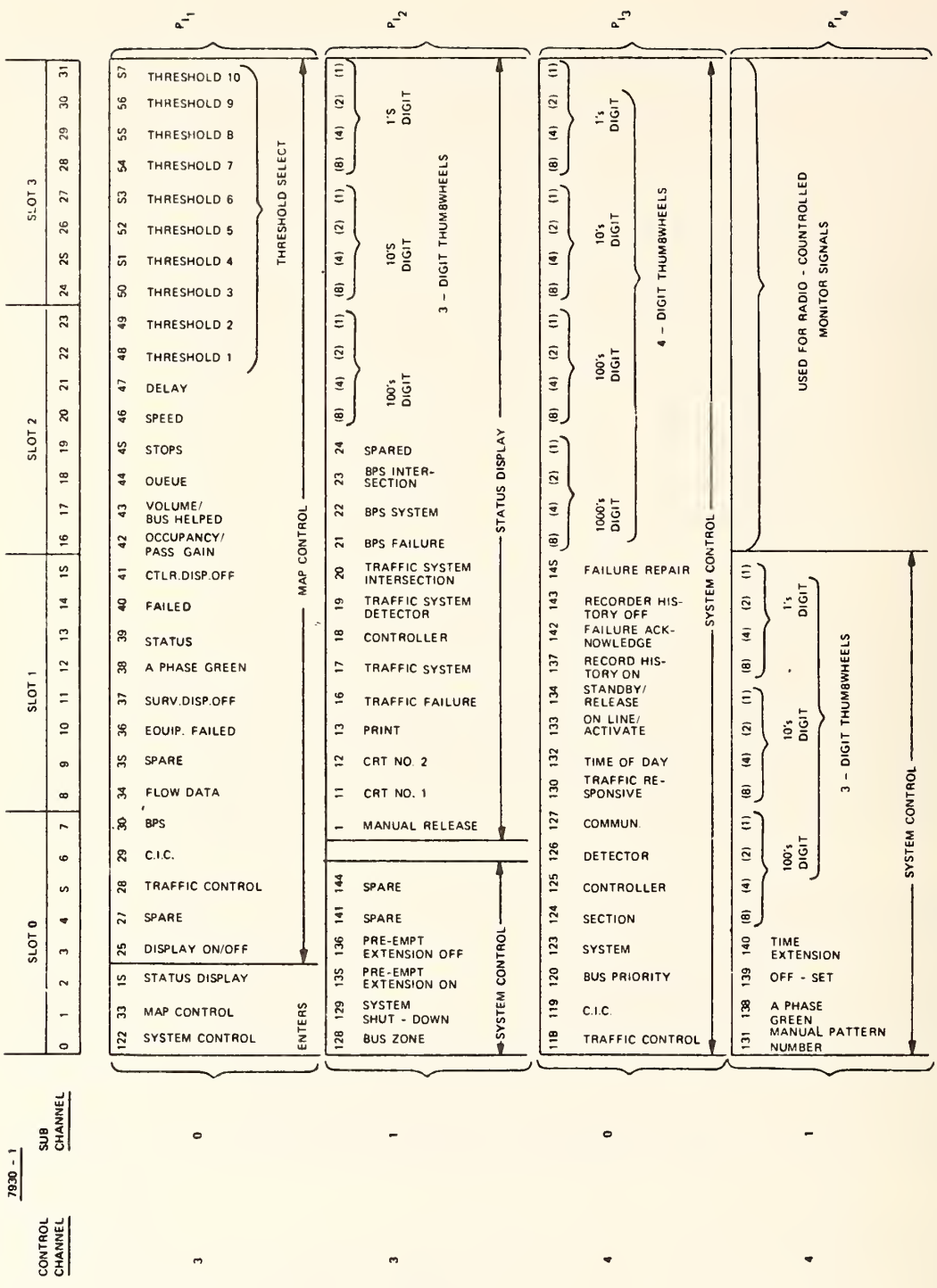


FIGURE 2.14.5.2. CONTROL PANEL INPUT BIT ASSIGNMENT

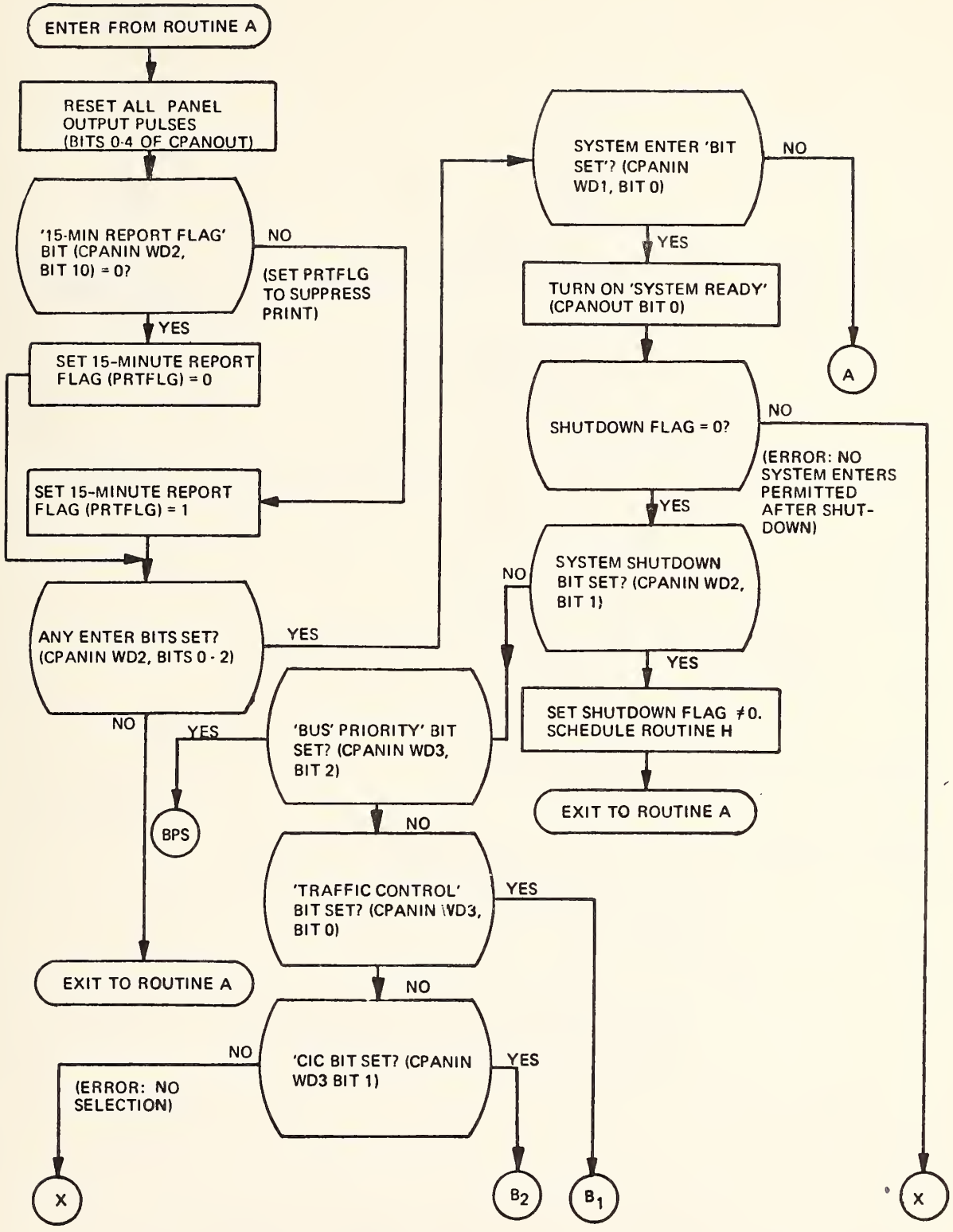


FIGURE 2.14.5.3. ROUTINE M SPECIFICATION

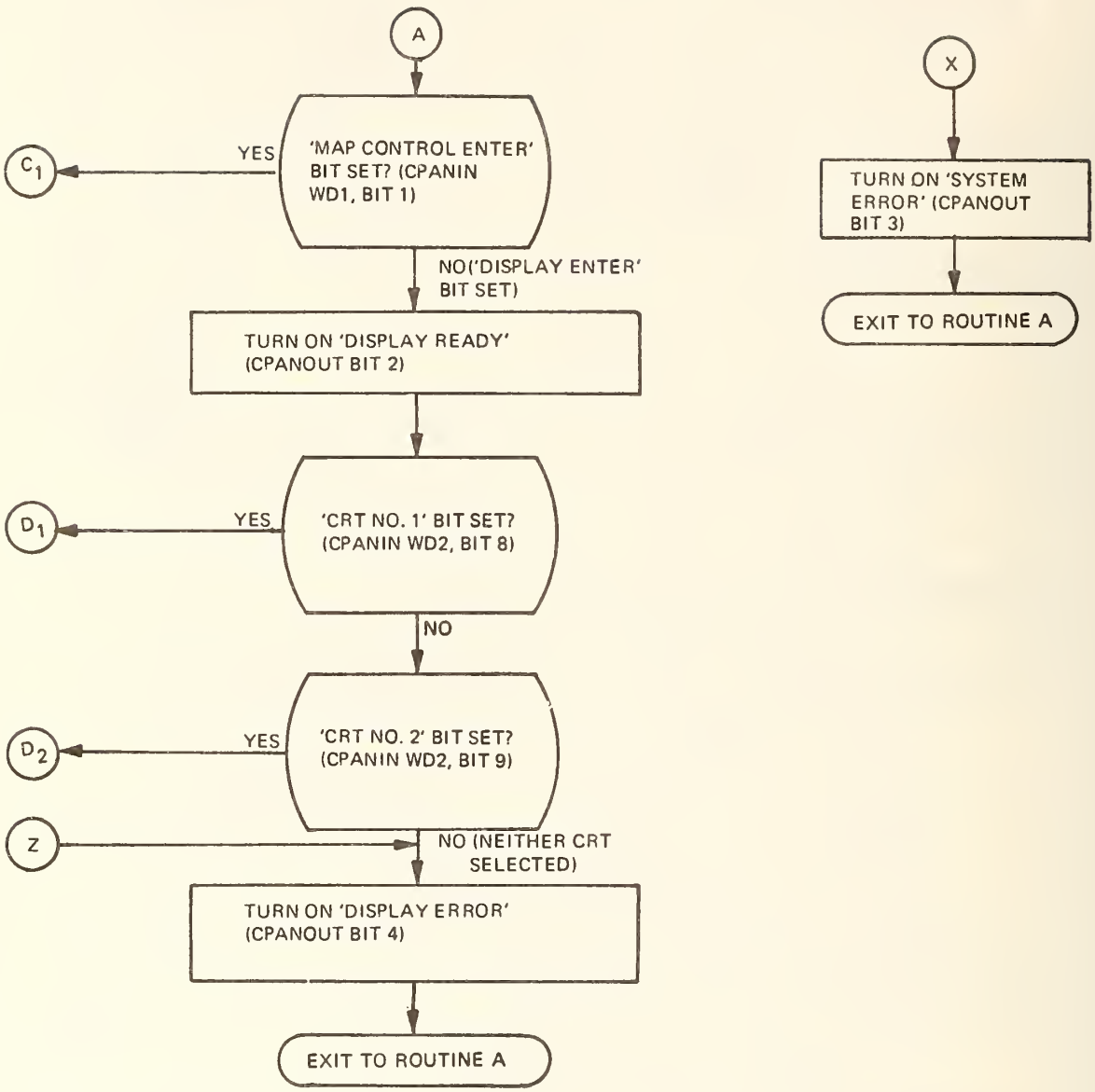


FIGURE 2.14.5.4. ROUTINE M SPECIFICATION

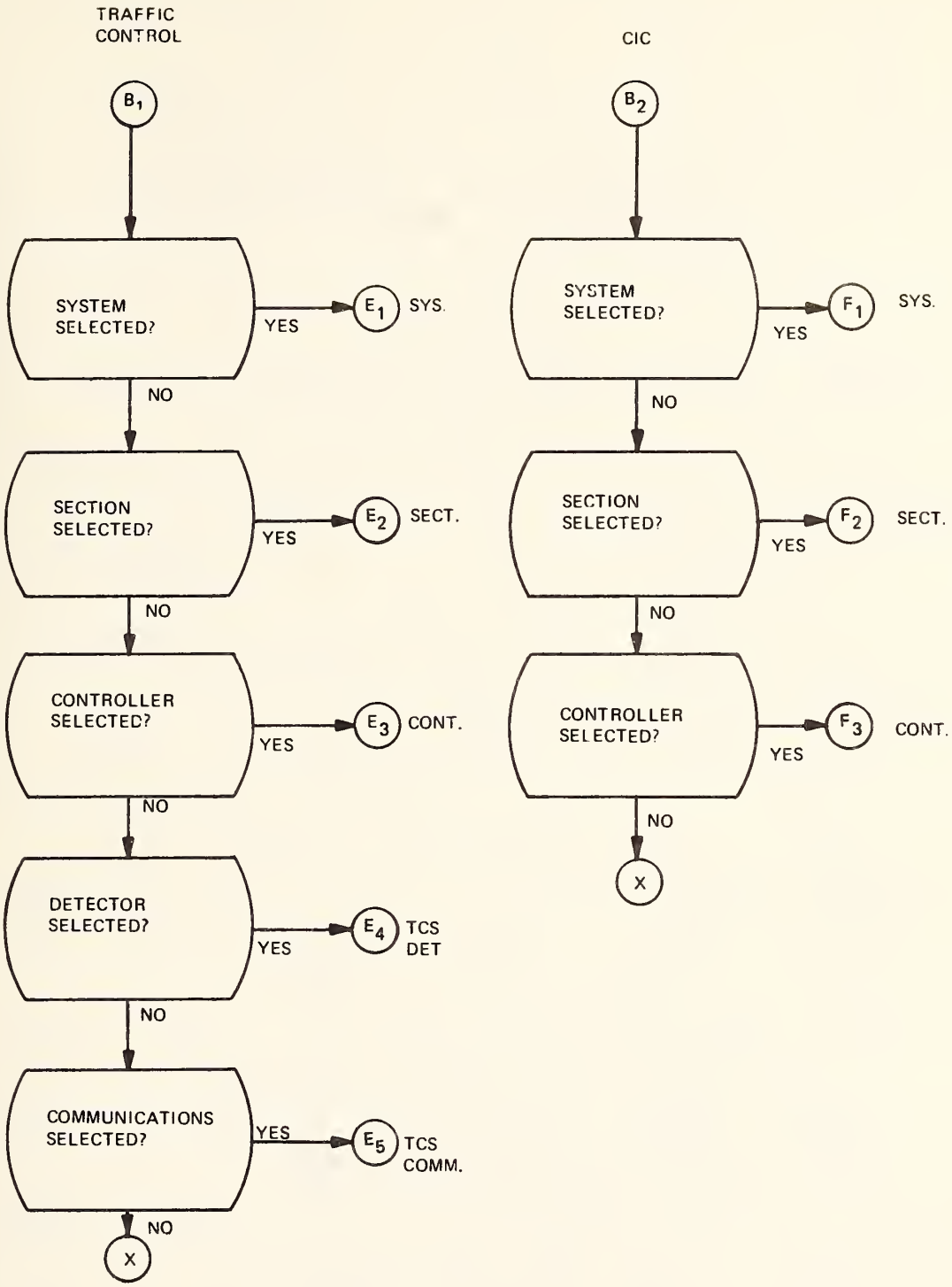


FIGURE 2.14.5.5. ROUTINE M FLOW CHART

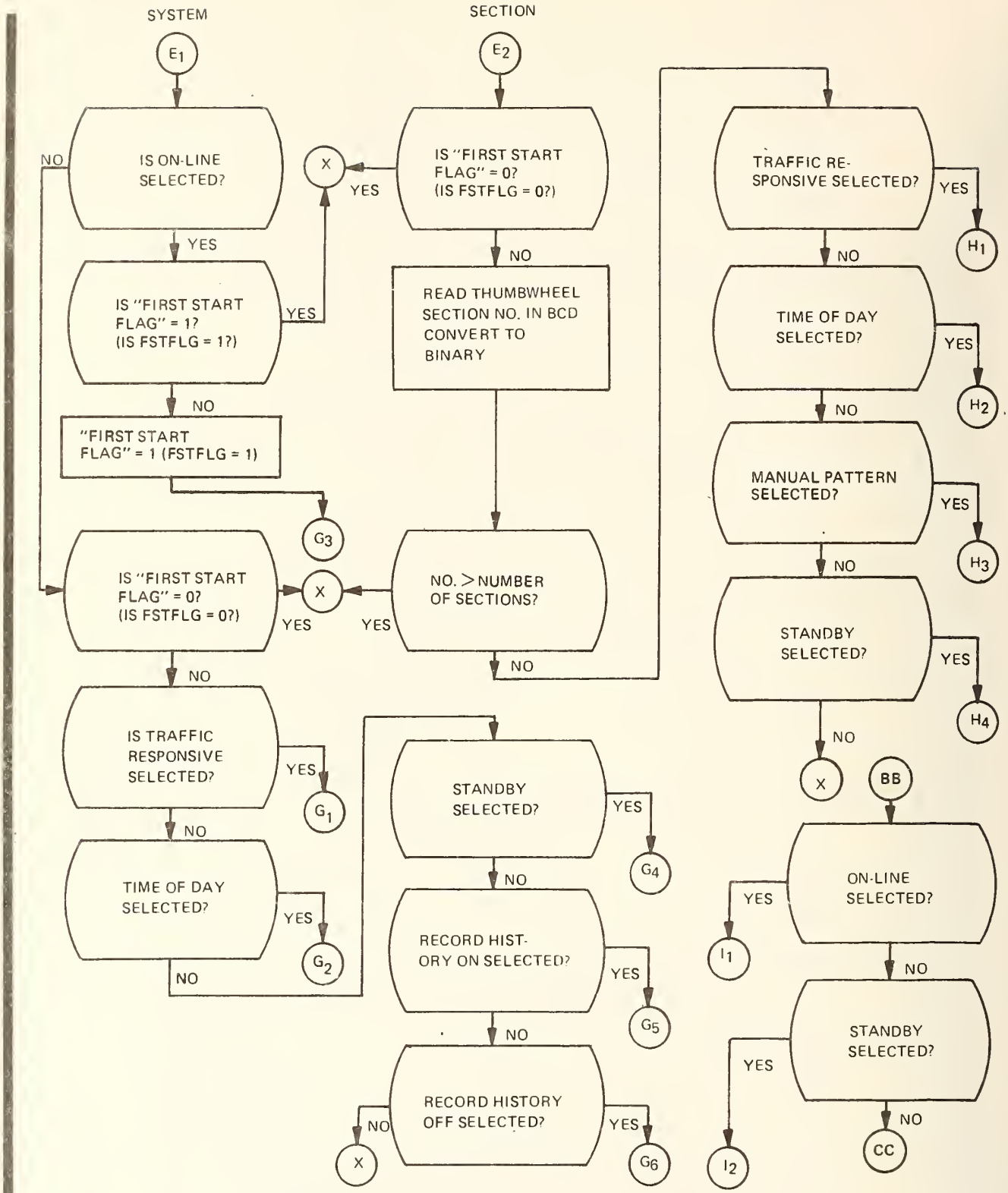


FIGURE 2.14.5.6. ROUTINE M FLOW CHART

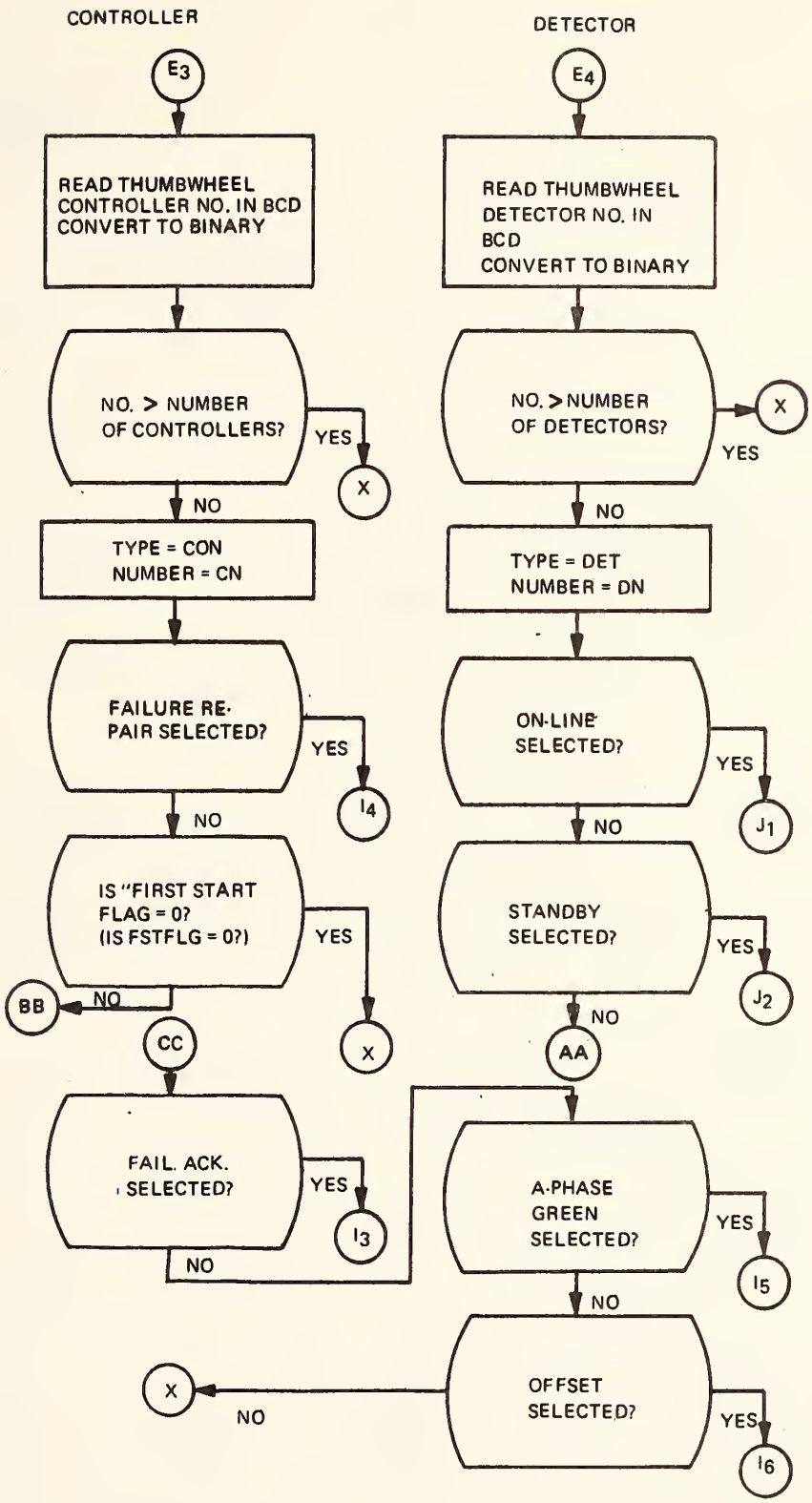


FIGURE 2.14.5.6. ROUTINE M FLOW CHART

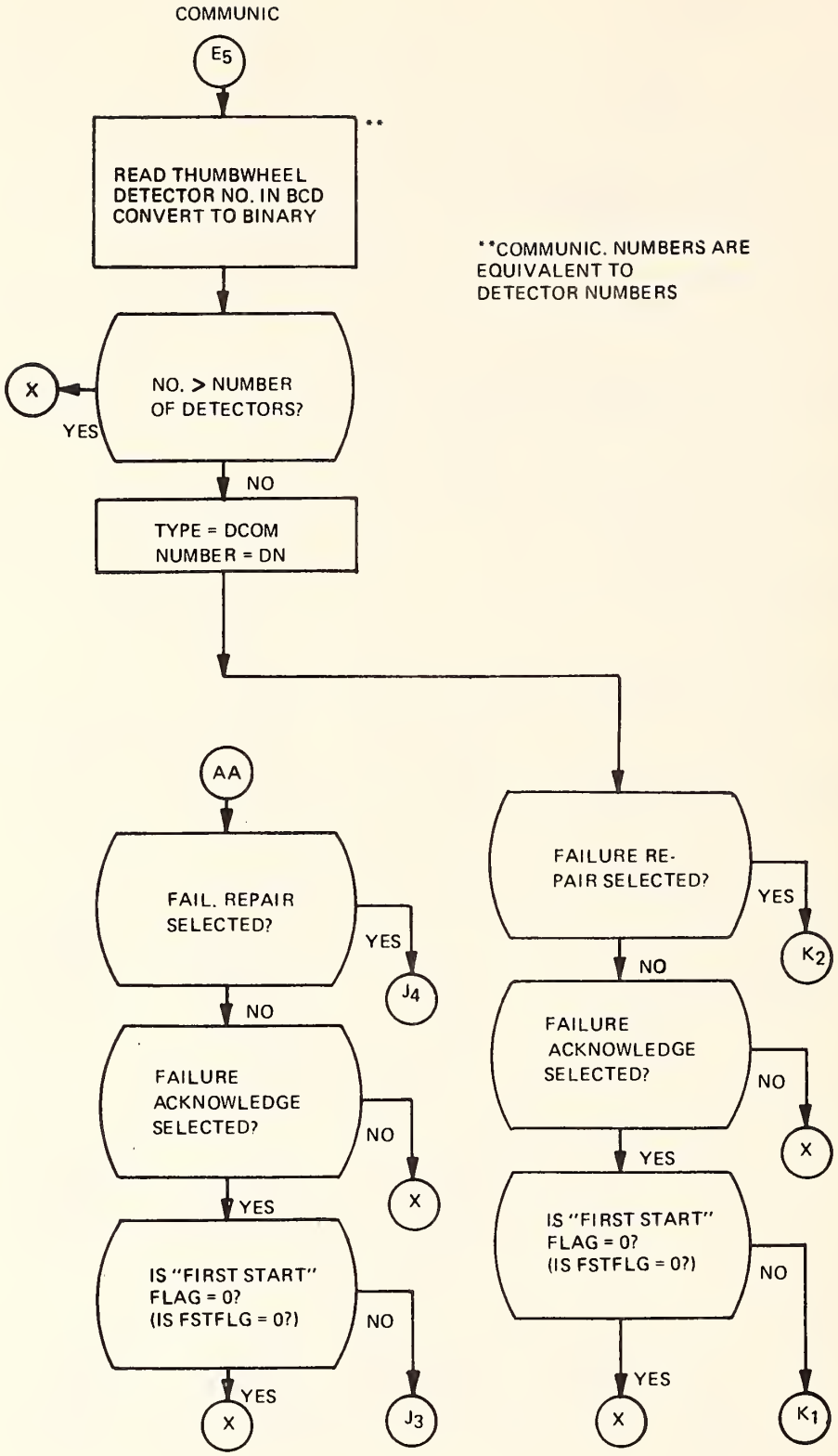


FIGURE 2.14.5.6. ROUTINE M FLOW CHART

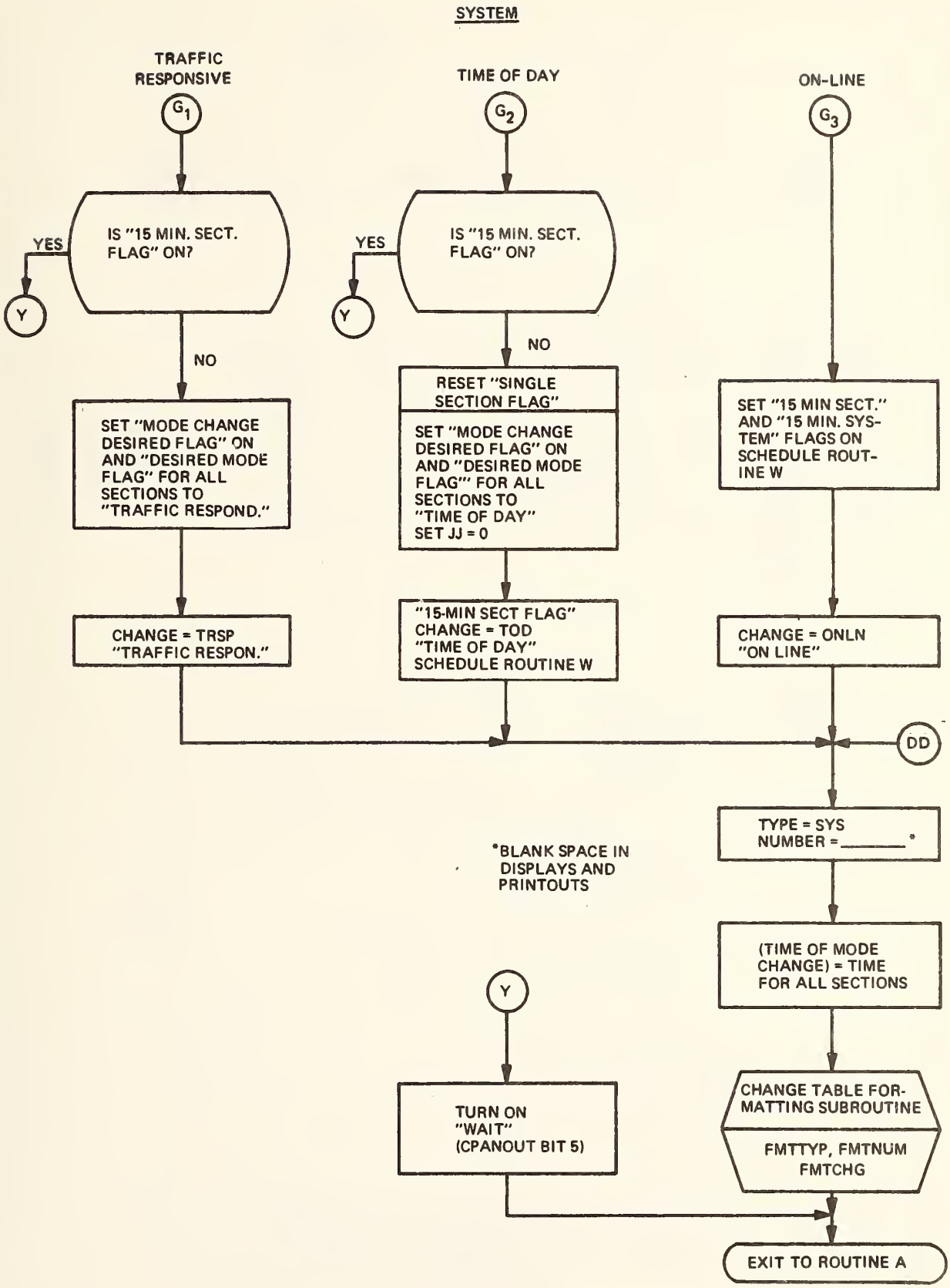


FIGURE 2.14.5.7. ROUTINE M FLOW CHART

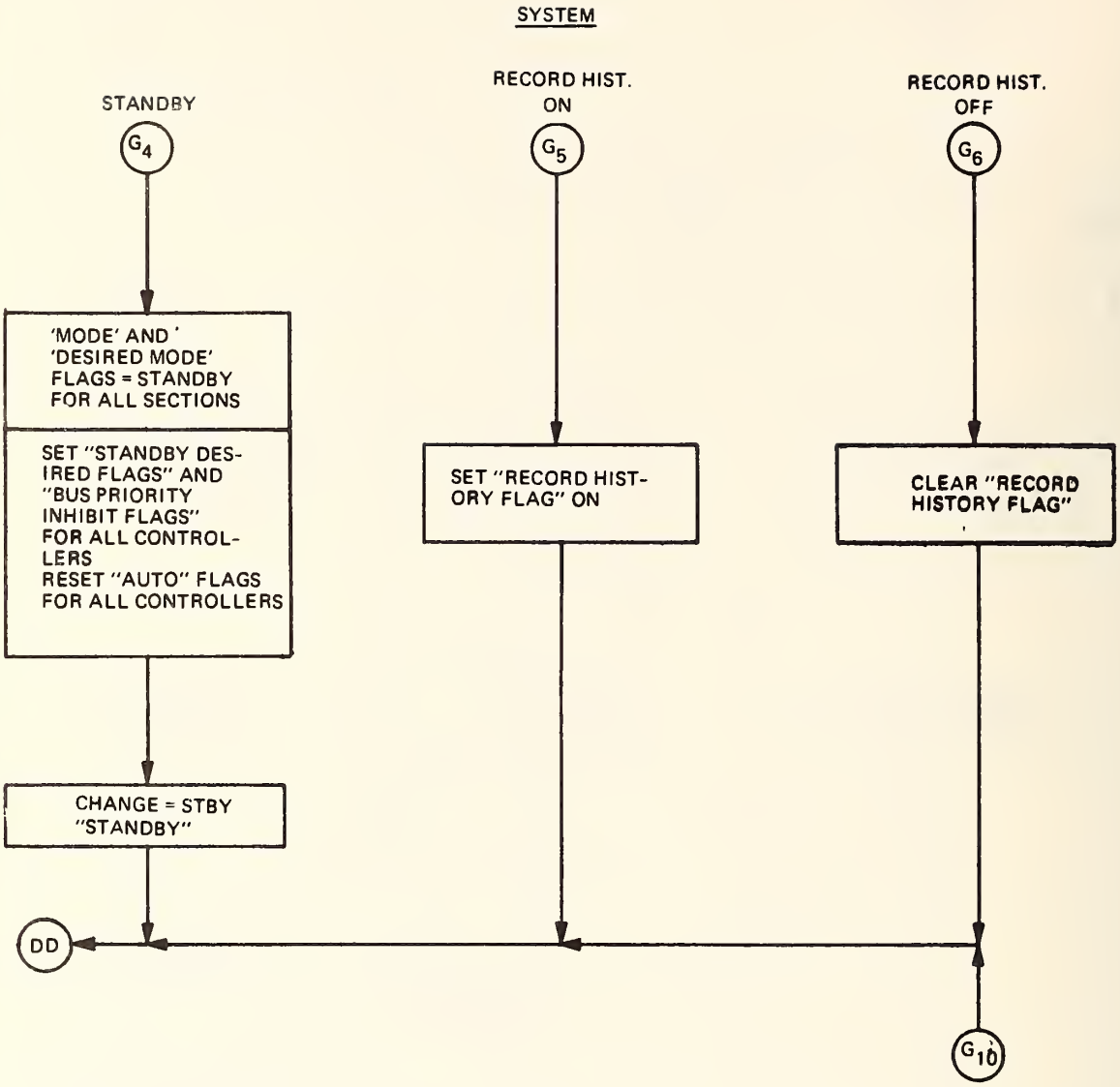


FIGURE 2.14.5.7. ROUTINE M FLOW CHART

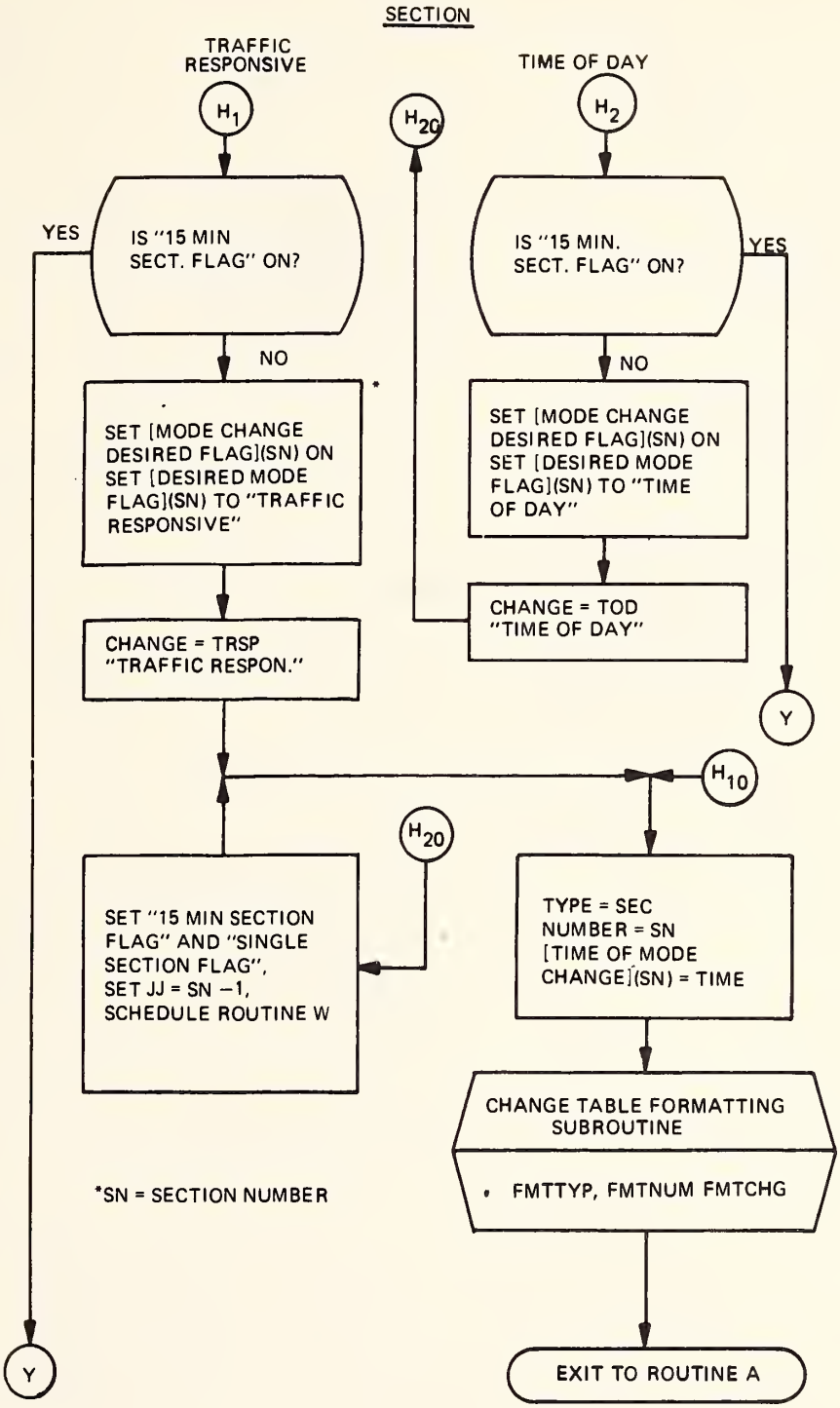


FIGURE 2.14.5.8. ROUTINE M FLOW CHART

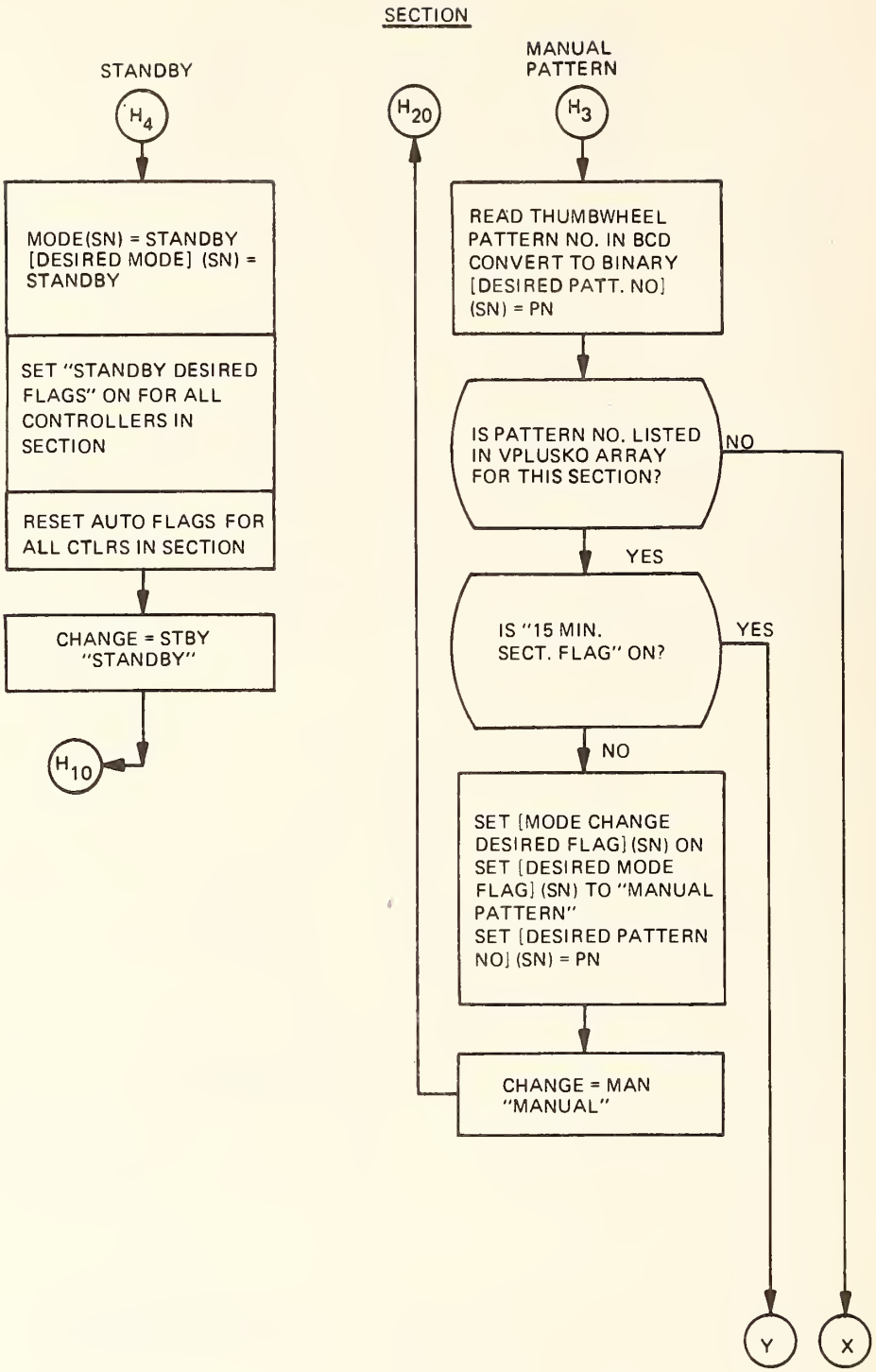


FIGURE 2.14.5.8. ROUTINE M FLOW CHART

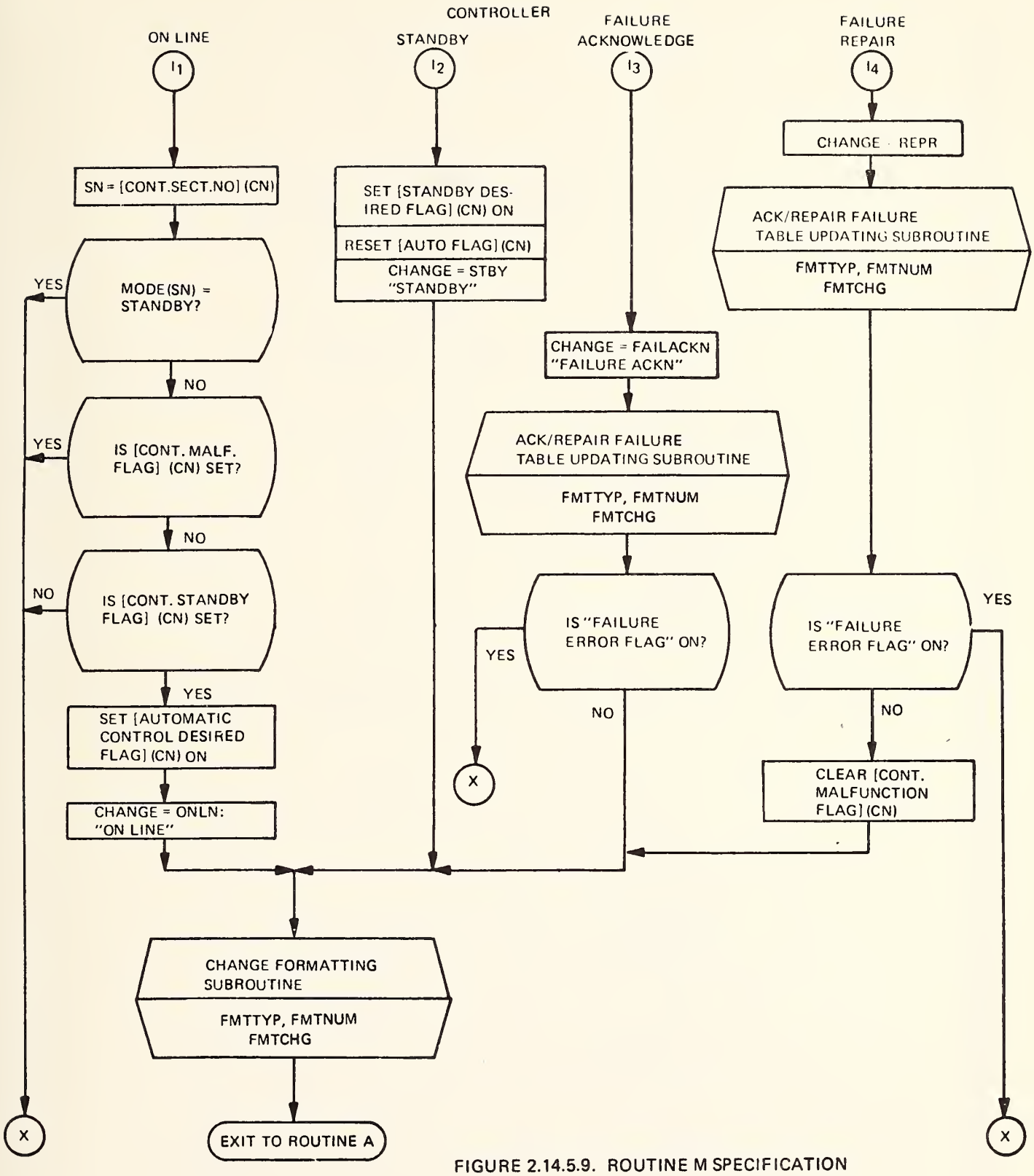


FIGURE 2.14.5.9. ROUTINE M SPECIFICATION

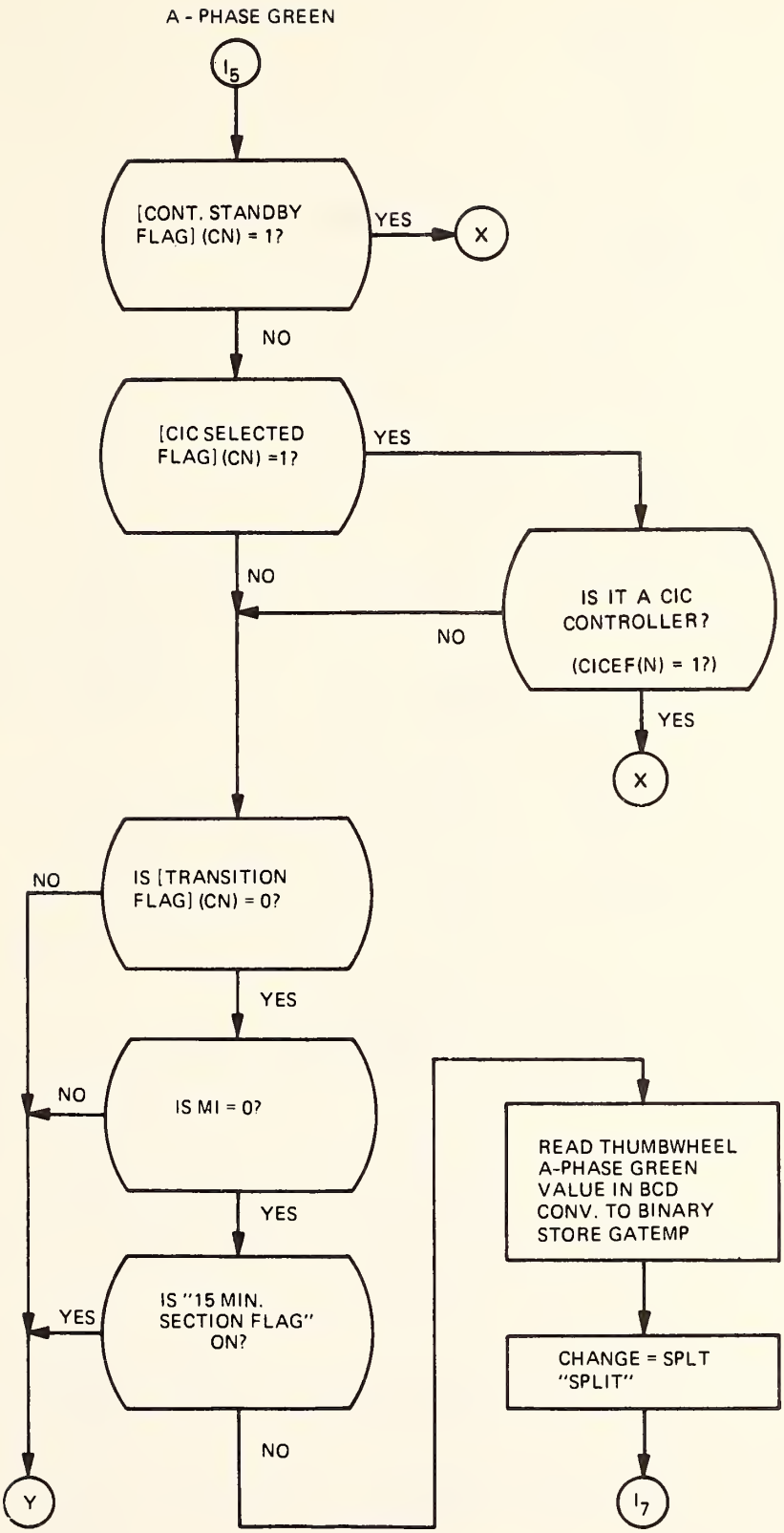


FIGURE 2.14.5.10. ROUTINE M FLOW CHART

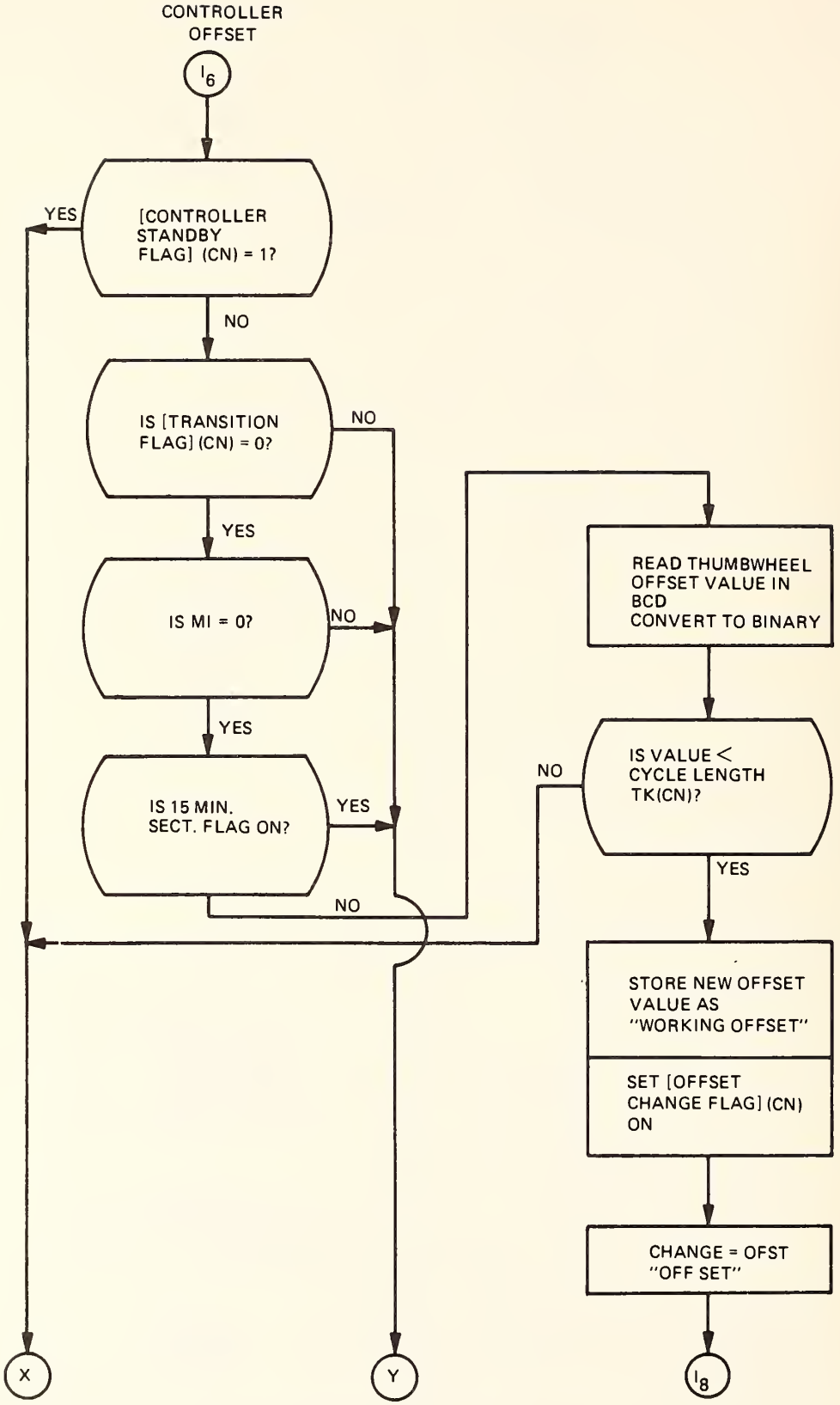


FIGURE 2.14.5.10. ROUTINE M FLOW CHART

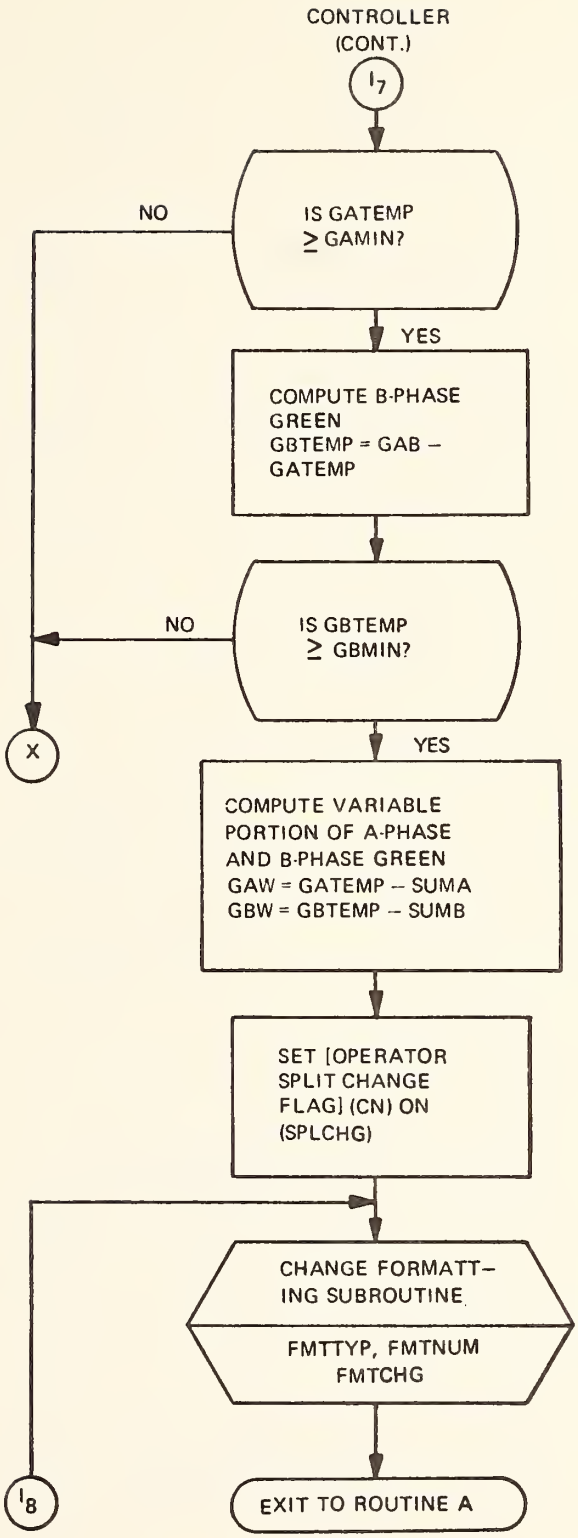


FIGURE 2.14.5.11. ROUTINE M SPECIFICATION

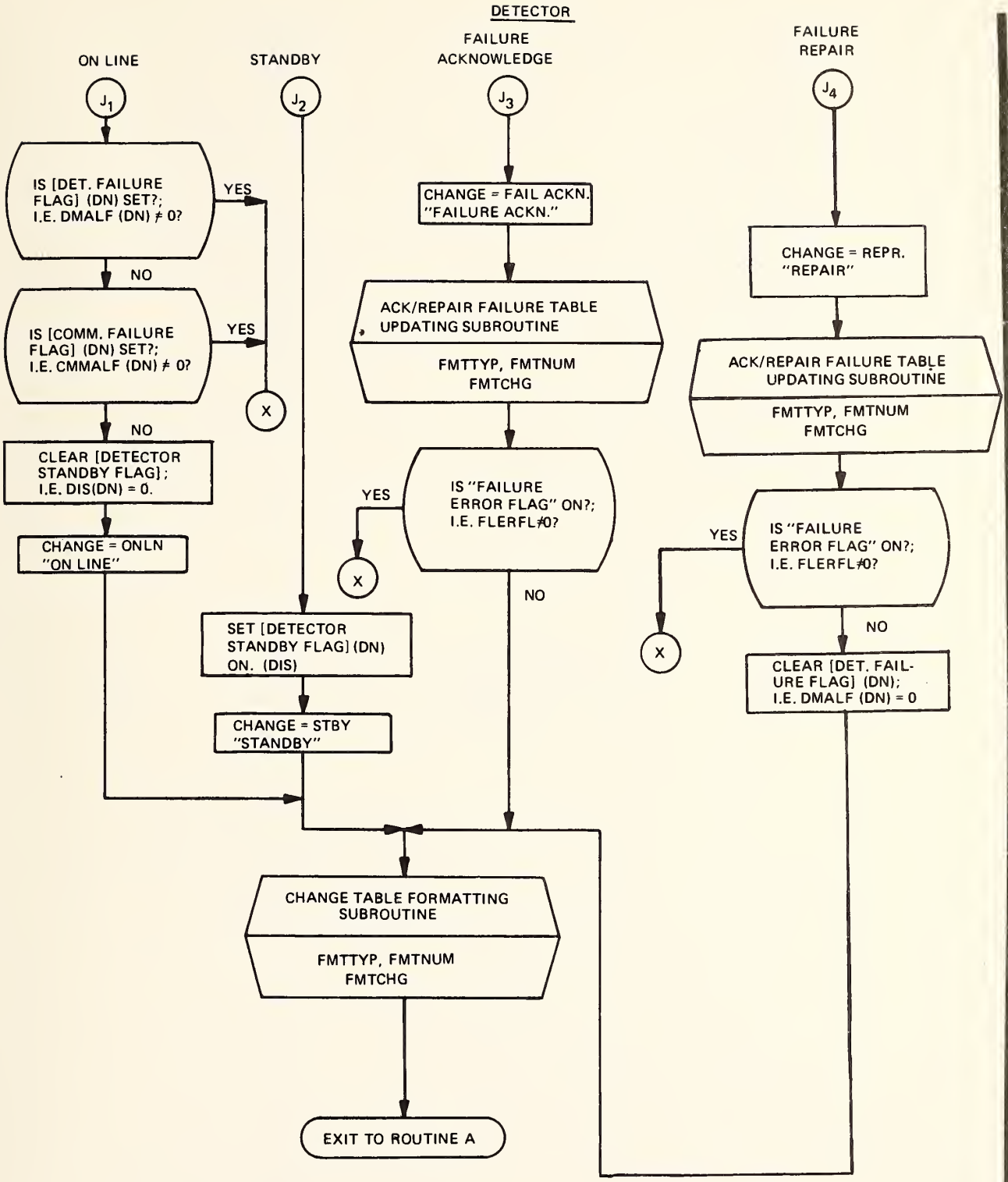


FIGURE 2.14.5.12. ROUTINE M FLOW CHART

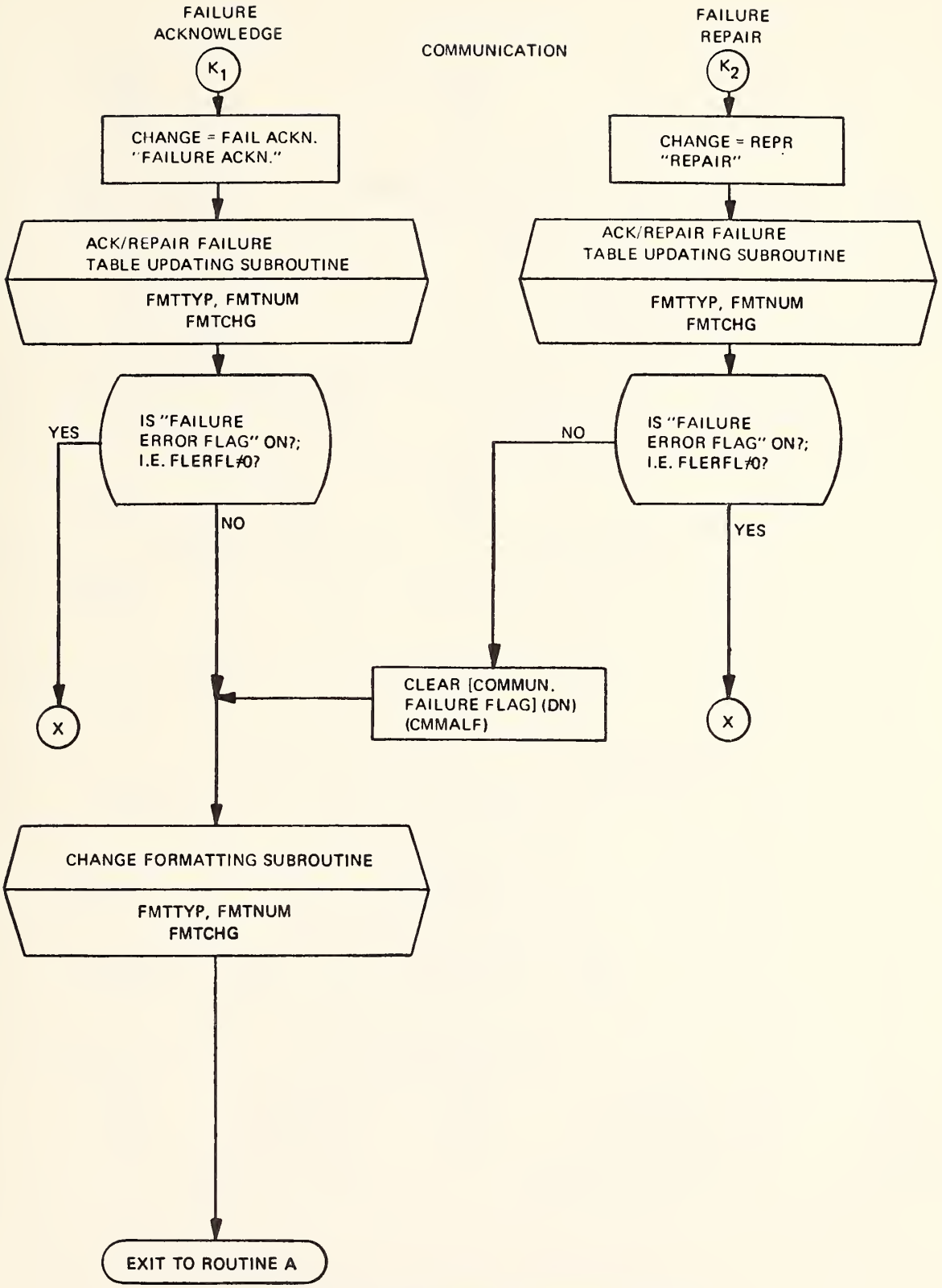


FIGURE 2.14.5.13. ROUTINE M SPECIFICATION

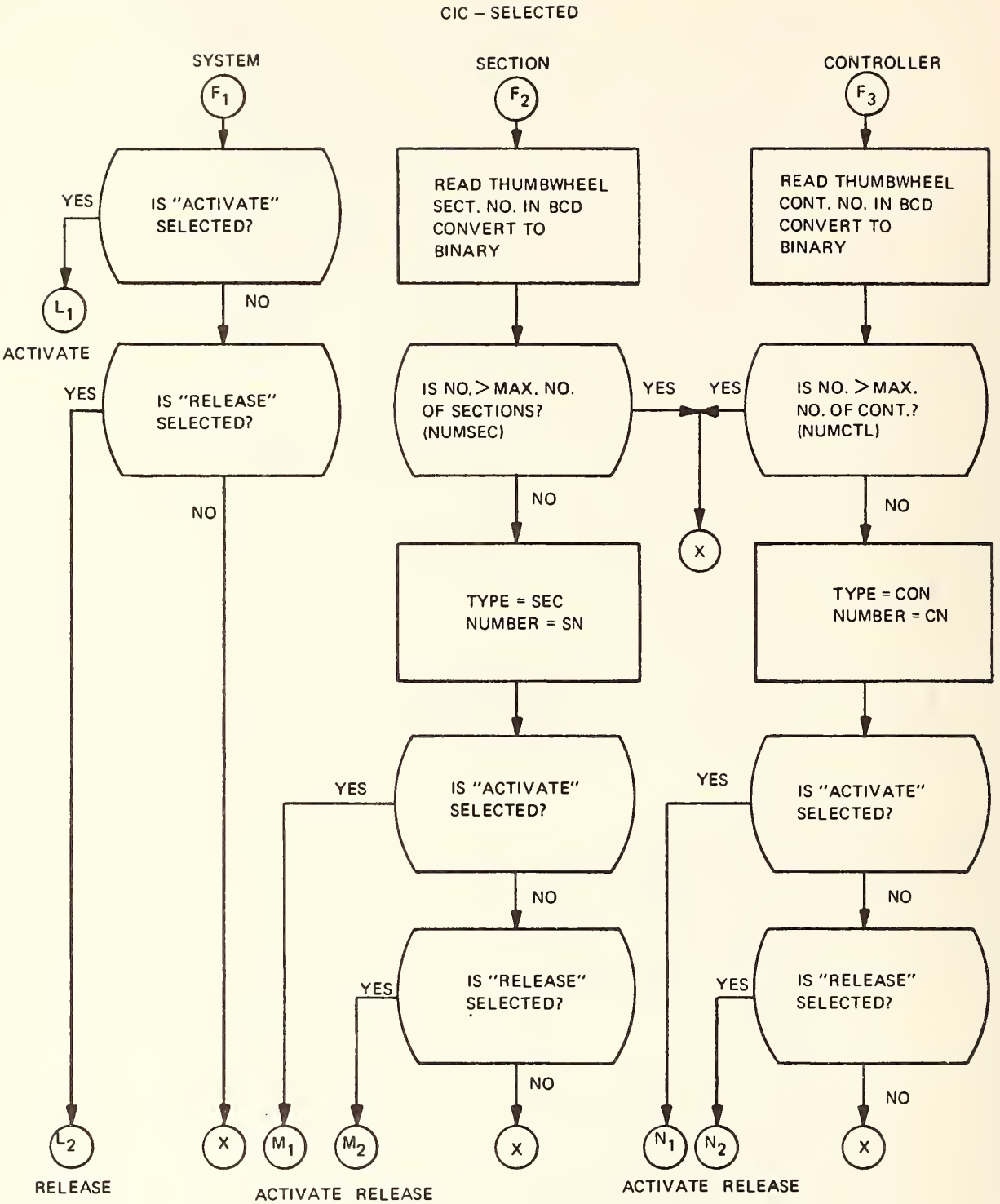


FIGURE 2.14.5.14. ROUTINE M SPECIFICATION

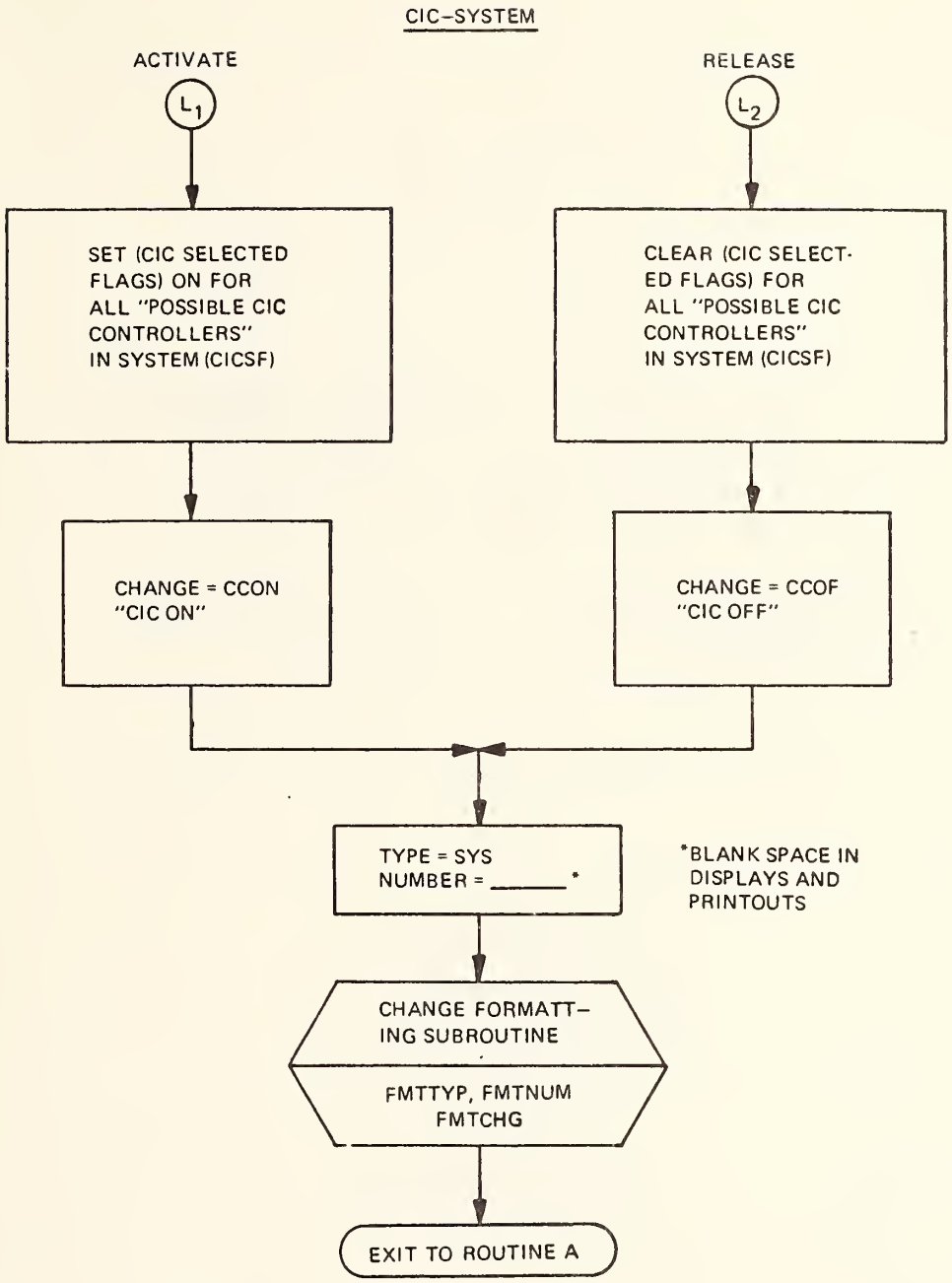


FIGURE 2.14.5.15. ROUTINE M SPECIFICATION

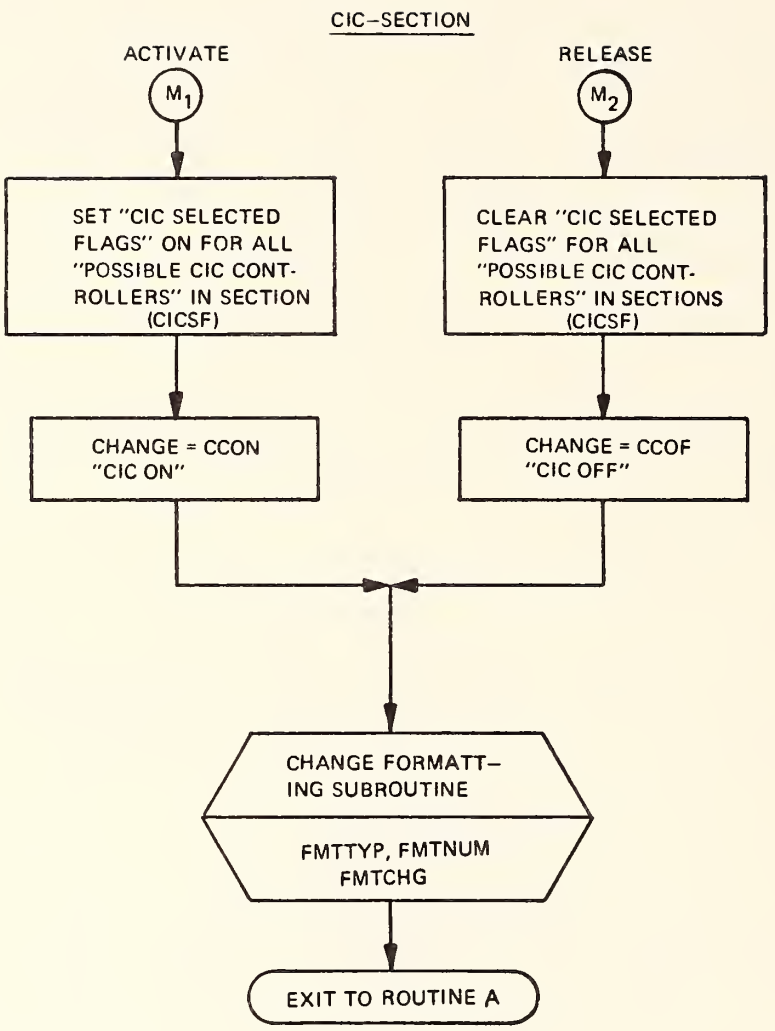


FIGURE 2.14.5.16. ROUTINE M SPECIFICATION

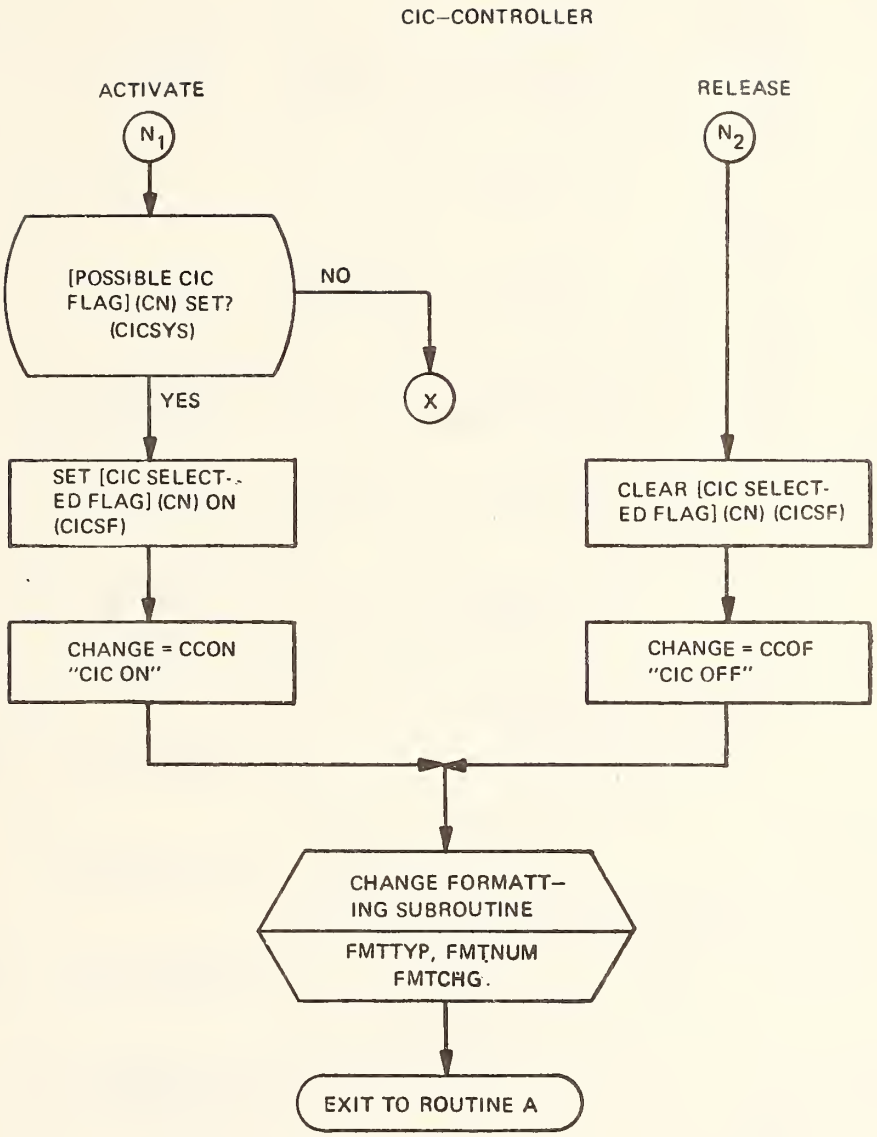


FIGURE 2.14.5.17. ROUTINE M SPECIFICATION

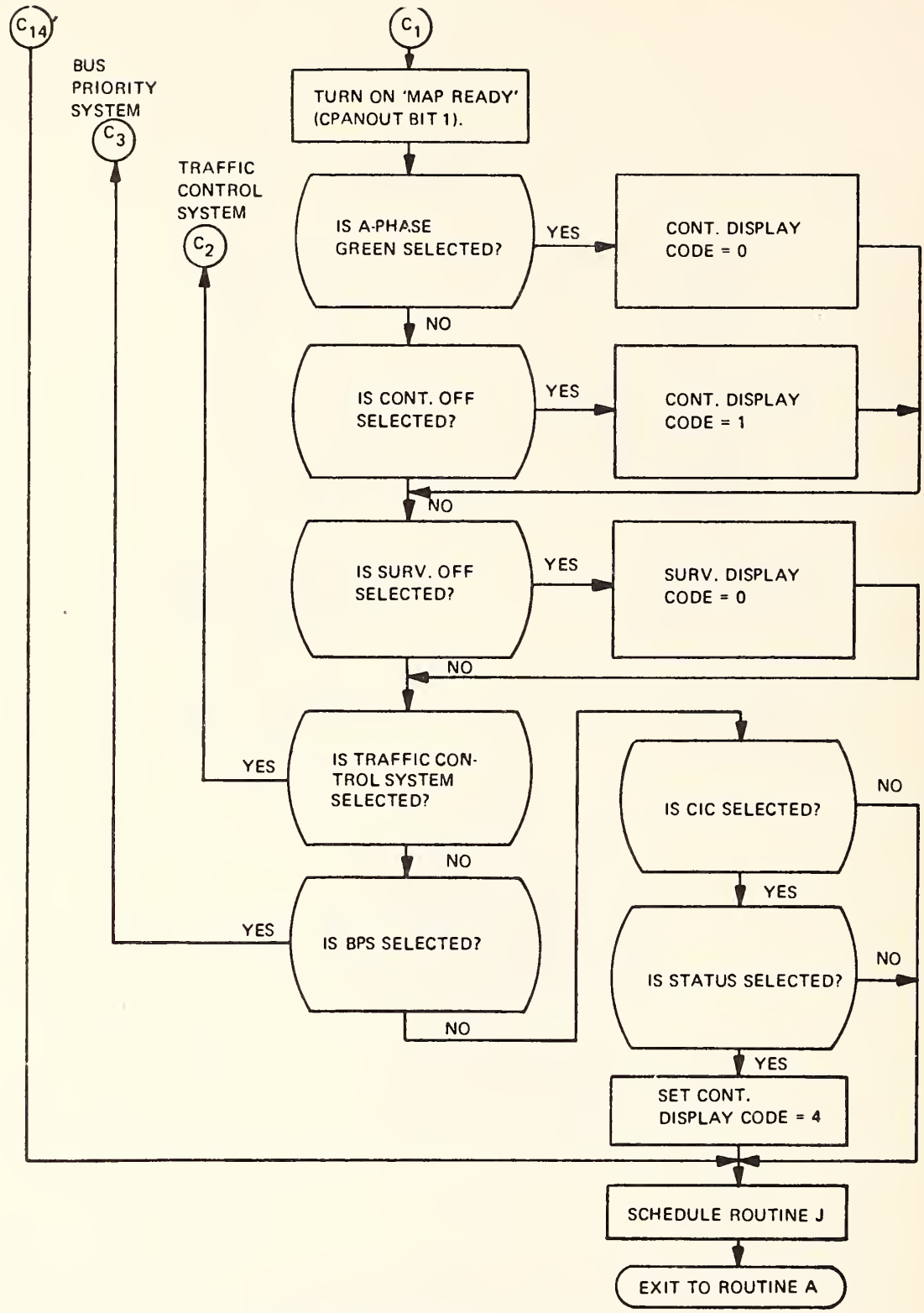


FIGURE 2.14.5.18. ROUTINE M SPECIFICATION

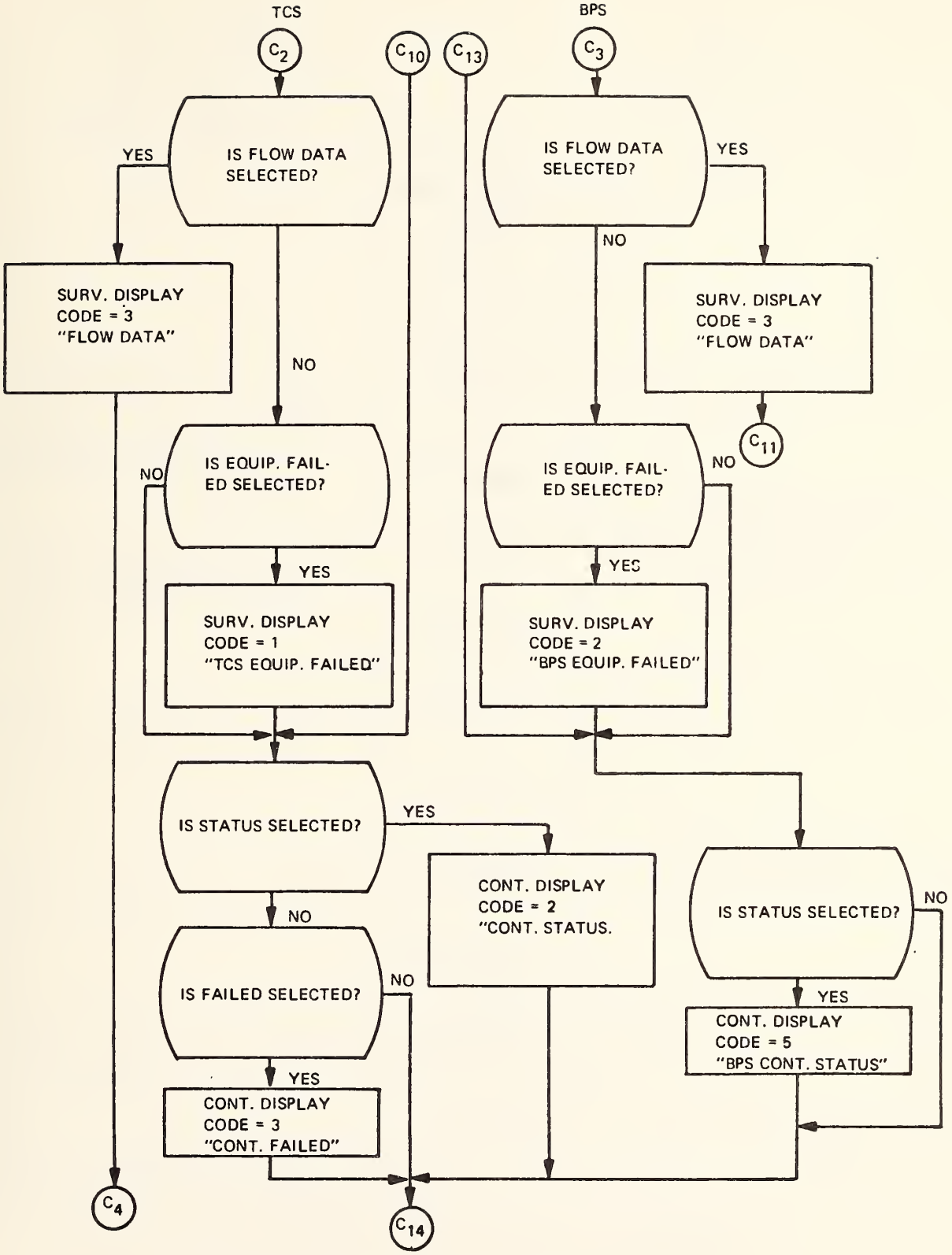
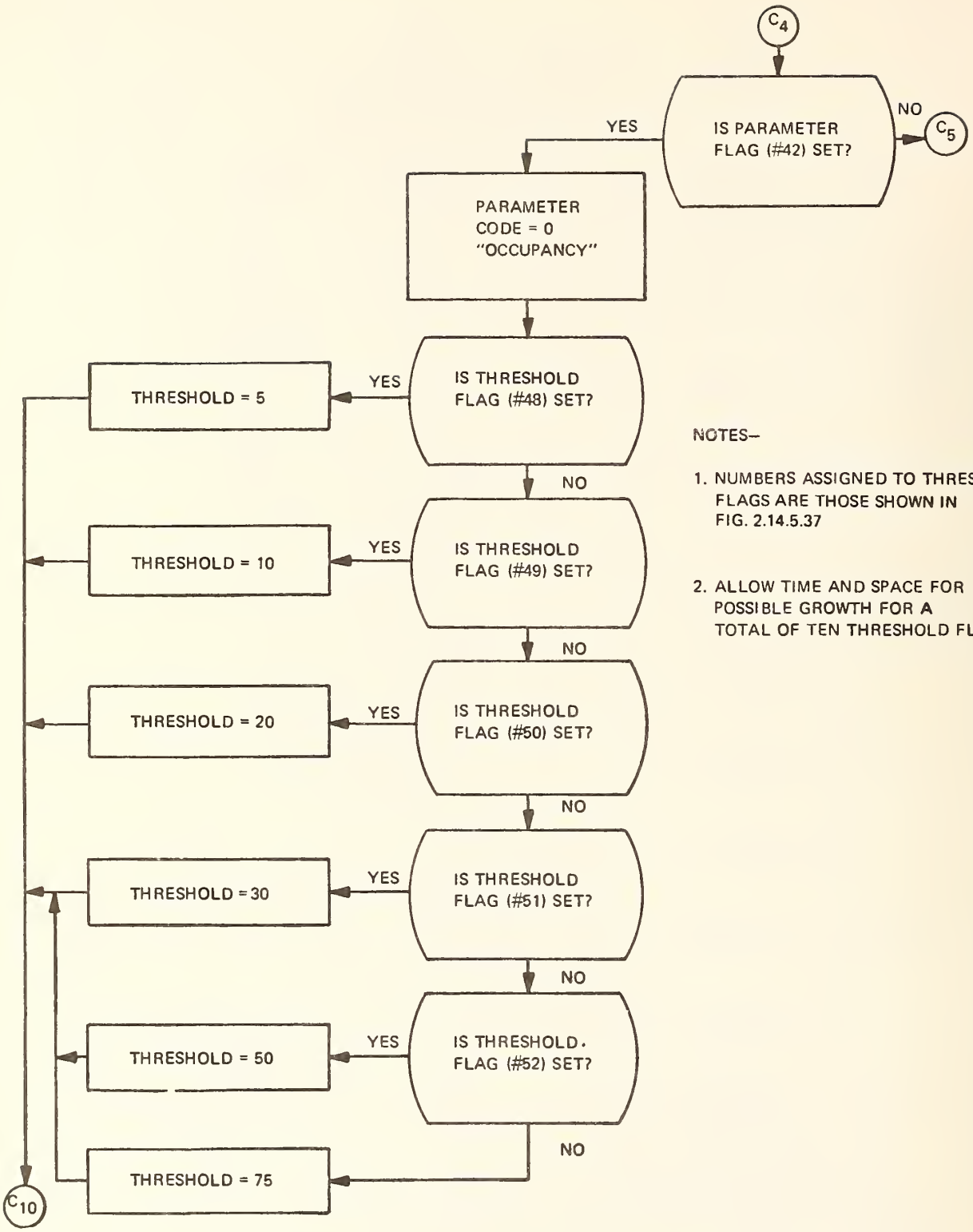


FIGURE 2.14.5.19. ROUTINE M SPECIFICATION



NOTES–

1. NUMBERS ASSIGNED TO THRESHOLD FLAGS ARE THOSE SHOWN IN FIG. 2.14.5.37

2. ALLOW TIME AND SPACE FOR POSSIBLE GROWTH FOR A TOTAL OF TEN THRESHOLD FLAGS.

FIGURE 2.14.5.20 ROUTINE M SPECIFICATION

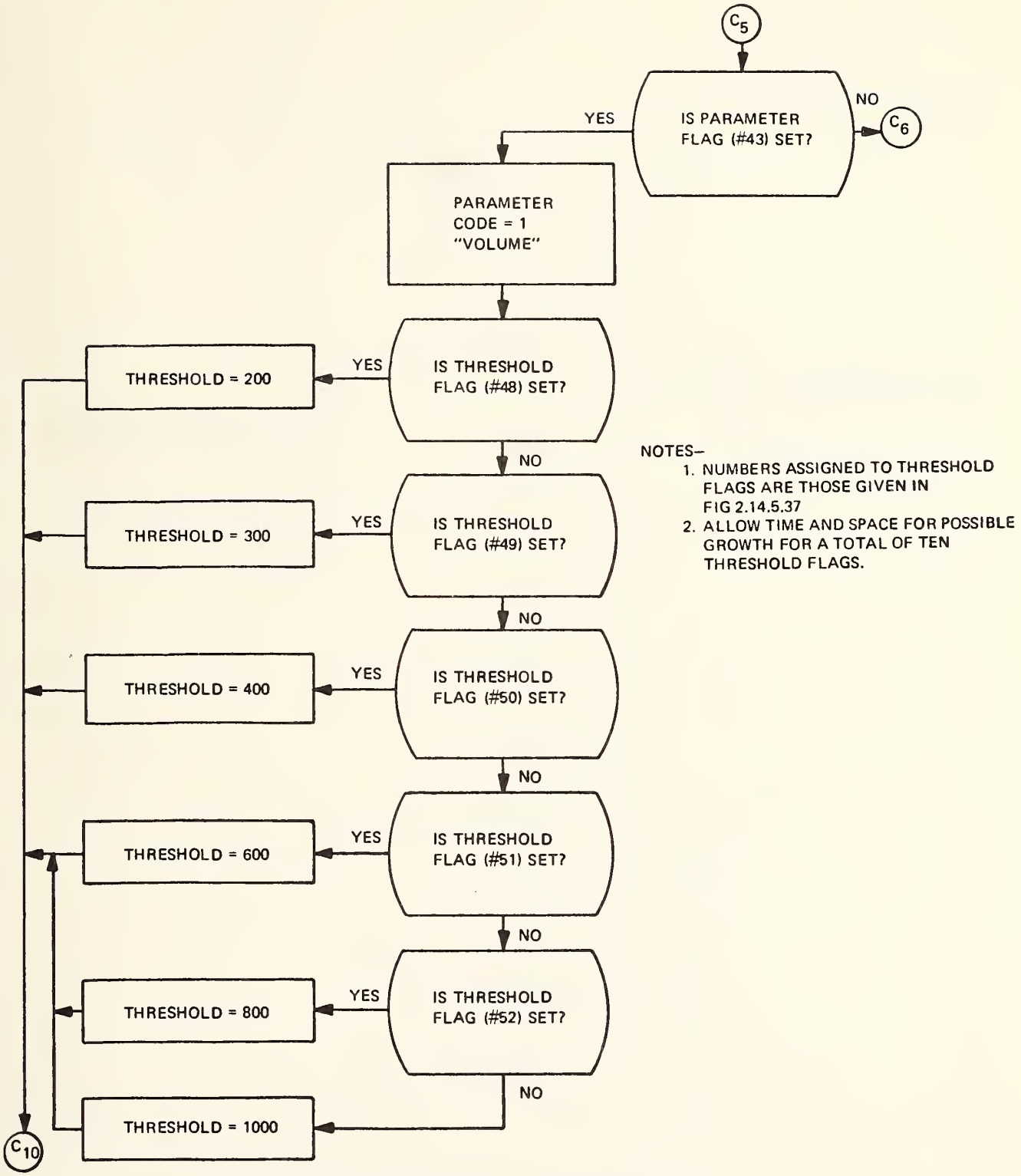
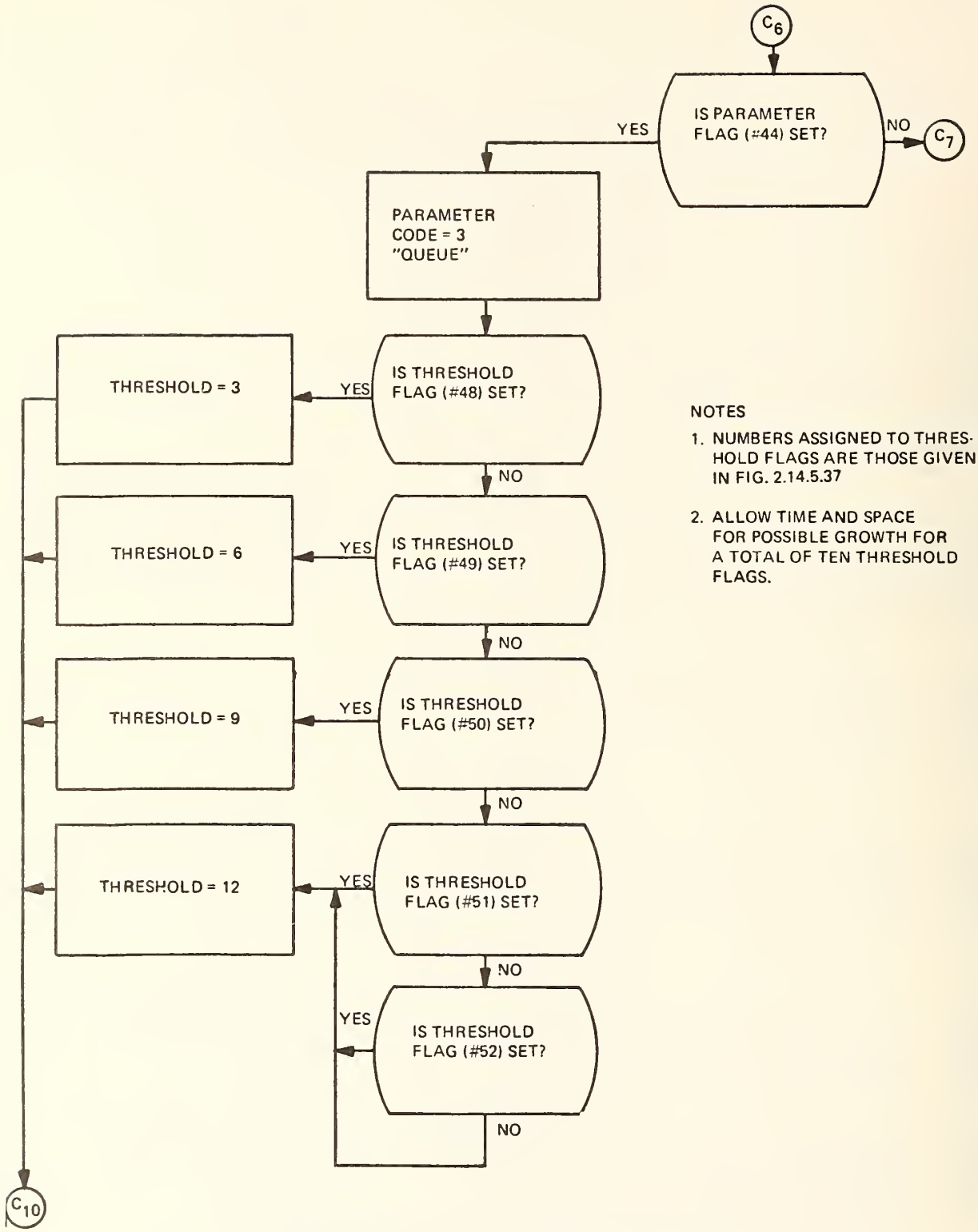


FIGURE 2.14.5.21. ROUTINE M SPECIFICATION



NOTES

1. NUMBERS ASSIGNED TO THRESHOLD FLAGS ARE THOSE GIVEN IN FIG. 2.14.5.37
2. ALLOW TIME AND SPACE FOR POSSIBLE GROWTH FOR A TOTAL OF TEN THRESHOLD FLAGS.

FIGURE 2.14.5.22. ROUTINE M SPECIFICATION

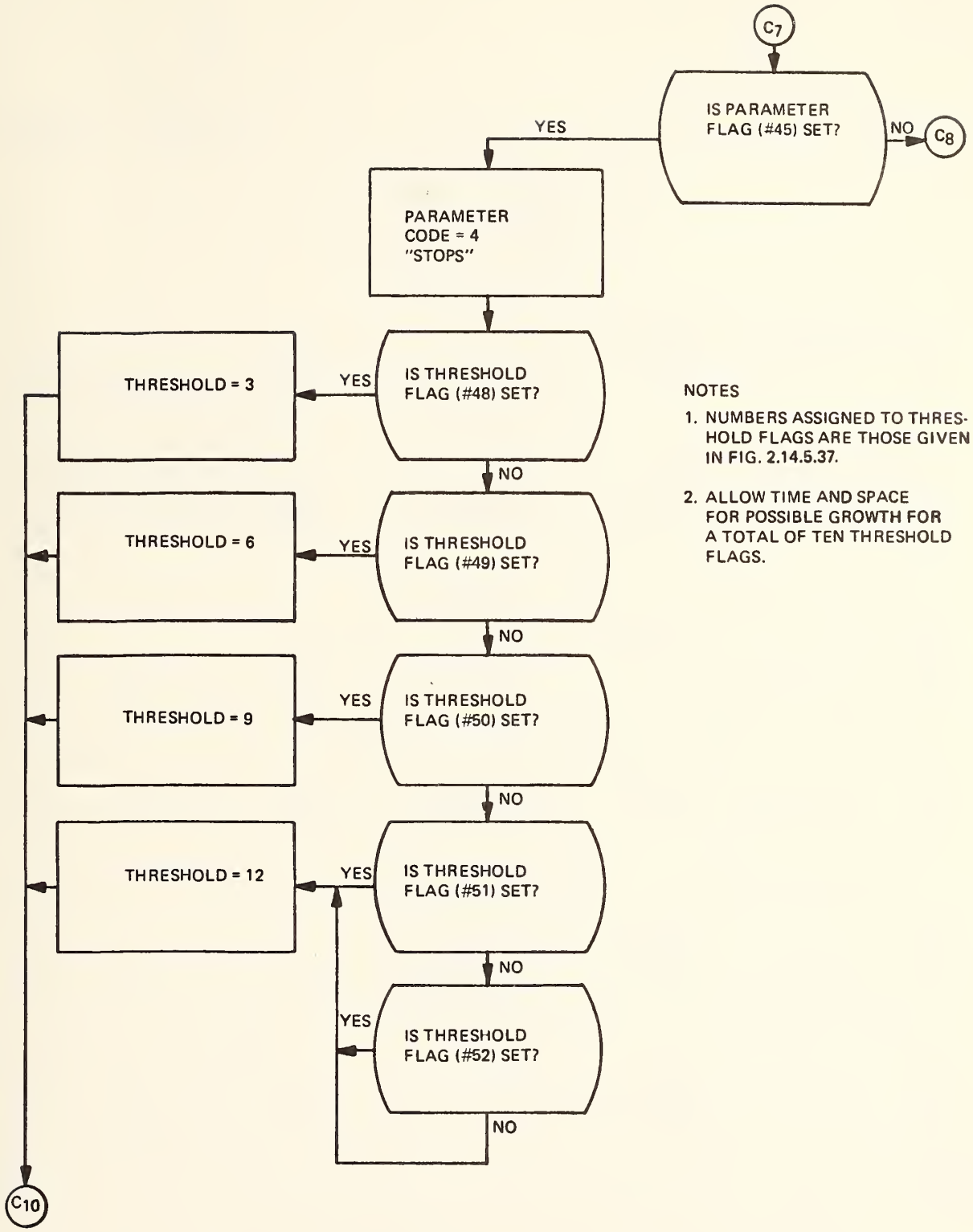


FIGURE 2.14.5.23. ROUTINE M SPECIFICATION

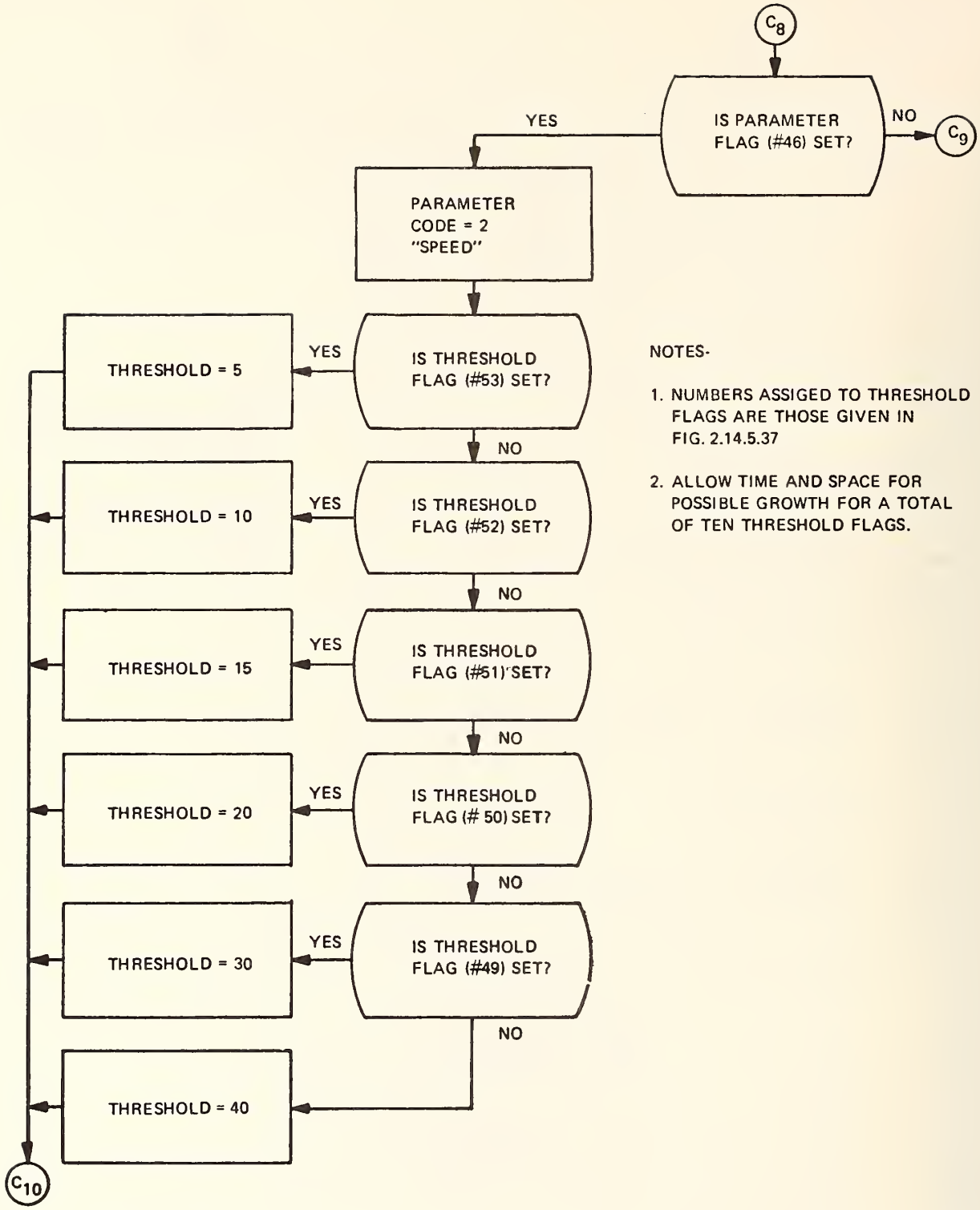


FIGURE 2.14.5.24. ROUTINE M SPECIFICATION

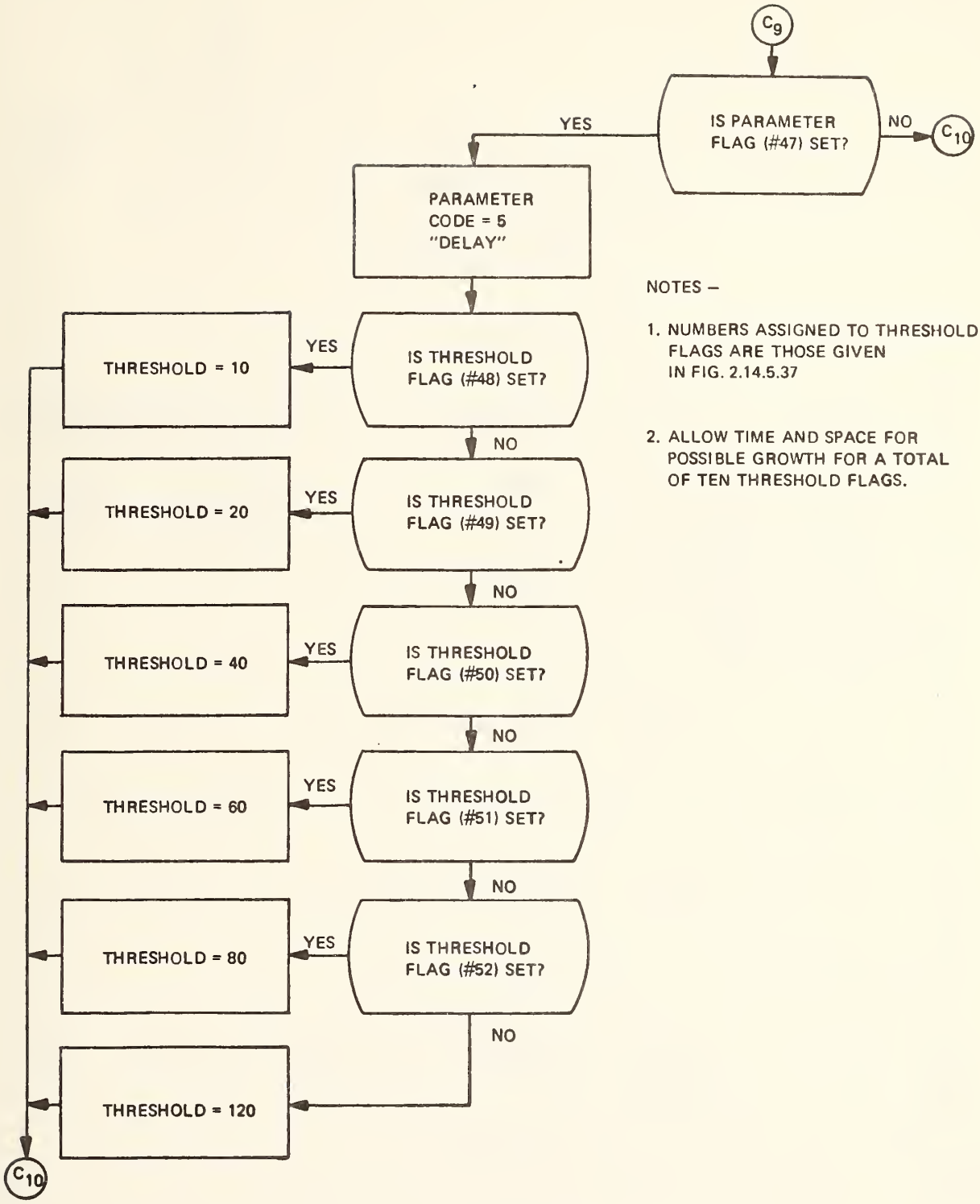


FIGURE 2.14.5.25. ROUTINE M SPECIFICATION

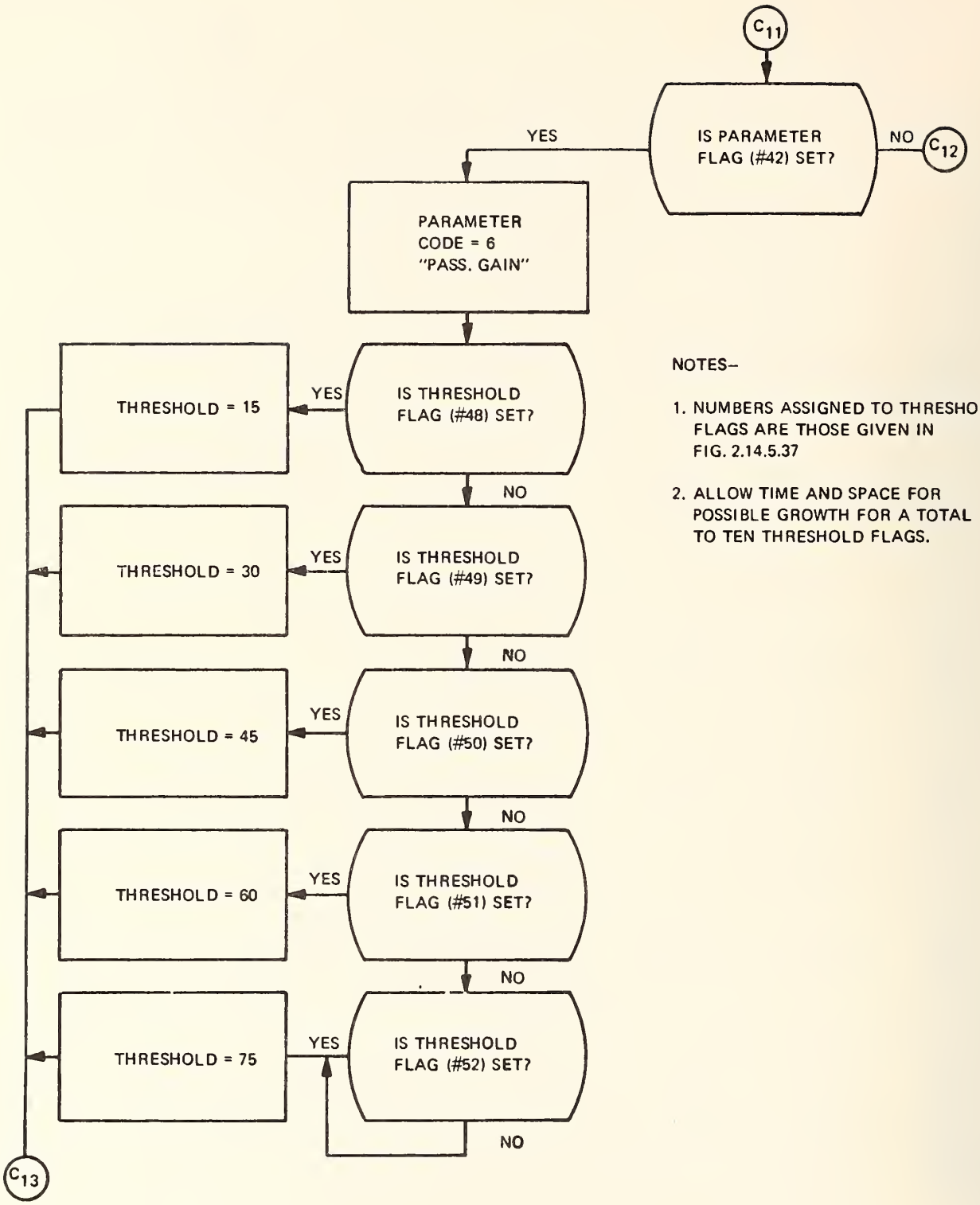


FIGURE 2.14.5.26. ROUTINE M SPECIFICATION

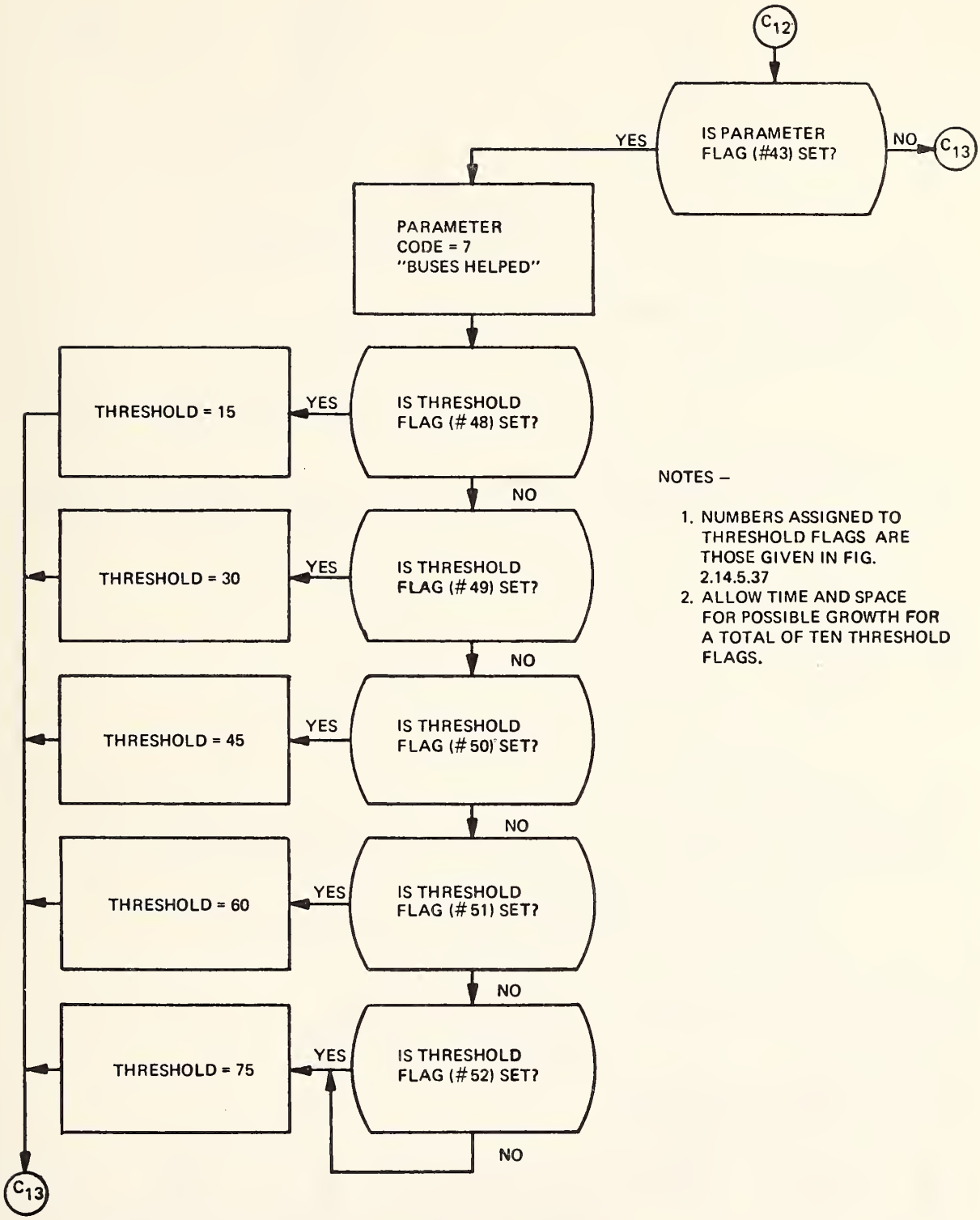


FIGURE 2.14.5.27. ROUTINE M SPECIFICATION

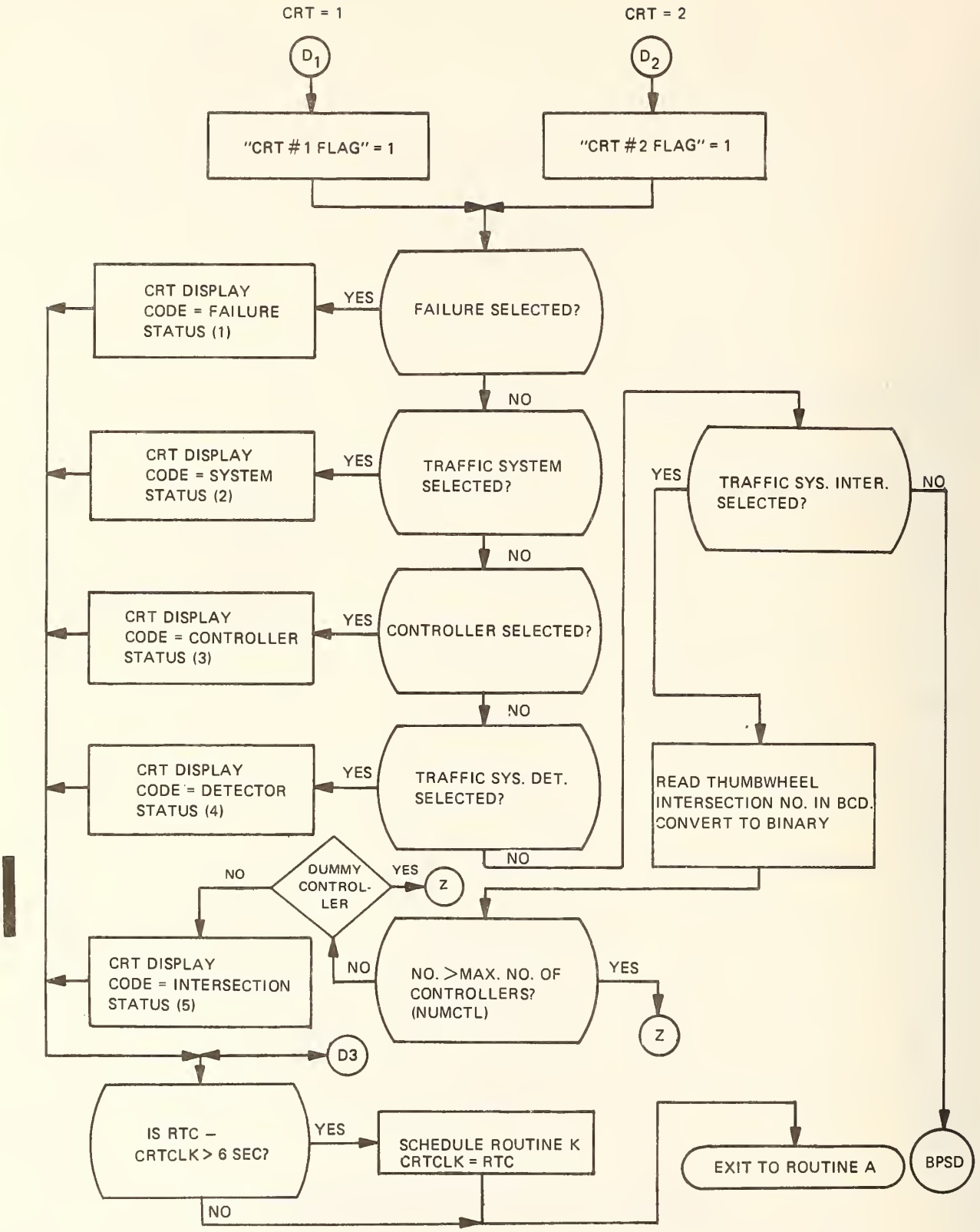


FIGURE 2.14.5.28. ROUTINE M FLOW CHART

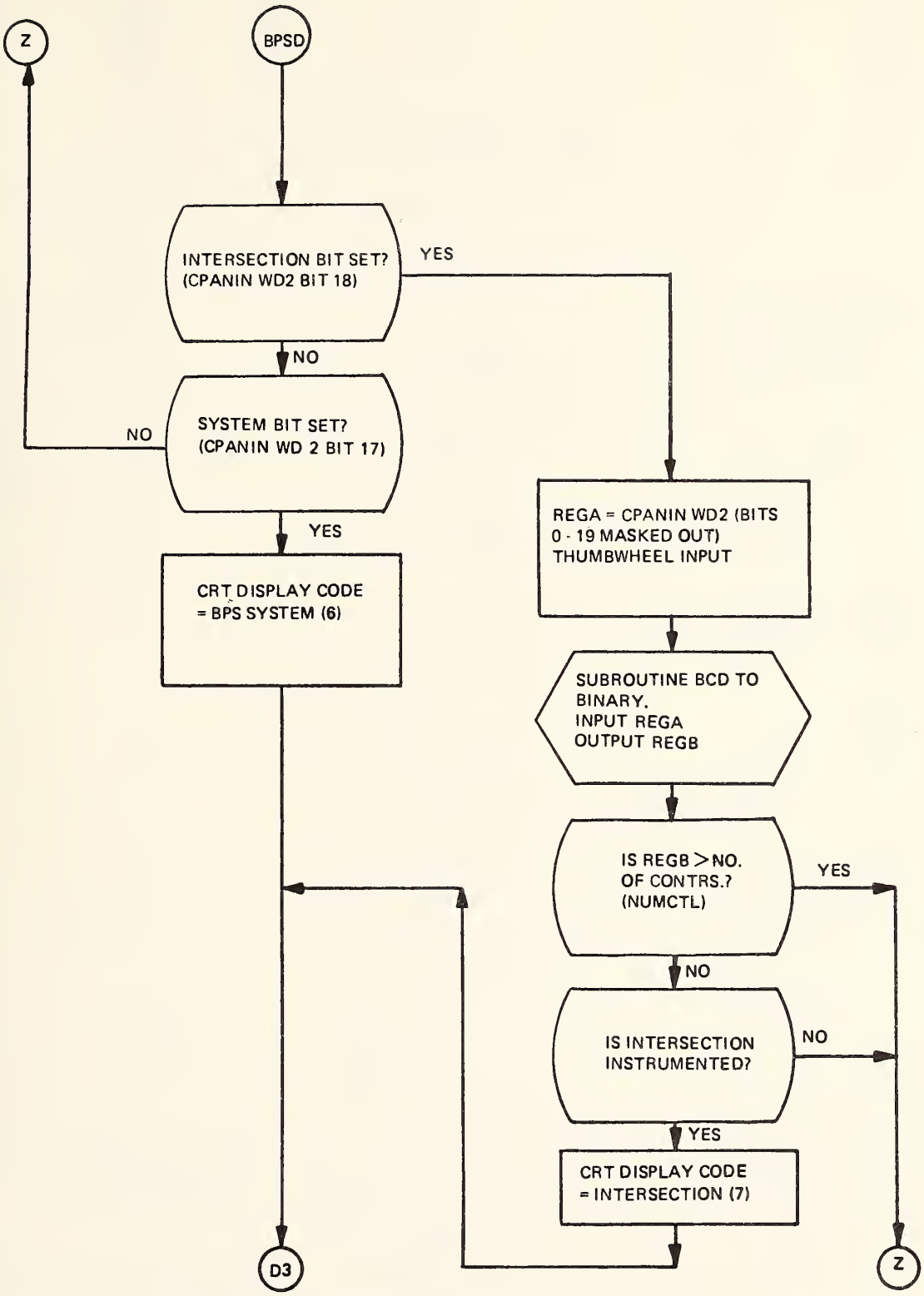


FIGURE 2.14.5.29. ROUTINE M SPECIFICATION

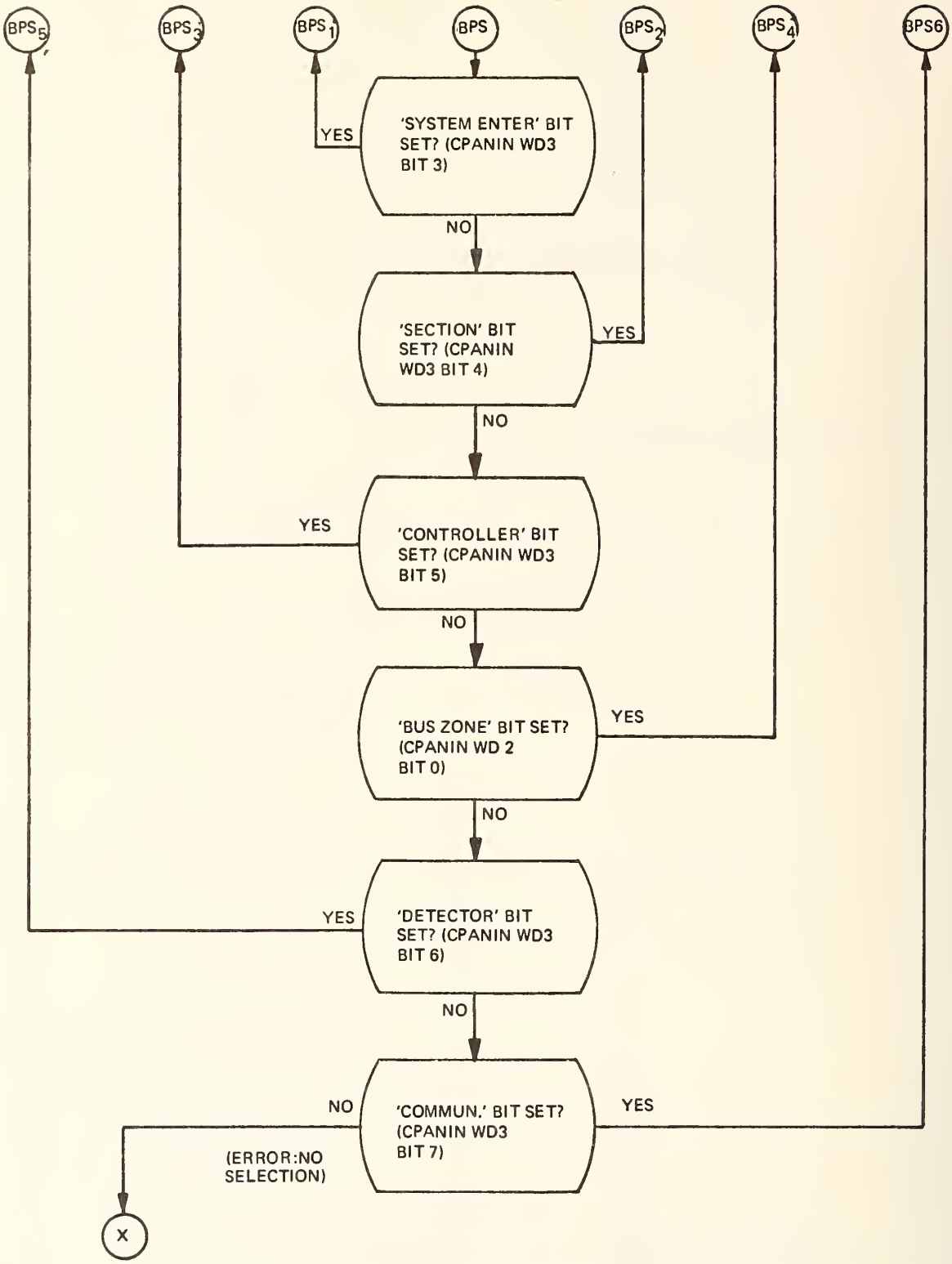


FIGURE 2.14.5.30. ROUTINE M SPECIFICATION

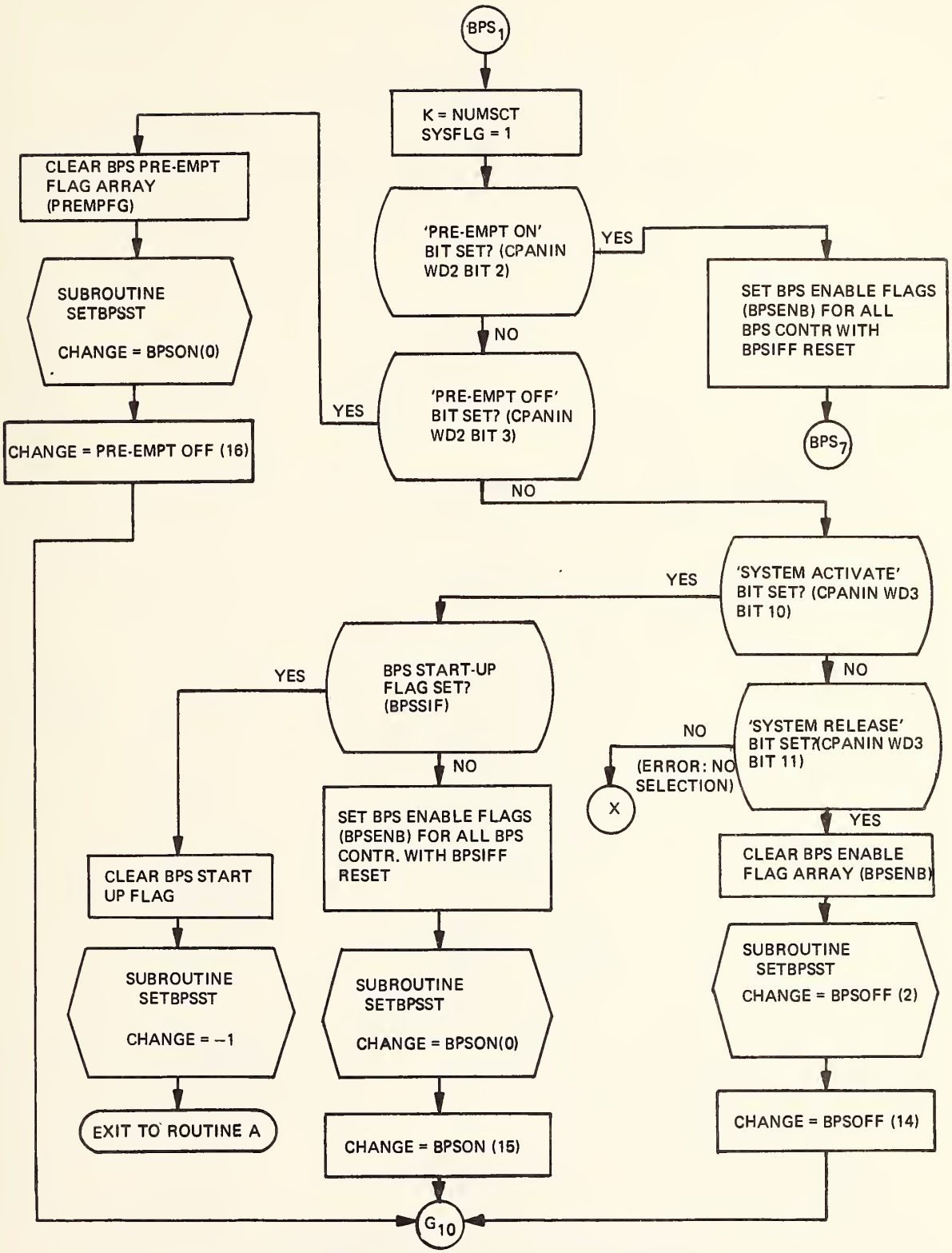


FIGURE 2.14.5.31. ROUTINE M FLOW CHART

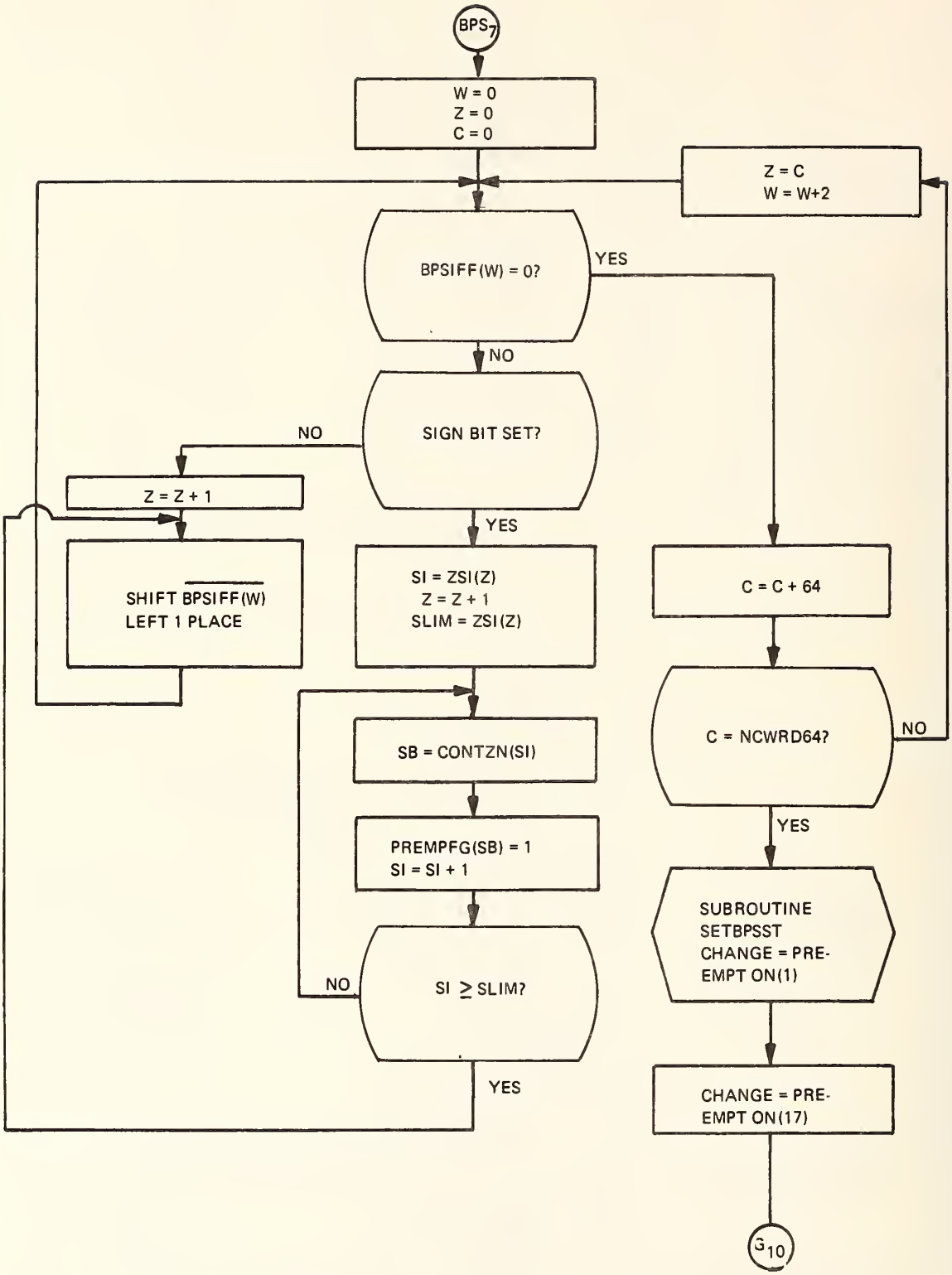


FIGURE 2.14.5.32. ROUTINE M FLOW CHART

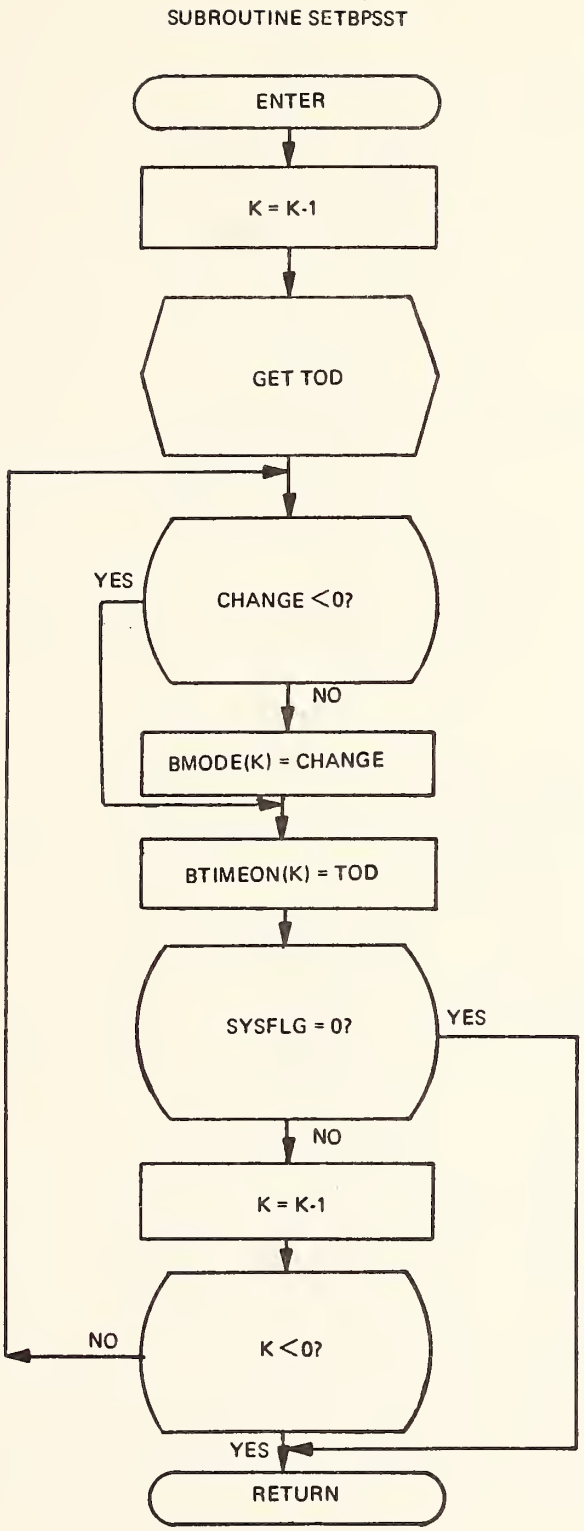


FIGURE 2.14.5.33. ROUTINE M SPECIFICATION

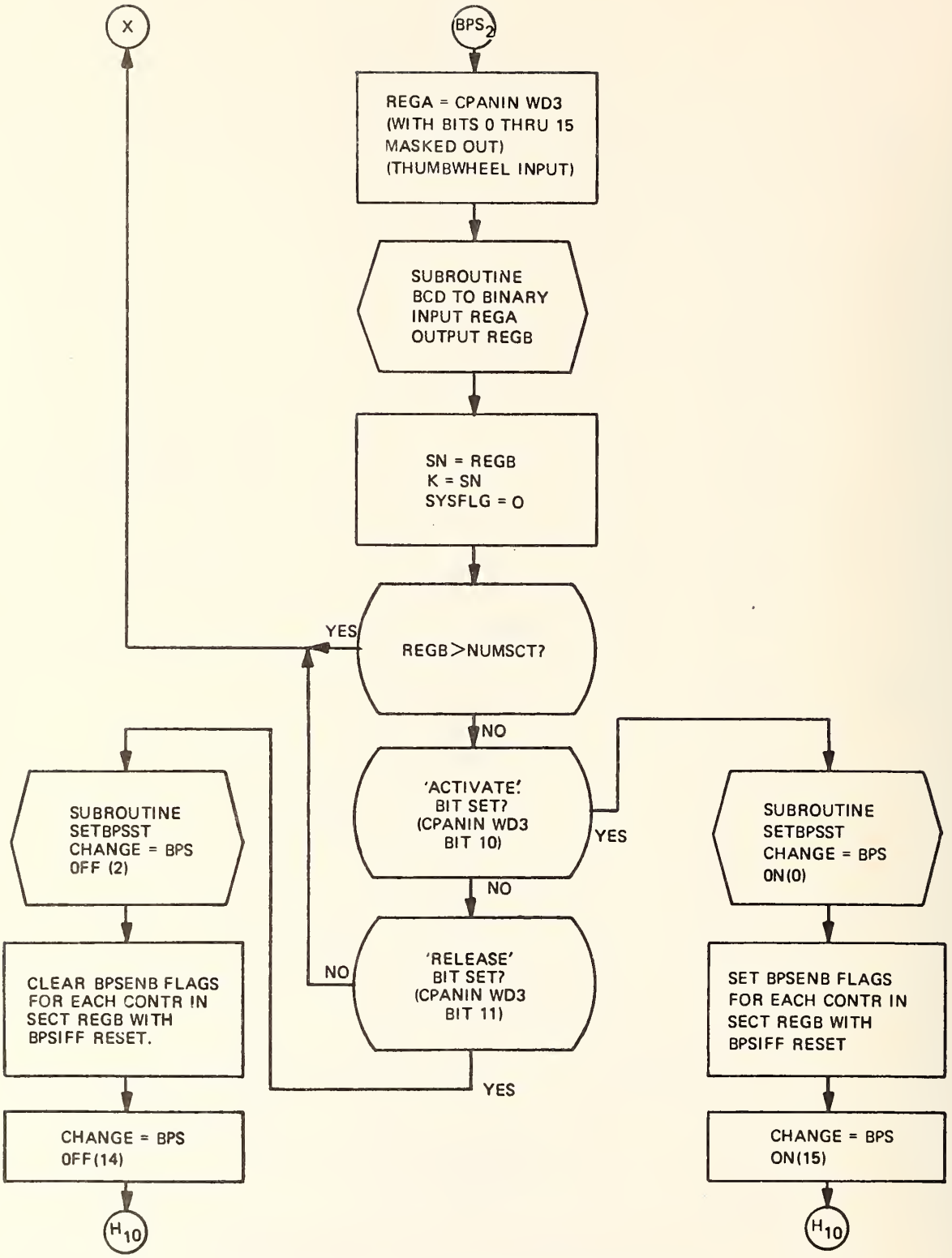


FIGURE 2.14.5.34. ROUTINE M SPECIFICATION

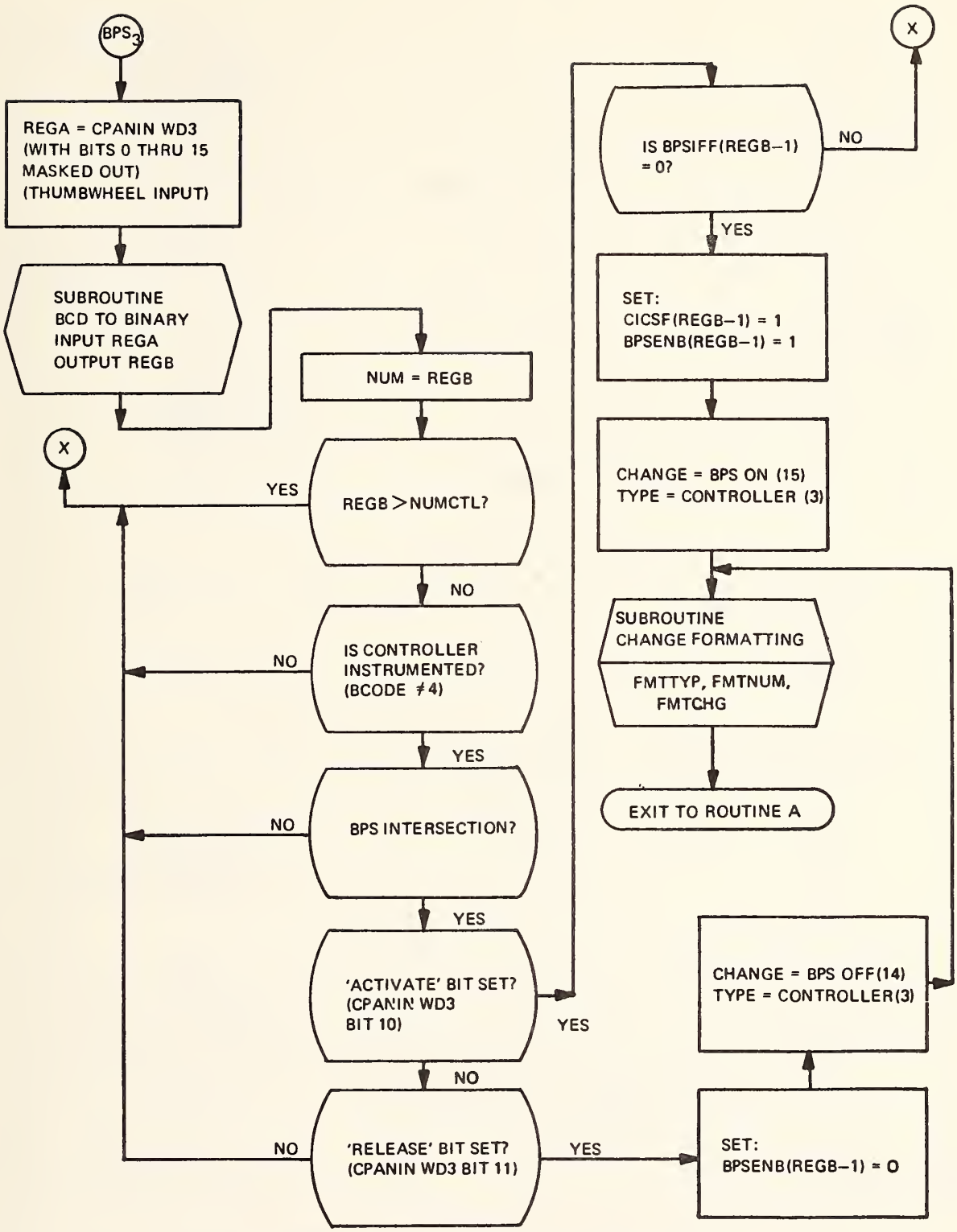


FIGURE 2.14.5.35. ROUTINE M SPECIFICATION

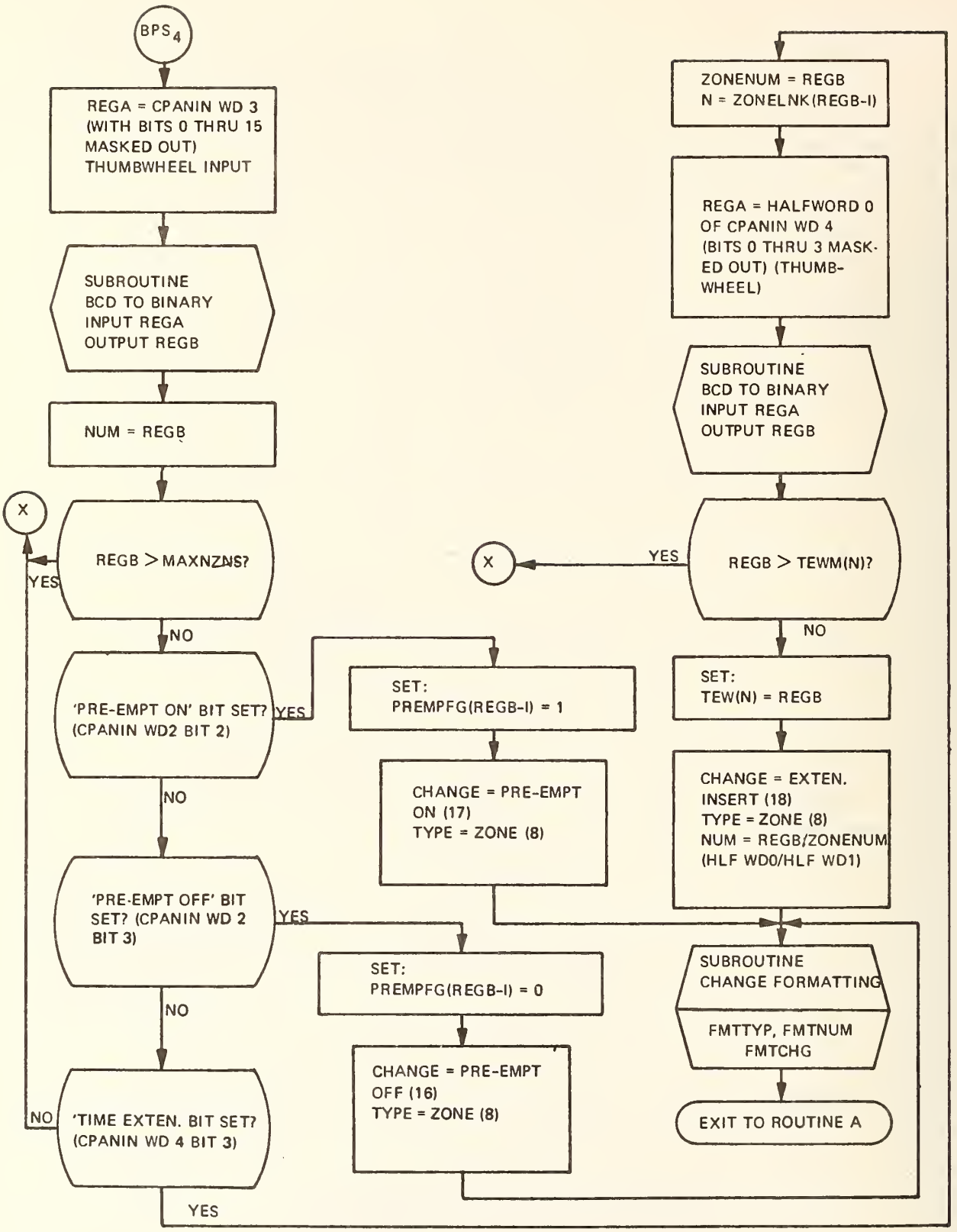


FIGURE 2.14.5.36. ROUTINE M SPECIFICATION

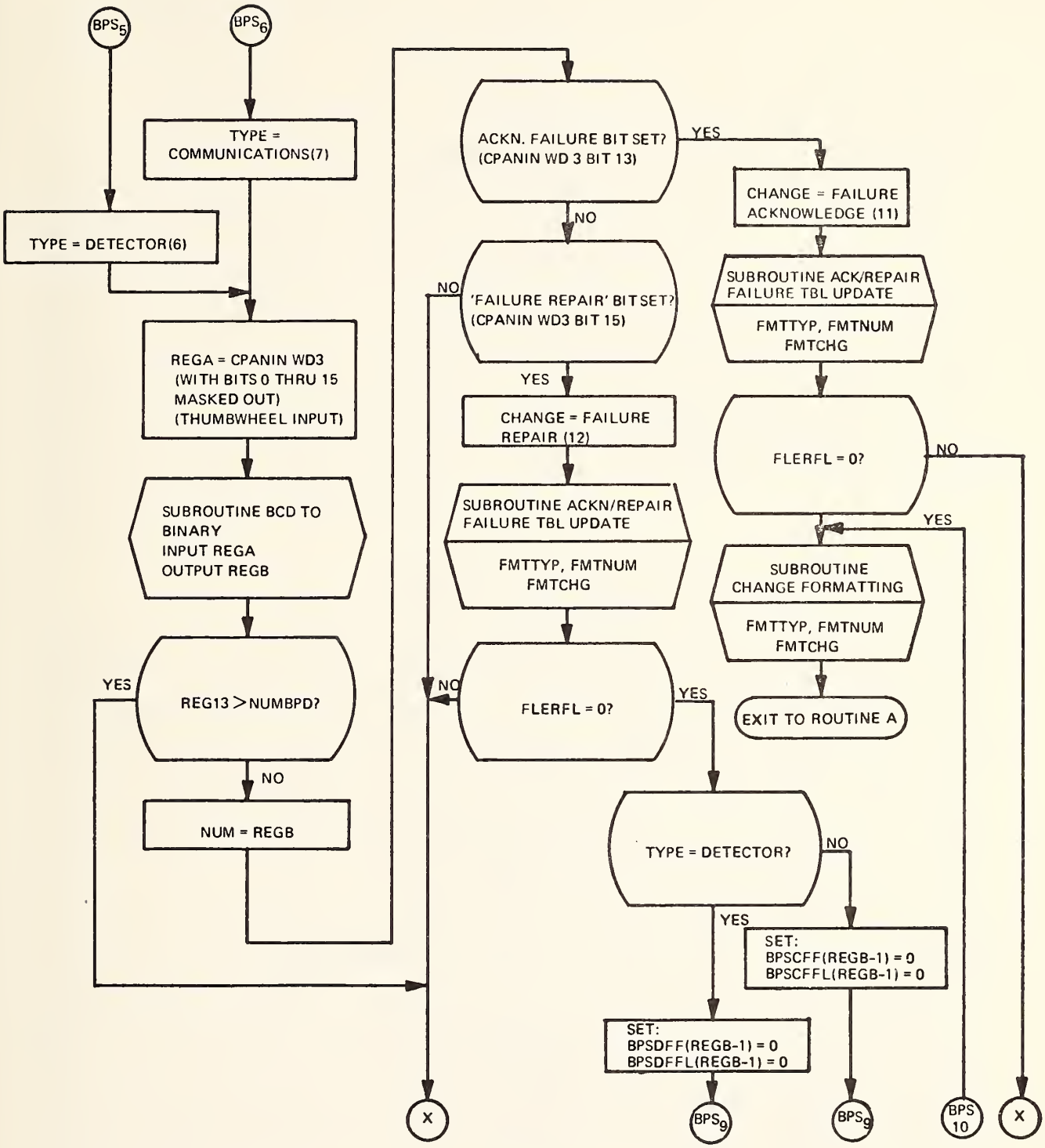


FIGURE 2.14.5.37. ROUTINE M SPECIFICATION

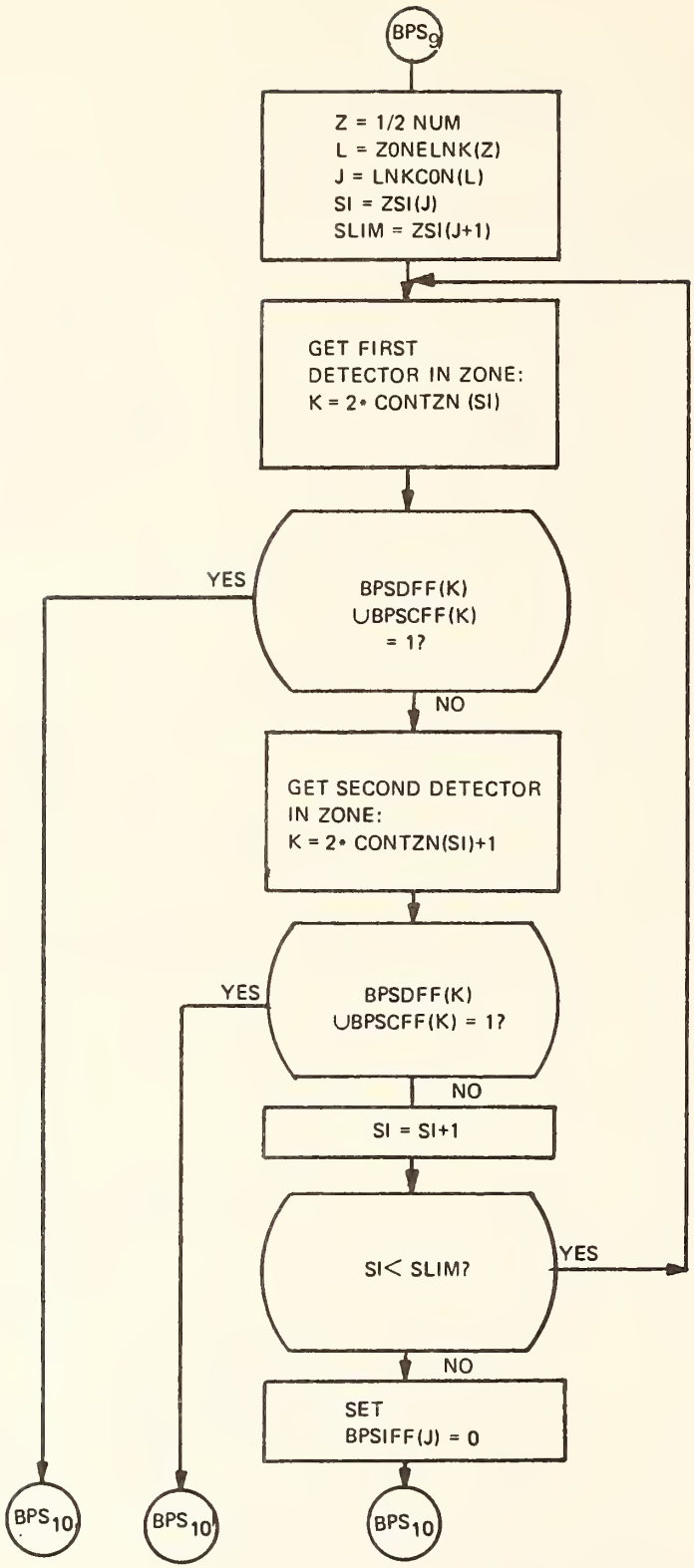


FIGURE 2.14.5.38. ROUTINE M SPECIFICATION

2.15 Routine N (Traffic Cycle Time-Keeping) Specification

2.15.1 Purpose

The purpose of Routine N is to time all possible controller cycle lengths that can be slected for on-street use. It sets a flag, once per cycle, for each cycle length being timed. These flags are used and reset in Routine E. As part of the start-up procedure, it attempts to synchronize the start of each cycle with the corresponding cycle timing reference from the District's system. As soon as a particular cycle length has been synchronized, timing of that cycle begins. If all cycle lengths have not been synchronized after 125 seconds from start-up, timing of the remaining cycle lengths begins. This is carried out since the longest cycle length in the District is 120 seconds. In addition, once per cycle length, the routine checks to see if cycles that previously were not in synchronism are now synchronized, and if cycles that were previously in synchronism are now out of synchronism. A flag is set for each cycle length to indicate its state of synchronism. These flags are used for display purposes on the CRT.

2.15.2 Method

Upon entry every half-second, the routine sets the Kth cycle time counter index, KCTCI, to the number of cycle lengths minus one, NCLM1. At start-up, modified location NMODLOC, will contain an instruction causing the program to branch to label NINITIAL, which is the initial synchronization portion of the program. At this point, the start-up time counter, NSUTC, which was intially set to 125 seconds, is decremented by 1/2 second. NSUTC is then checked to see if 125 seconds have elapsed. The first time through the routine from start-up, the routine extracts the state of a bit in the Kth cycle timing flag, KCTF. This bit is a "one" if the cycle length had previously been synchronized with the District's master controller synchronization pulses. At start-up, all bits in KCTF are set to zero. The 32 word array MASK, contains 32 one bit masks, from which 17 are used to extract the cycle lengths used in the District. MASK (K) contains a "one" in bit position K and "zeroes" elsewhere. MASK (KCTCI) is used to extract the timing flag from KCTF for cycle length number KCTCI. If the bit is present (TEMP2 > 0), subroutine CYCLTFKC is performed. Whether or not the timing subroutine is performed, KCTCI is decremented and tested to see any other cycle lengths remain to be checked for synchronization. If any remain, the procedure is repeated for each cycle length after which the routine is exited.

When 125 seconds have elapsed (NSUTC=0), the contents of NMODLOC will contain an instruction causing the program to branch and link to subroutine CYCLTFKC. This will cause the routine to bypass the initial synchronization portion of the program until after the next start-up. After 125 seconds from start-up, routine N will simply enter subroutine CYCLTFKC, a number of passes equal to the number of cycle lengths.

Upon entry, subroutine CYCLTFKC decrements the kth cycle timing counter, KCTC, for cycle length KCTCI. If this counter has not counted down (TEMP4 > 0), the subroutine is exited. Otherwise, KCTC is set to the kth cycle length value, KCL, for cycle length KCTCI. Also, the kth cycle start flag, KCSF, is set for cycle length KCTCI. At this time, the subroutine checks for synchronism. If this cycle length was not previously in synchronism but now is synchronized, the corresponding bit in KCTF is set to a "one". If this cycle length was previously synchronized but is now out of synchronism, the corresponding bit in KCTF is reset to a "zero". After the synchronism check is performed, Routine E is scheduled by setting its activity bit in MAST. After scheduling Routine E, the subroutine is exited.

2.15.3 Repetition Rate

This routine is executed once per 1/2 second for each cycle length that is being timed.

2.15.4 Cross Reference

This routine is processed at the beginning of Priority Level 2 routines. It schedules Routine E, at Priority Level 3, whenever any cycle starts. The routine exits to the next sequential Level 2 routine, A-Phase Green Processing (Routine O).

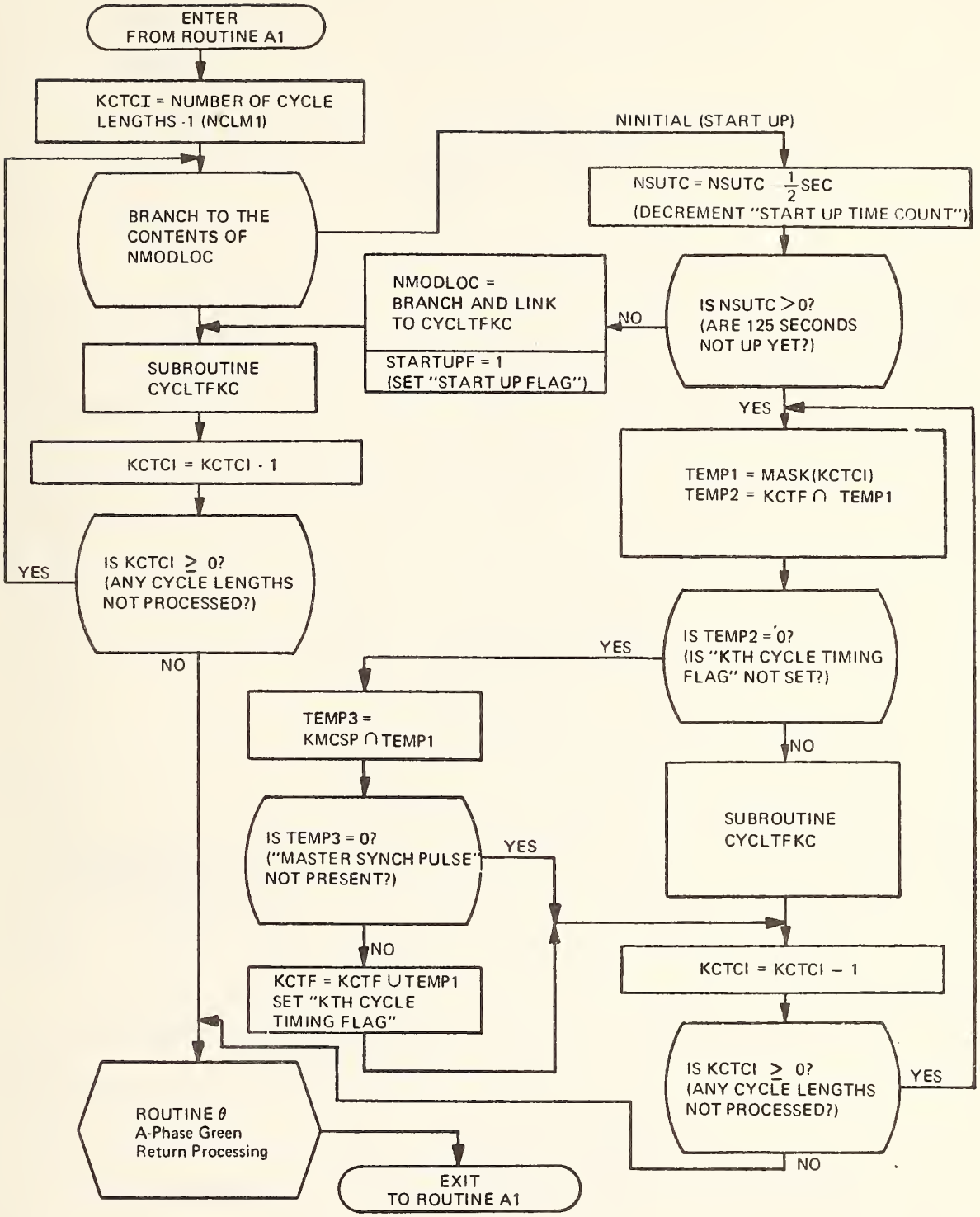


FIGURE 2.15.5.1. ROUTINE N SPECIFICATION

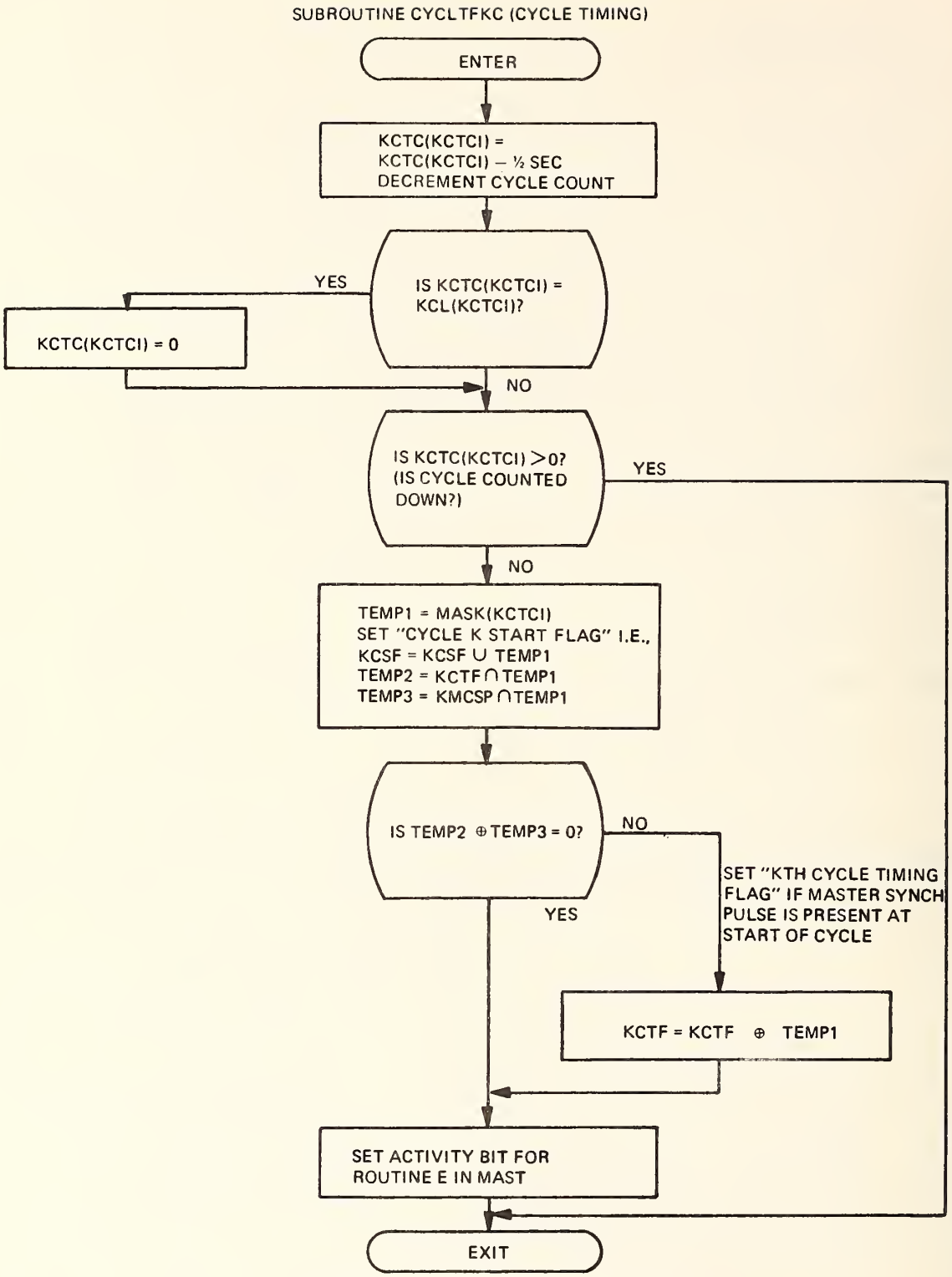


FIGURE 2.15.5.2. ROUTINE N SPECIFICATION

2.16 Routine O (A-Phase Green Return Processing) Specification

2.16.1 Purpose

The purpose of routine O is to set A-Phase Green indication bits in word AOG, and start of A-Phase Green bits in word STARTA, for each local controller.

2.16.2 Method

Upon entry every half-second, array word index (AWI) is set equal to twice the number of controller words (2NCWRD). For each controller word, the routine subsequently computes the corrected A-Phase Green Return word (AOG) and start of A-Phase Green (STARTA). This is accomplished by first indirectly storing into pointer GAP1, the one's complement of A-Phase Green return input word GAI. The input data must be complemented since the MUX supplies the data to the computer in complemented form. GAP1 points to alternate input array labels GA1 or GA2 and is initially set to label GA1. In location GT, the result of the boolean operation GA1 $\cap$ GA2 is stored for word AWI. Note that GA1 and GA2 are interleaved, where GA2(I+1)=GA1(I). The start of A-Phase Green is computed using the boolean operation (AOG $\oplus$ GT) $\cap$ GT, which is equivalent to $\overline{AOG} \cap GT$. The operation using an exclusive "OR" was chosen since the Sigma V CPU does not have a one's complement instruction. By using an exclusive "OR", one instruction is saved per operation.

After computing STARTA, AOG is calculated. The algorithm used sets controller bits in AOG to a "one" if the signal was present for two pulses in a row, i.e., GA1 and GA2 are both a "one". It also sets these bits to a "zero" if the signal was absent for two pulses in a row. Otherwise, the bits in AOG remain unchanged. This has the effect of removing a single noise pulse where no signal is present and filling in a single missing pulse when the signal is present. Note that AOG and STARTA are interleaved, where STARTA (I+1) = AOG(I). Thus, both of these quantities are referenced by even indices only.

After computing AOG, AWI is decremented by 2 and AWI is tested for completion. Upon completion of all controller words, the label in GAP1 is interchanged to the alternate buffer label, and the routine is exited.

2.16.3 Repetition Rate

This routine is executed once per 1/2 second for all local controllers.

2.16.4 Cross Reference

This routine is processed immediately following Routine N and exits to Routine A1.

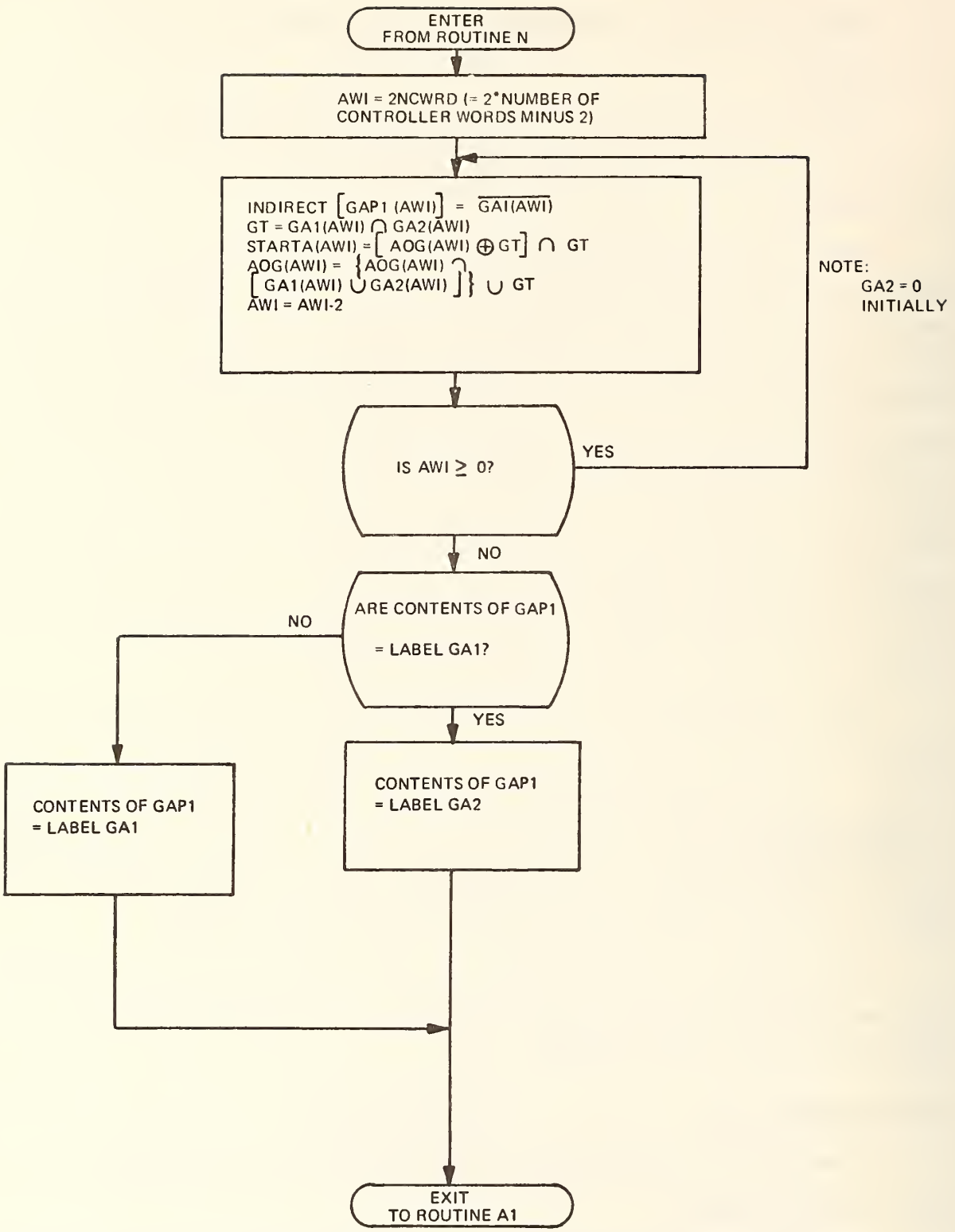


FIGURE 2.16.5.1. ROUTINE O SPECIFICATION

2.17 Routine P (Synchronization of Controller with Computer) Specification

2.17.1 Purpose

The purpose of this routine is to scan the compliment of controllers which have been flagged as being out of synchronization with the computer. If the controller is out of phase by one interval a correction is attempted, otherwise, the controller is dropped into standby.

2.17.2 Method

Routine P is the first routine in the Controller Do-Loop (defined in Routine A1, Do-Loop Routine) and is scheduled by the Do-Loop Routine whenever it determines there is a controller out of phase. Routine A1 then passes a bit configuration (in register 8), representative of 32 controllers, to Routine P for processing. This routine then scans for a "1" in any bit position of the register - indicating a faulted controller. For each "1" detected, this routine determines if the corresponding controller is leading or lagging the computer.

If the controller is found to be lagging, a timeout procedure is initiated with a 3 second duration. If the controller is still lagging after timeout, an advance pulse is sent to the controller and a 1.5 second timeout is initiated. If the controller is still found to be lagging after this period, it is dropped into standby and the CRT Failure Table is appropriately updated.

When a controller is found to be leading the computer a test is made to determine if it is more than one interval out of phase. If it is out of phase by more than one interval, it is dropped into standby. Otherwise the next advance pulse to the controller is inhibited.

Routine K, CRT Failure Table Update, is called as a subroutine if a controller is dropped into standby.

2.17.3 Repetition Rate

This routine is executed once per 1/2 second for every controller out of phase.

2.17.4 Cross Reference

This routine is the first routine in the Controller Do-Loop and is executed at Priority Level 2. It is called by the Level 2 Exec.

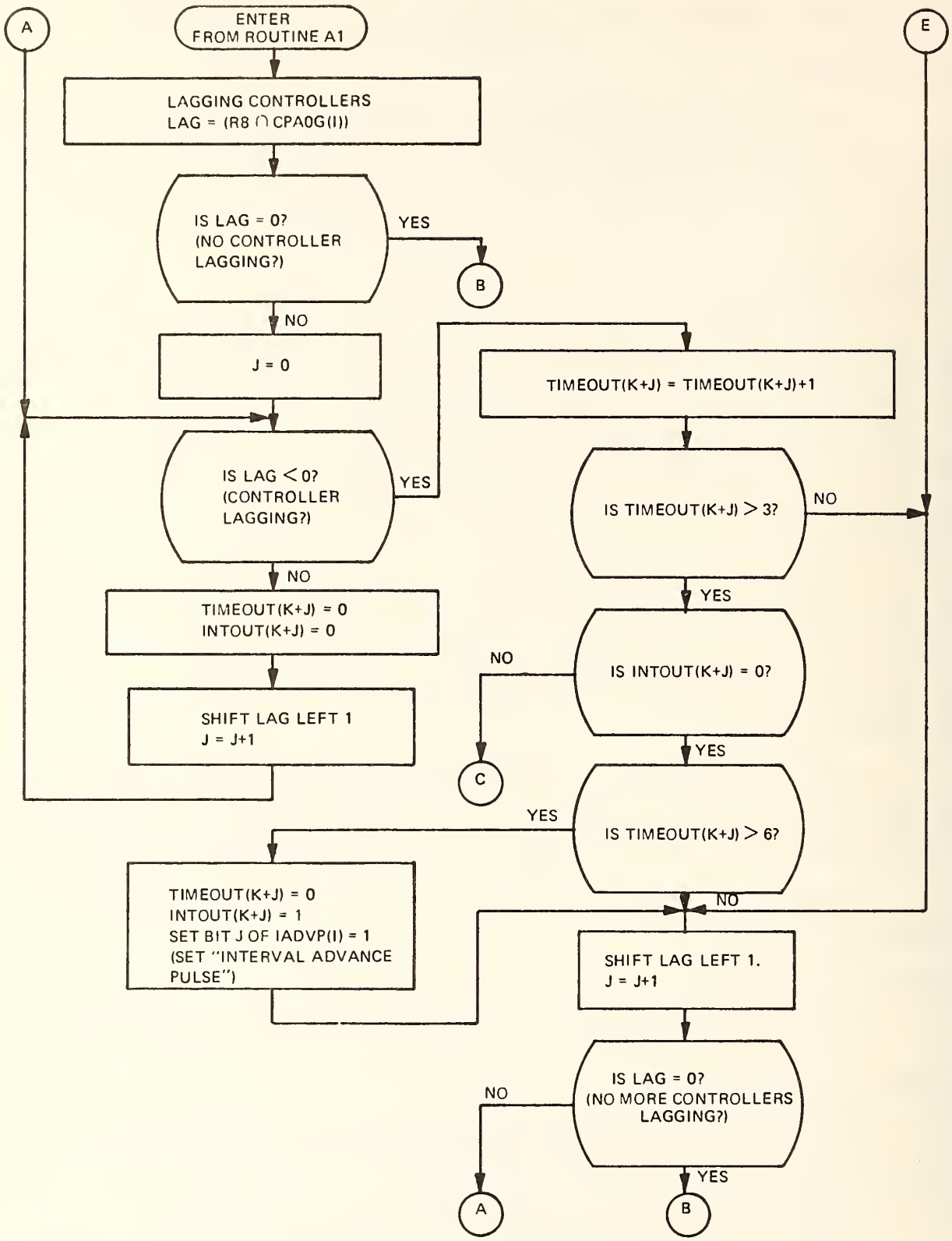


FIGURE 2.17.5.1. ROUTINE P SPECIFICATIONS

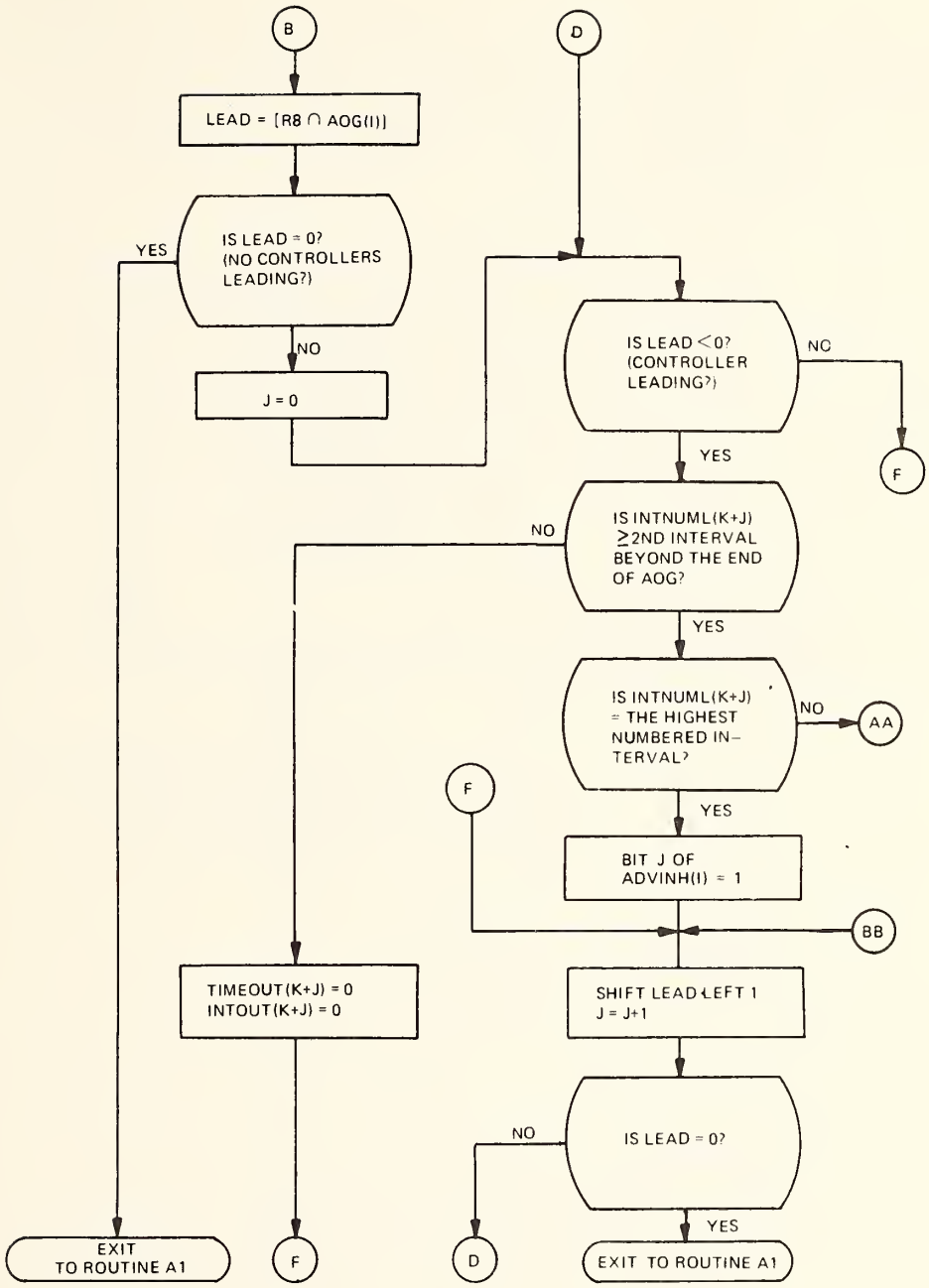


Figure 2.1.7.5.2. Routine P Flow Chart (Sheet 1 of 2)

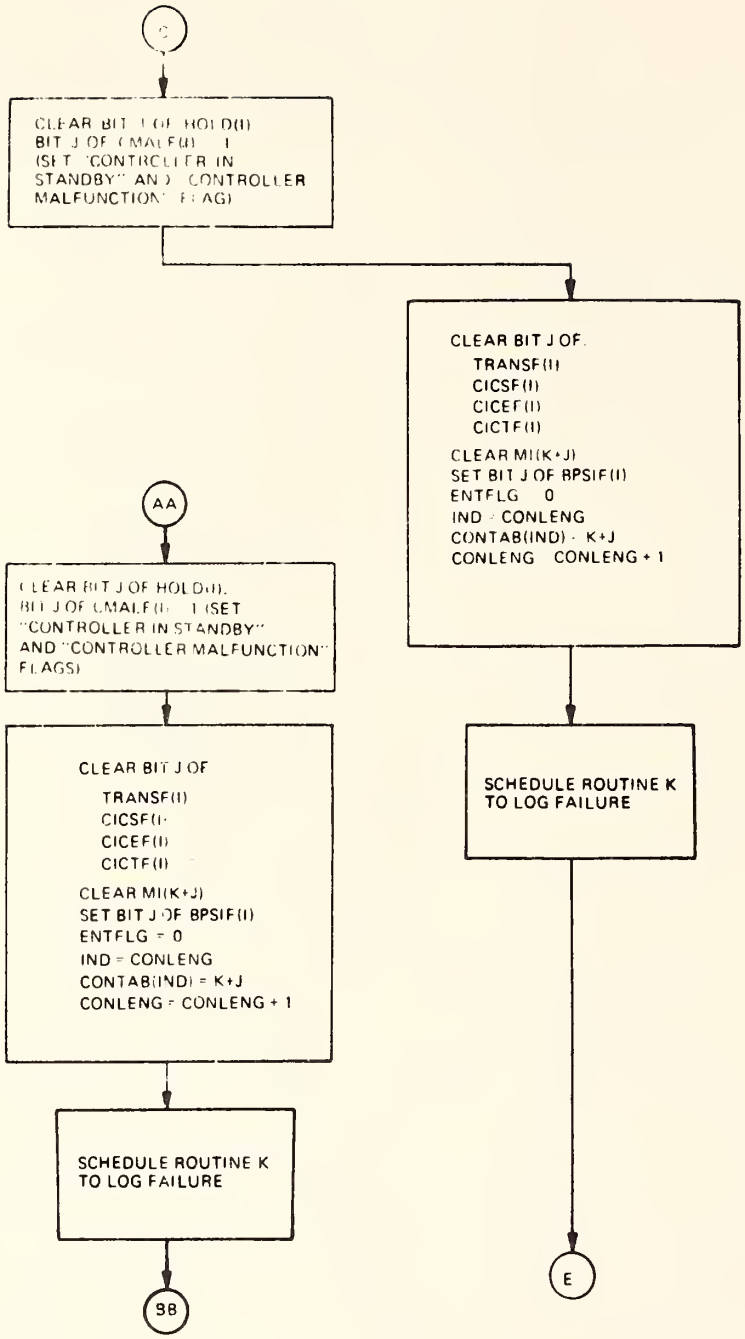


Figure 2.1.7.5.2. Routine P Flow Chart (Sheet 2 of 2)

2.18 Routine Q (Shutdown) Specification

2.18.1 Purpose

The purpose of the Shut Down Routine is to store data on the RAD required for the next start-up, and to return control to RBM for batch processing when the entire UTCS system has completed its shutdown tasks.

2.18.2 Method

Two entries are required to complete the shut down procedure. The first is initiated by Routine I which schedules Routine Q upon finding the shut down flag (SHTFLG) set. The first entry requests that all controllers be dropped into standby. It then sets a scheduler clock (QCNT) to 180 seconds and exits to Routine A. When Routine A decrements the clock to zero, Routine Q is re-scheduled for the second pass. The second entry stores the required arrays (See Figure 2.18.5.1) on the RAD and releases the the UTCS program.

2.18.3 Repetition Rate

The Shut Down Routine is entered on demand whenever shutdown is requested by the operator.

2.18.4 Cross Reference

This routine is scheduled by Routine I initially.

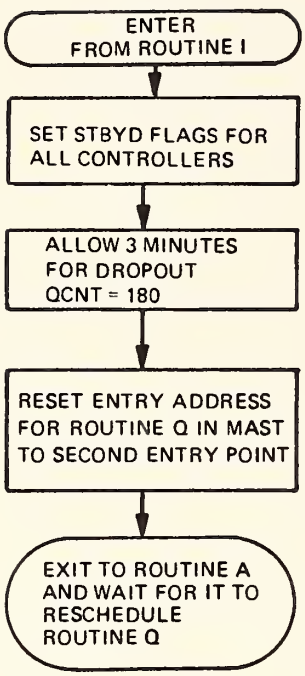
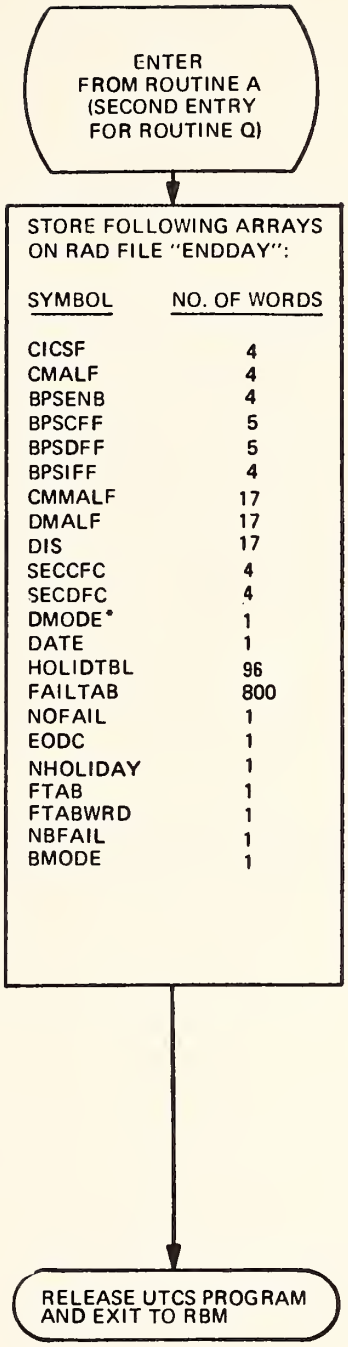


FIGURE 2.18.5.1. ROUTINE Q SPECIFICATION



*DMODE MAY BE ALTERED DURING SHUTDOWN. ALL MANUAL REQUESTS ARE CHANGED TO TOD REQUESTS

FIGURE 2.18.5.2. ROUTINE Q SPECIFICATION

2.19 Routine R (Transformation From Computer Control to Standby) Specification

2.19.1 Purpose

This routine will effect the transition of a non-semi-actuated controller from computer control to standby, upon operator request.

2.19.2 Method

Routine R is the second routine in the Controller Do-Loop and is scheduled, unconditionally, after the termination of Routine P. As with other routines in this loop, Routine R processes 32 controllers per entry. When an operator request to drop a controller is encountered, (STBYD (I) $\neq$O) the routine scans for the start of A-Phase Green (STARTA) for the selected controller. When the A-Phase Green return is detected, a timeout (STBTIM) of 7.5 second duration is initiated. If the request is still standing at the end of this period, the controller is dropped into standby.

2.19.3 Repetition Rate

This routine is scheduled once per 1/2 second at Priority Level 2.

2.19.4 Cross Reference

This routine is executed as part of the overall Priority Level 2 routines. It is entered upon completion of Routine P and exits to the Routine A1.

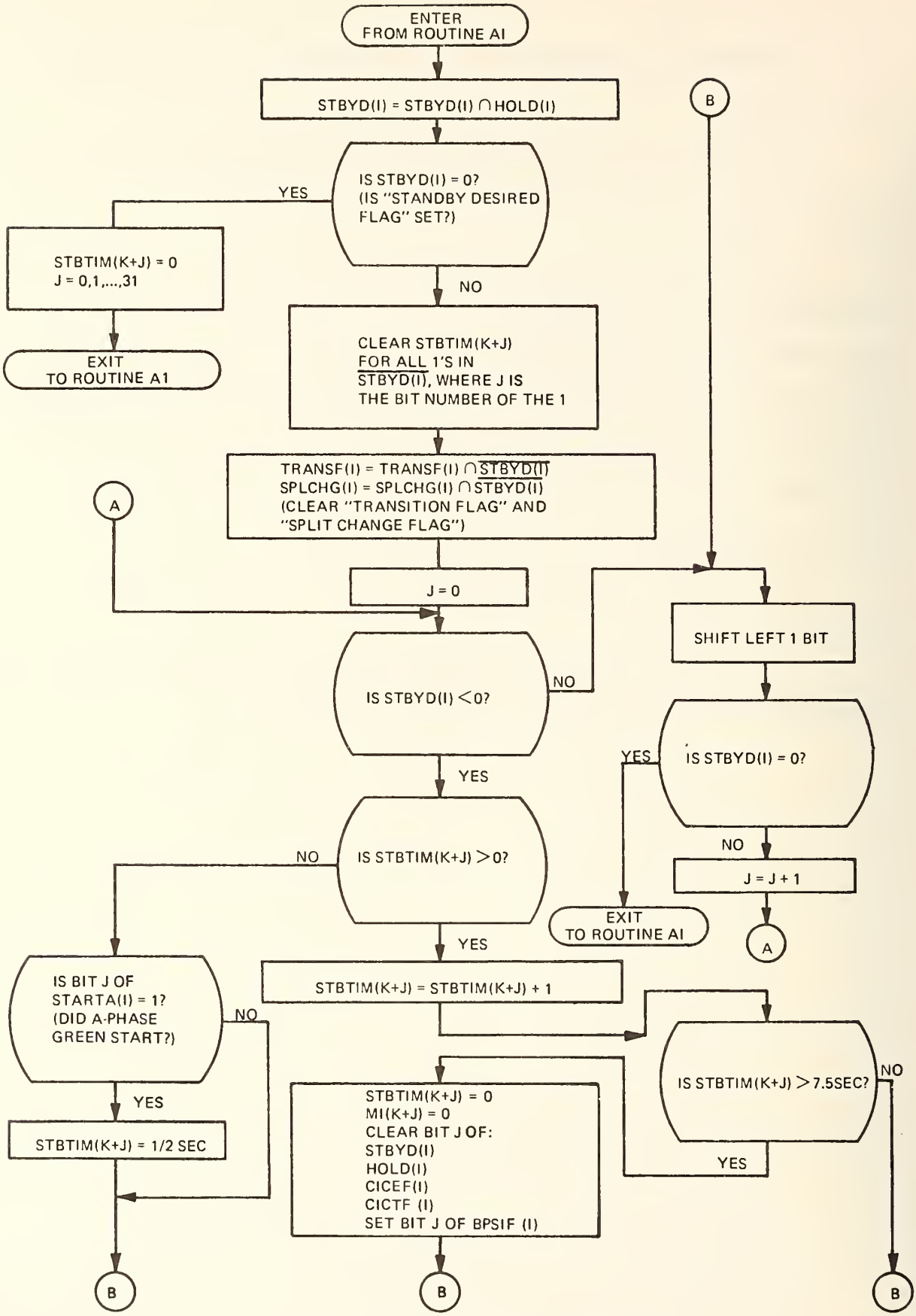


FIGURE 2.19.5.1. ROUTINE R SPECIFICATION.

2.20 Routine S (Transition) Specification

2.20.1 Purpose

Routine S computes the required parameters to allow a smooth transition from one area pattern to another. It preserves all safety intervals; utilizes the newly selected split for the major phases at the controller; and contains the transitional cycle length to a value between the minimum used in the section and twice that number. The transformation occurs in the minimum time subject to the following conditions: A transition can be initiated by any of the following two conditions:

a) Controller being transferred from standby to computer control.

b) A new pattern has been selected for the section containing this controller.

Upon detection of any of these conditions the routine will compute:

a) number of intermediate cycles required

b) the intermediate cycle length

c) the intermediate variable interval durations

2.20.2 Method

This routine is entered at the start of A-Phase Green if any one of the two conditions summarized in Section 2.20.1, Purpose, is present. The routine will perform the following computations.

1. The difference, DOFF, between the present offset and the desired new offset will be computed.

2. If negative, DOFF will be converted to its positive equivalent.

3. If the magnitude of DOFF is less than three seconds, no transitional cycles will be required.

4. If DOFF is greater than three seconds, either one or two intermediate cycles, whose cycle length is greater than a prescribed minimum value and less than twice that value, will be generated.

5. If there are more than two adjustable interval durations at the controller (or more than three for a Type B multiple-phase critical intersection controller), all of those intervals above this number will be set to a defined minimum value.

6. The split during the transitional cycles will be apportioned according to the following logic:

a. The durations of all safety intervals will be maintained.

b. The adjustable interval durations associated with all the minor movements will be set equal to their respective minimum values. The residual cycle time will be apportioned to the two or three major movements according to the procedure below.

c. The split for these two or three major movements will be set equal to that value which will be used after the transitional cycles have been completed.

7. After the transitional cycle adjustable interval durations have been completed and stored in "Working Storage", Routine G, Controller-Link Cross Reference and Timing, will be called in order to adjust the MOE Period durations required for detector data processing.

2.20.3 Repetition Rate

This routine is called when required by Routine T.

2.20.4 Cross Reference

This routine is incorporated in the system as a subroutine. It is called exclusively by the Interval Advance Routine, Routine T. It calls Routine G as a subroutine.

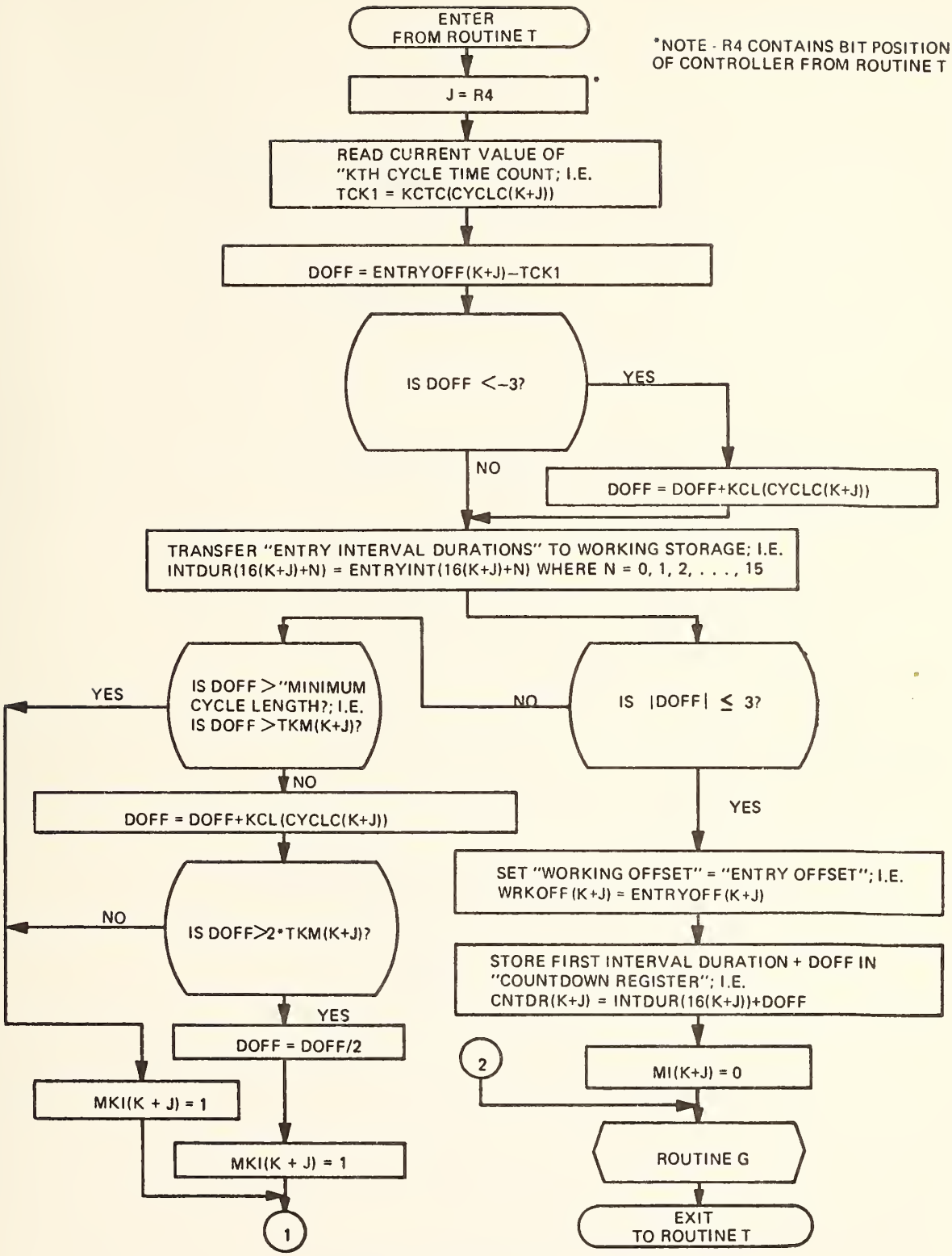


FIGURE 2.20.5.1. ROUTINE S SPECIFICATION

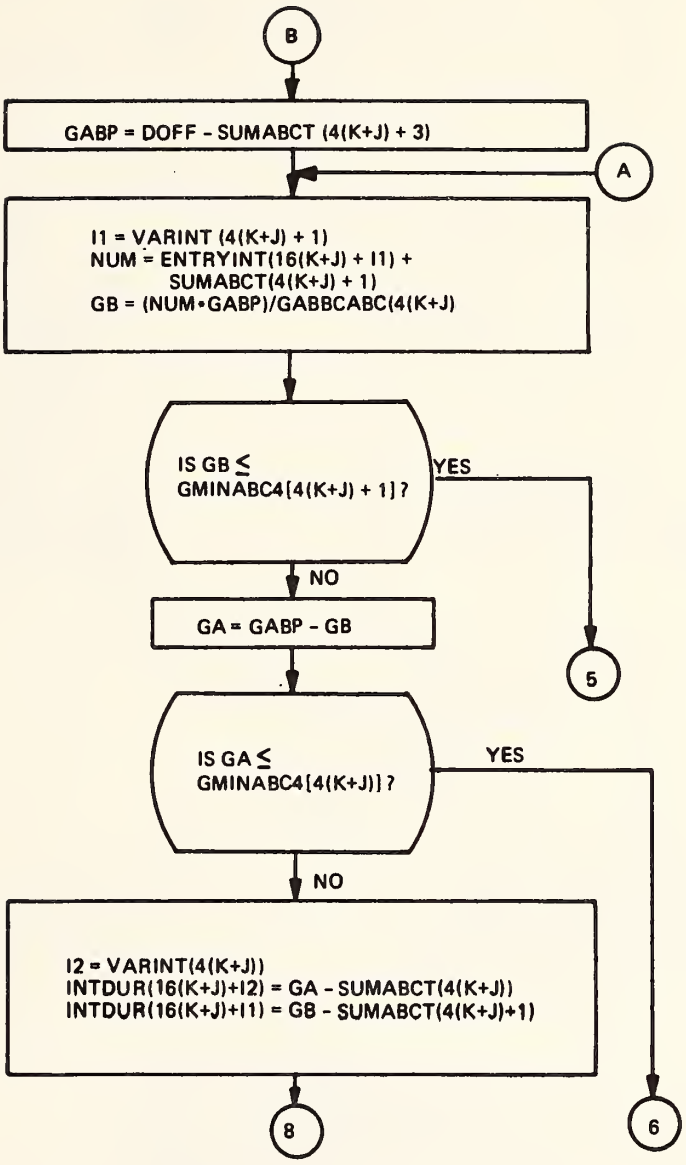


FIGURE 2.20.5.2. ROUTINE S FLOW CHART

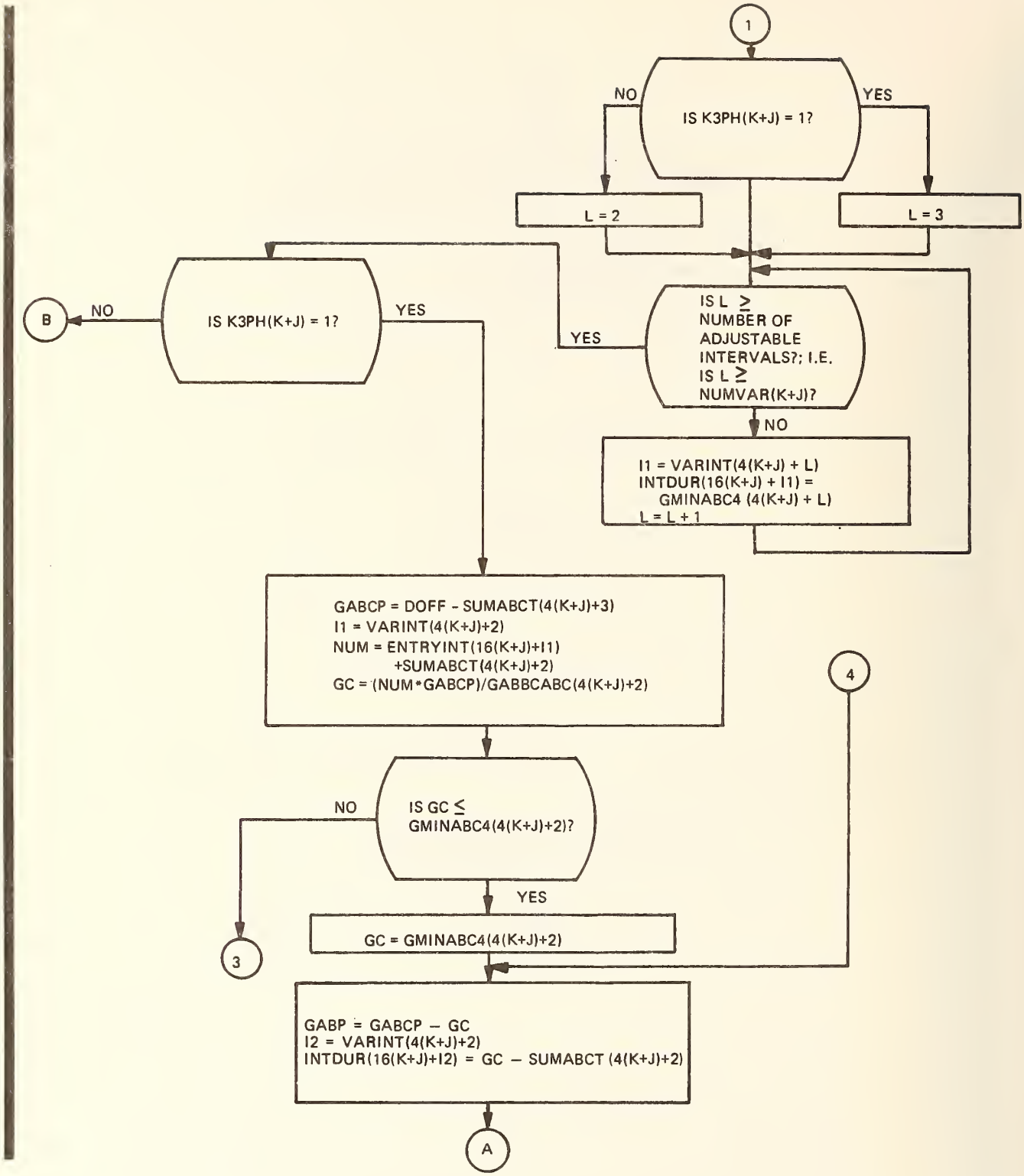


FIGURE 2.20.5.2. ROUTINE S FLOW CHART

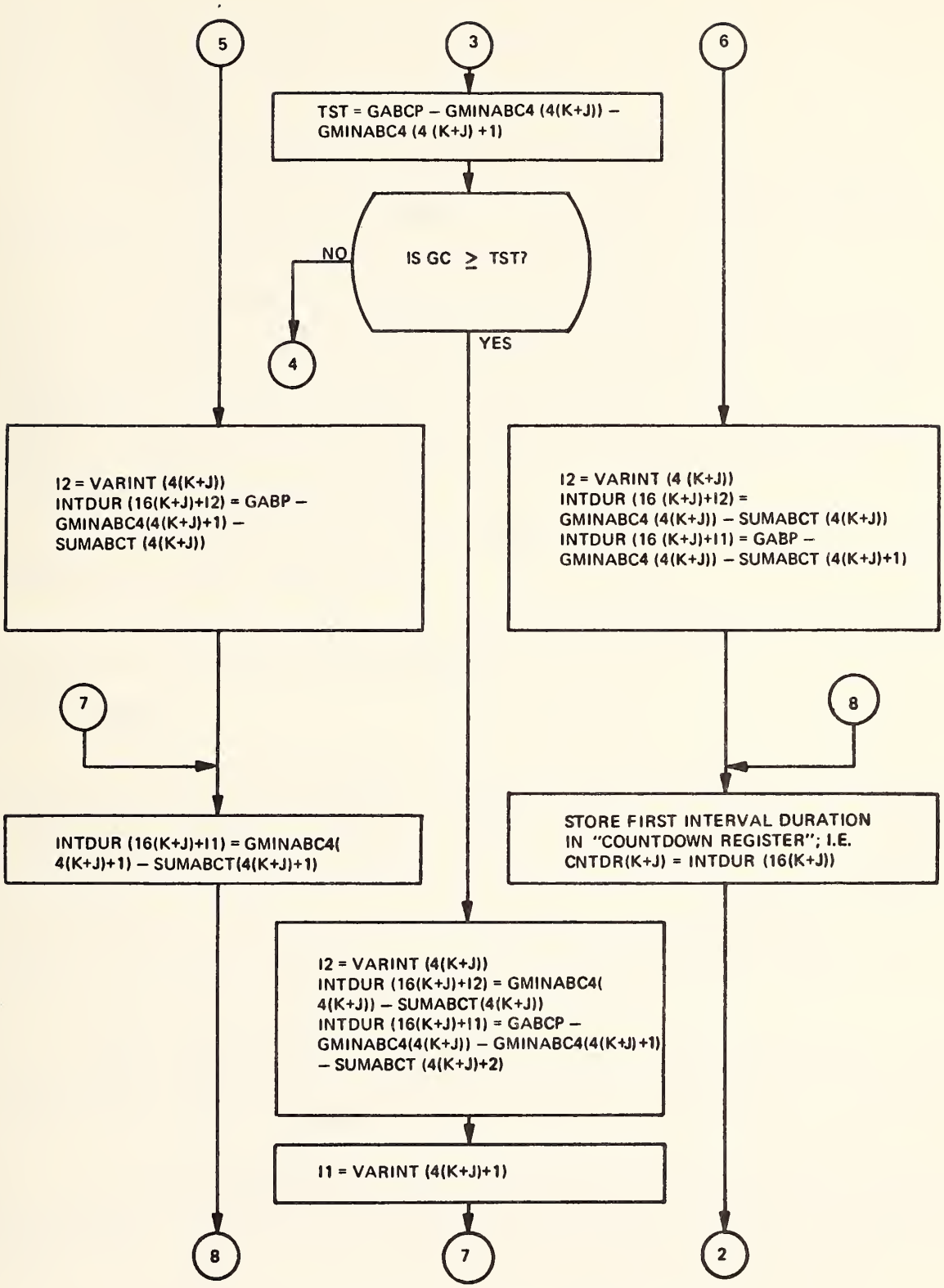


FIGURE 2.20.5.3. ROUTINE S SPECIFICATION

2.21 Routine T (Interval Advance) Specification

2.21.1 Purpose

The primary functions of this routine are as follows:

a) Establish and impose the necessary transition cycles to transform a controller from standby to computer control. This transition is initiated at the start of A-Phase Green provided the necessary input conditions are satisfied.

b) Count down, by subtracting 1/2 second per pass through the routine, the interval durations for those controllers under computer control. When the count goes to ZERO the interval number is incremented by 1 and tested for the maximum. If the maximum is exceeded, the interval number is reset to 1 and the count down register is initialized to the first interval duration. Otherwise, the next interval duration is stored into the count down register.

c) Provide the capability to incorporate operator selected values of split or offset at the start of interval one.

d) Provide the necessary logic to incorporate BPS extensions by reducing specified interval durations for a given cycle.

2.21.2 Method

This routine checks for the presence of the "Automatic Control Desired Flag" for those controllers which are in standby. If these conditions are met, the controller will be placed under computer control at the beginning of the next A-Phase Green. At this time, the "Automatic Control Desired Flag" will be cleared, and the interval number count will be initiated at 1. The next step is call of Routine S, Transition Routine, which will compute the required intermediate cycle, split, and offset to effect the change to the computer-selected cycle, split, and offset.

Under normal computer control, this routine will decrement an interval "Count-Down Register" every 1/2 second until zero is reached. At this time the following sequence of events will be initiated:

1. If the "Advance Pulse Inhibit Flag" (ADVINH) has not been set by Routine P, Synchronization of Controller with Computer, the "Interval Advance Pulse" (IADVP) will be set.

2. If the "Advance Pulse Inhibit Flag" is set, it will be cleared at this time, and no "Interval Advance Pulse" will be transmitted.

3. The "Interval Count" will be updated by one and will be checked for exceeding the highest numbered interval.

4. If the highest numbered interval has not been exceeded, the next interval duration will be stored in the "Count-Down Register" (CNTDR). If the highest numbered interval has been exceeded, the "Interval Count", (INTNUM) will be reset to one, and some combination of the following six functions will be performed.

- Transitional cycle(s) will be initiated to transfer to a new selection of cycle, split, and offset if the "Transition Flag" (TRANSF) is set. These flags are set whenever a new timing pattern is being imposed.

- A transition already in effect will be continued for one additional cycle if the MI count is non-zero. There will be a maximum of two intermediate cycles. The MI count is determined by computations in Routine S and is indicative of the minimum number of cycles necessary to impose the selected timing pattern on a given controller.

- An operator split change will be introduced if the "Operator Split Change Flag" (SPLCHG) is set, and a transition is not in effect as evidenced by the "Transition Flag" or the MI count.

- An operator offset change will be introduced at this time, by calling Routine U, if new offset data has been selected, and a transition is not in effect. It should be noted that a transition will override either an operator split selection or an operator offset selection.

- Any cumulative offset error which has accrued over the preceding cycle will be adjusted at this time by calling Routine U, Offset Correction Routine, provided the program is not in a transitional cycle.

- Routine G, Controller - Link Cross Reference and Timing, will be called whenever controller interval data has been changed as a result of either Routine S, Transition Routine, or Routine M, Manual Control Panel Processing.

2.21.3 Repetition Rate

Routine T is part of the Level 2 do-loop and is executed every 1/2 second.

2.21.4 Cross Reference

Routine T may call the following routines:

a) Routine S - Transition Routine

b) Routine U - Offset Correction Routine

c) Routine G - Controller Link Cross Reference and Timing Routine.

It is entered after Routine R and exits to Routine A1.

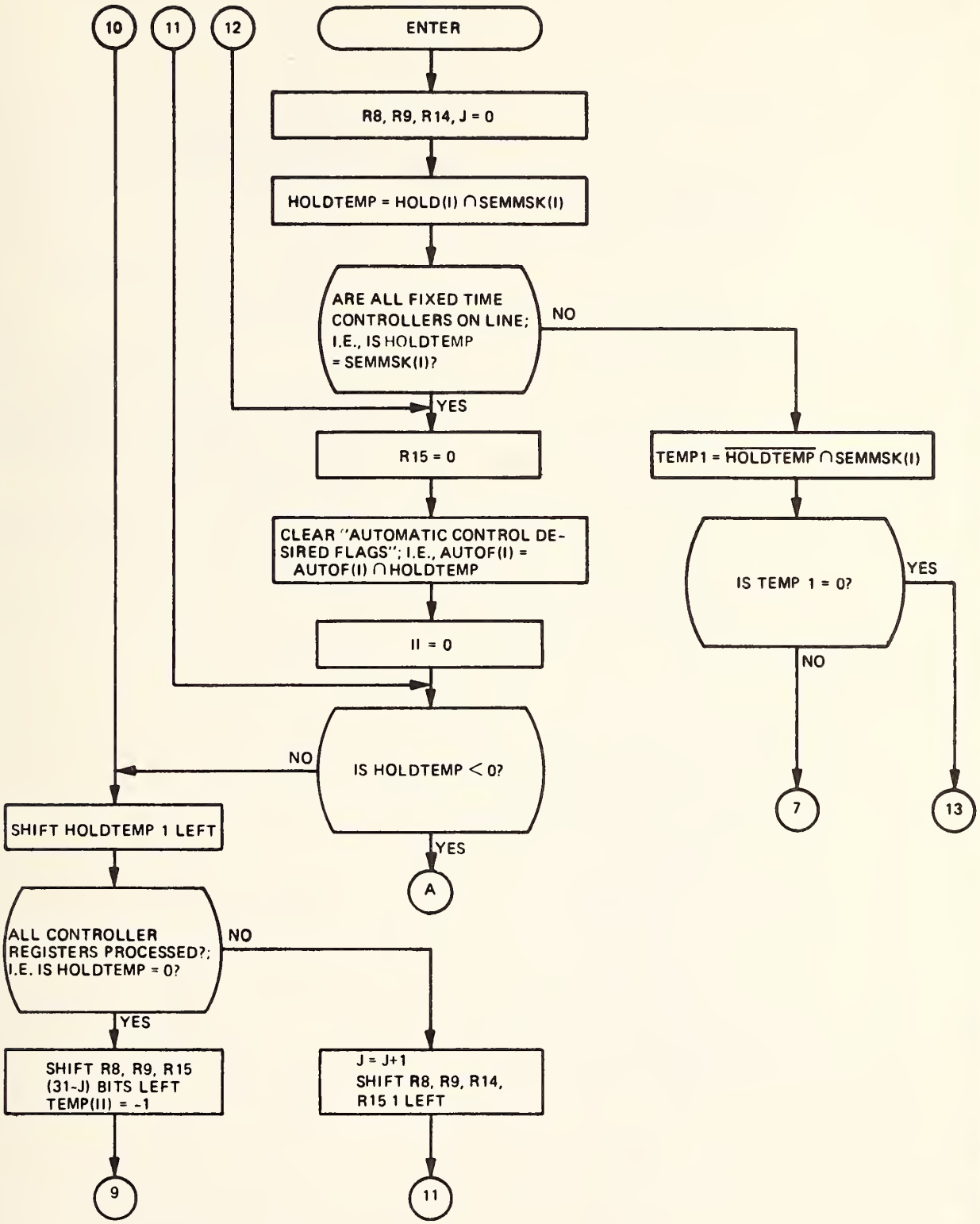


FIGURE 2.21.5.1. ROUTINE T FLOW CHART

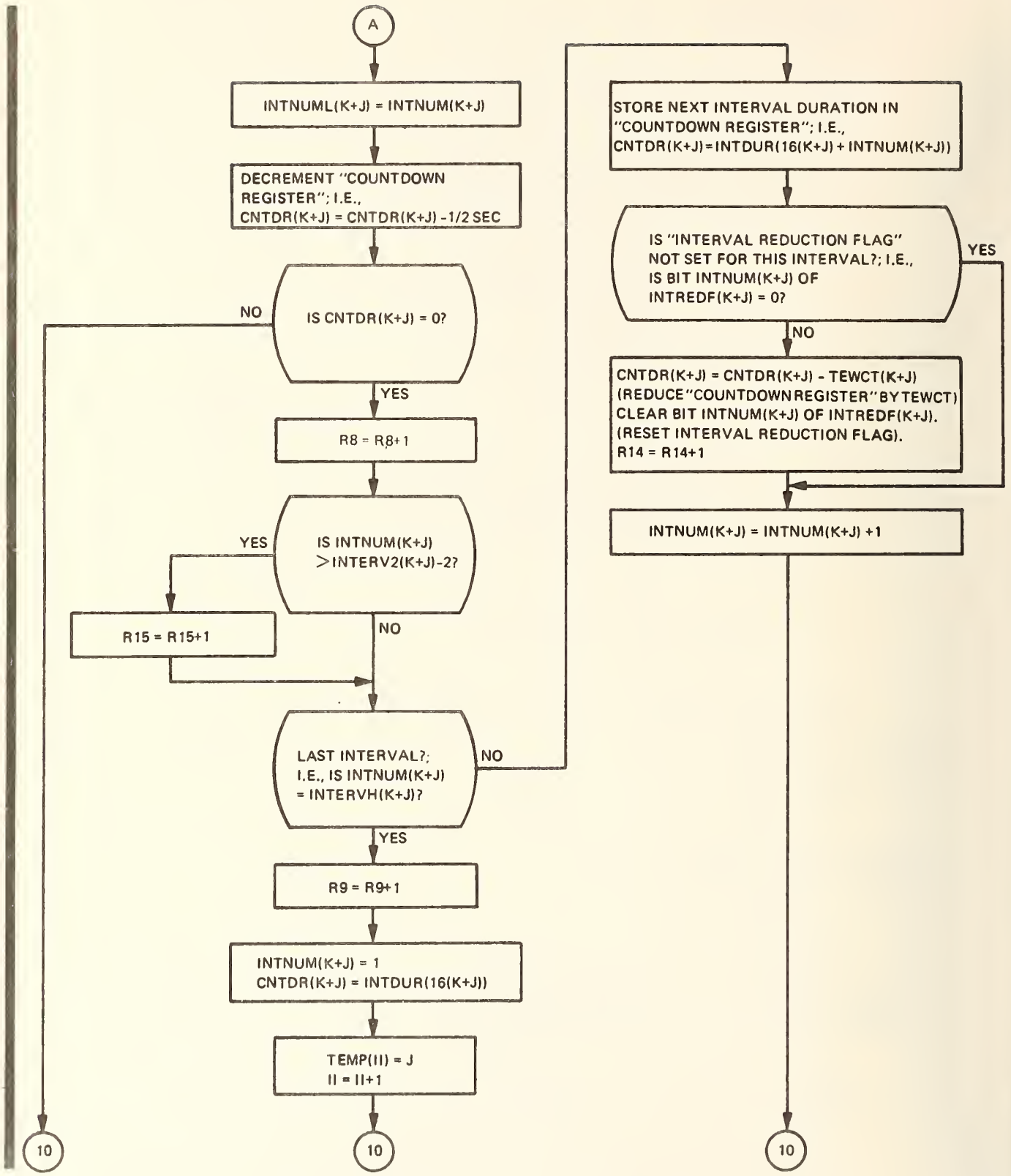


FIGURE 2.21.5.1. ROUTINE T FLOW CHART

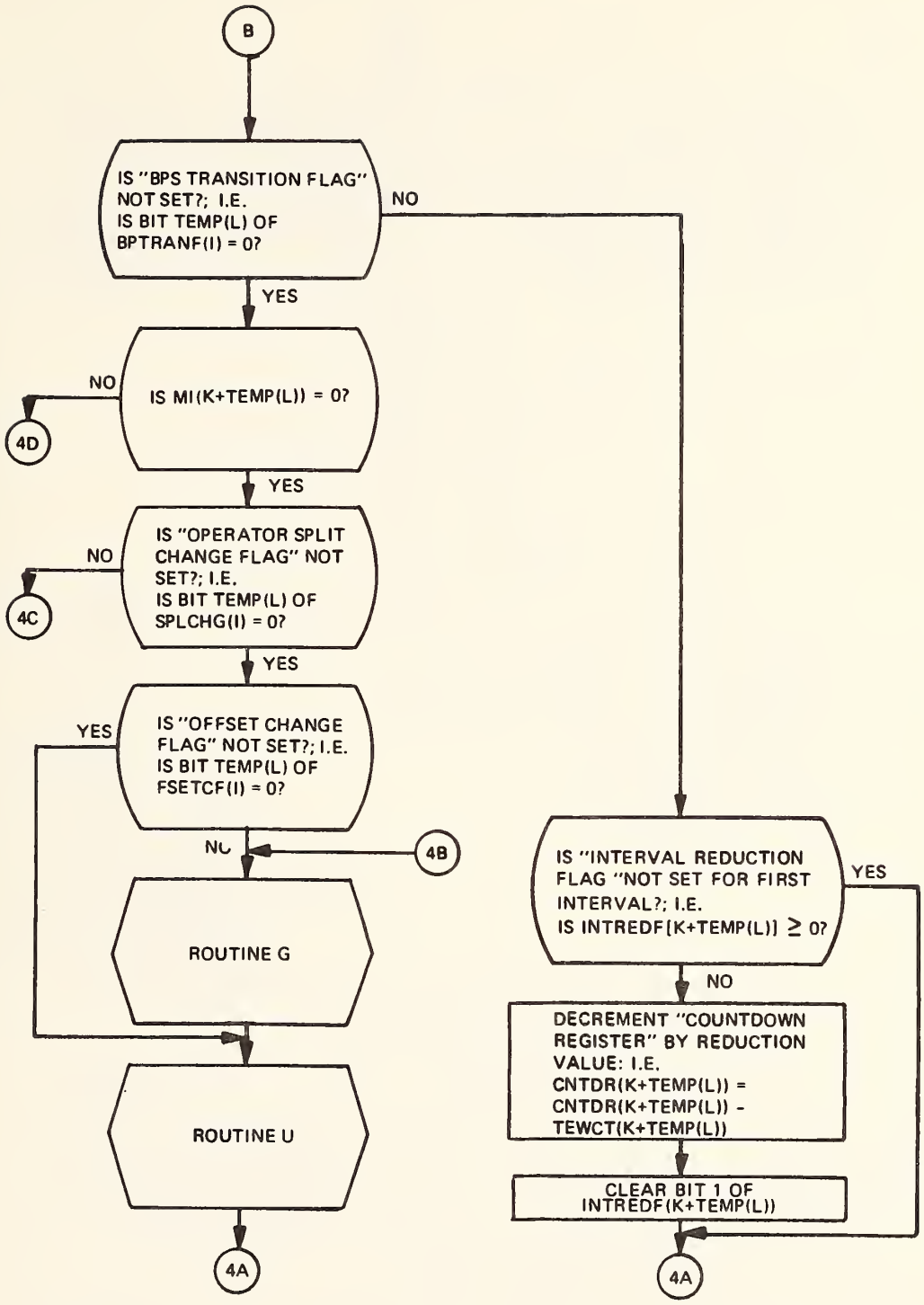


FIGURE 2.21.5.2. ROUTINE T FLOW CHART

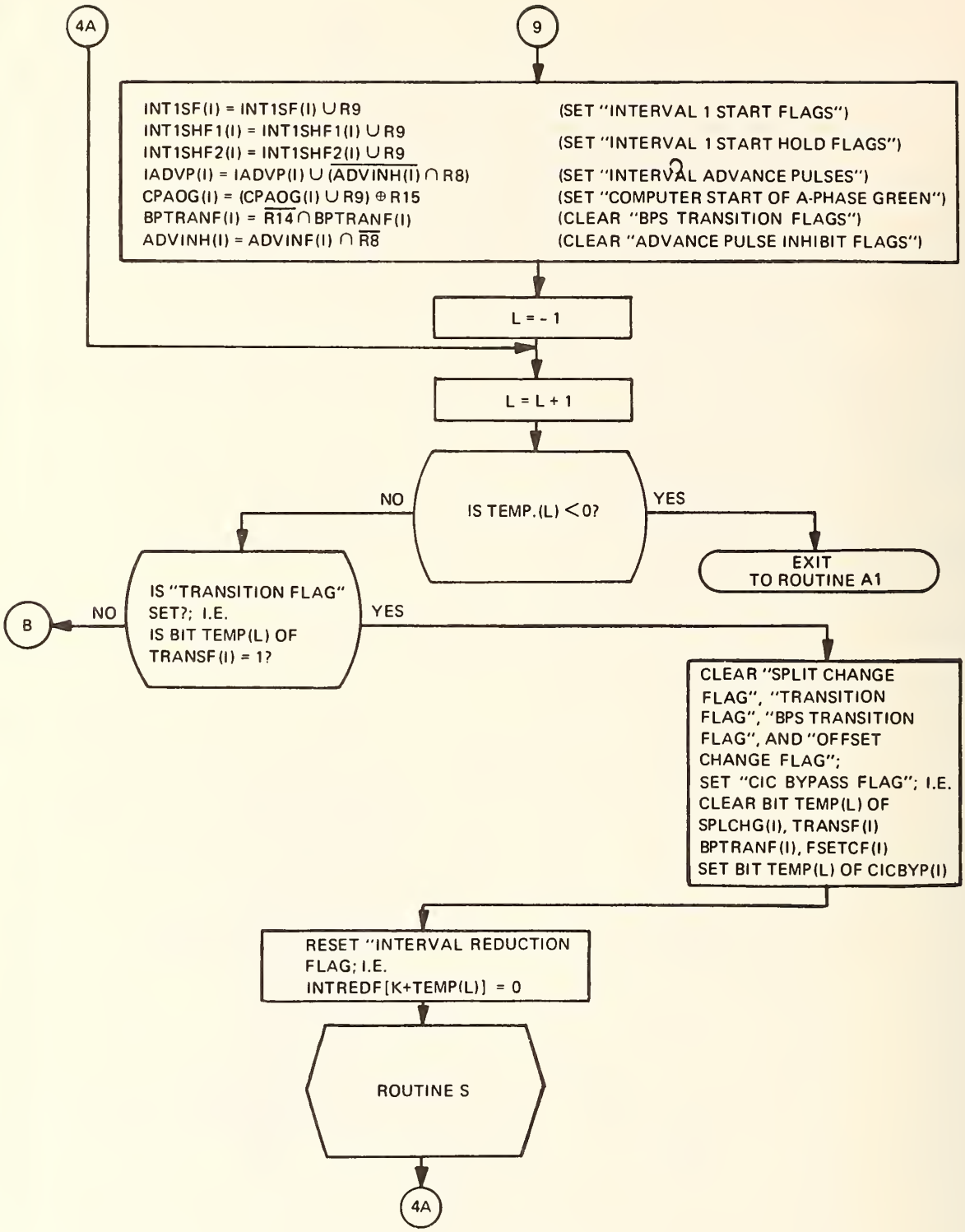


FIGURE 2.21.5.2. ROUTINE T FLOW CHART

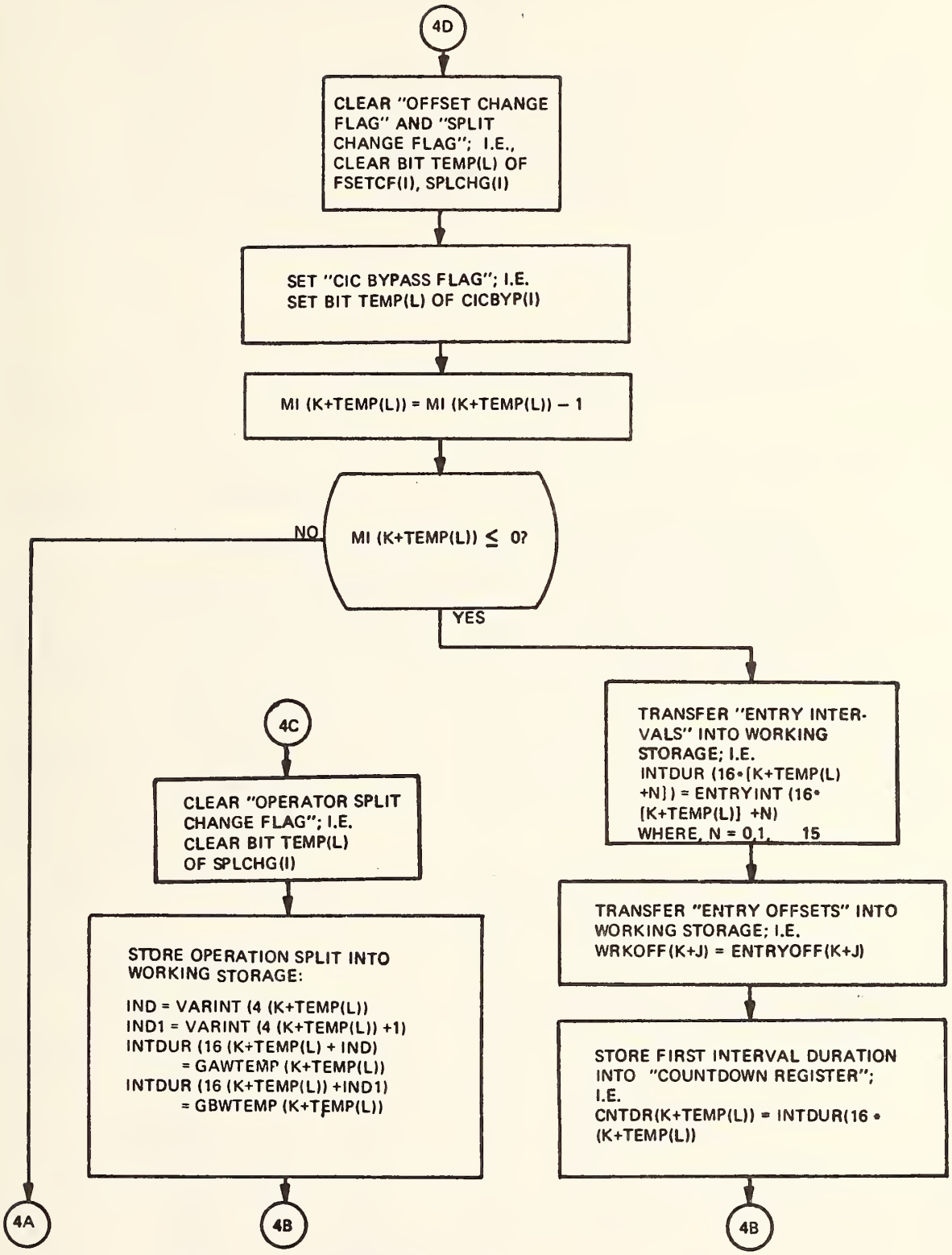


FIGURE 2.21.5.3. ROUTINE T SPECIFICATiON

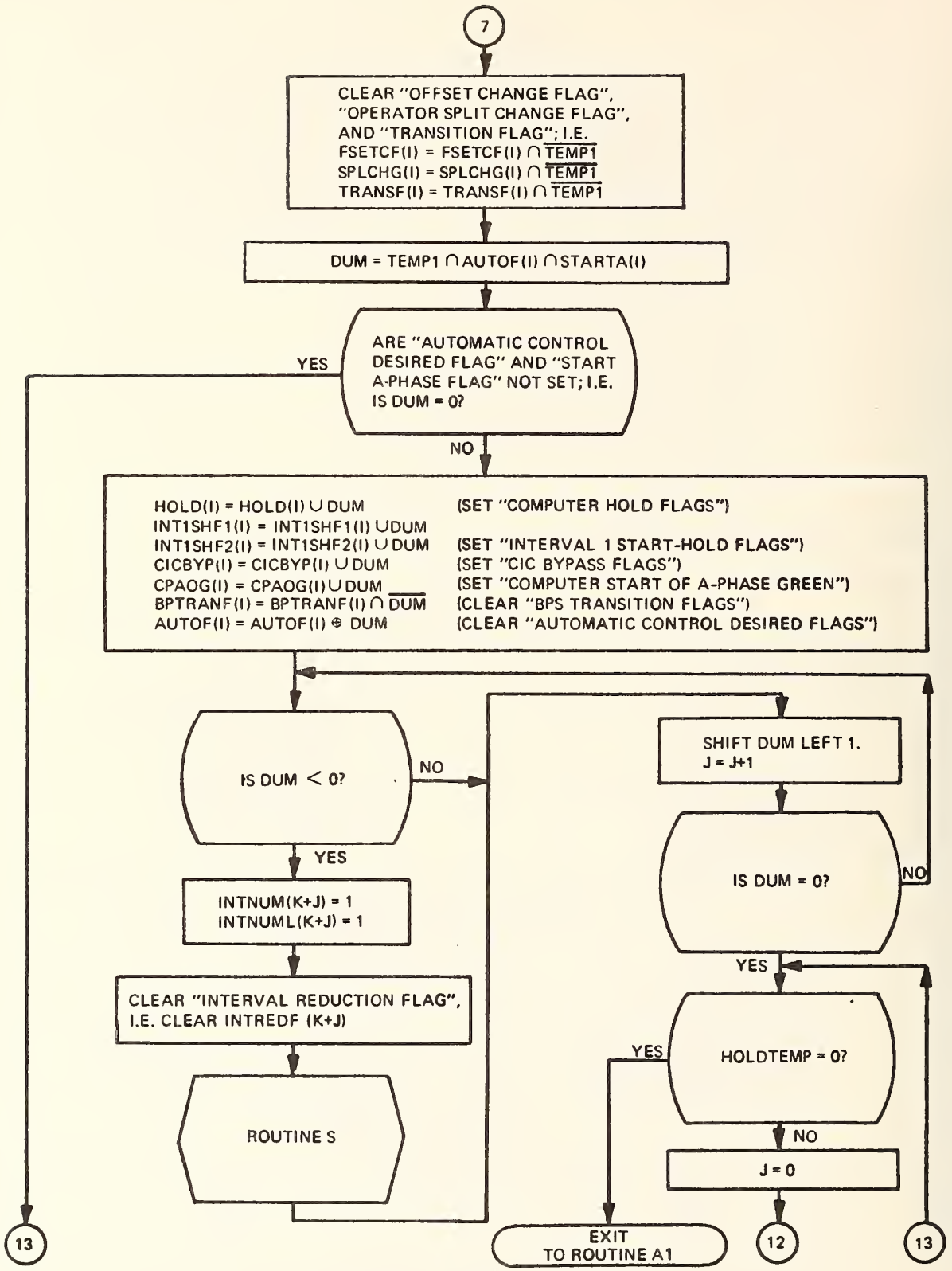


FIGURE 2.21.5.4. ROUTINE T SPECIFICATION

2.22 Routine U (Offset Correction) Specification

2.22.1 Purpose

The purpose of this routine is to compute the difference between the present controller offset and the desired controller offset and correct for this difference. This correction is limited between +6 seconds and -3 seconds per cycle, so the necessary compensation may extend over several cycles. MOE computations reflecting these corrections are also performed.

2.22.2 Method

This routine is entered at the start of the programmed A-phase green, provided that a transition has not been initiated or is not in progress at this controller. The routine will perform the following series of computations.

1. The difference, EPSOF, between the present controller offset, TCK1, and the desired offset value, WRKOFF, will be computed.

2. EPSOF will be converted so that the shortest time between the two offset values will be chosen. The converted correction will then be imposed over a series of cycles, with the constraint that a given cycle's correction will always be greater than -3 seconds and less than +6 seconds in order to minimize the transitional effect.

3. EPSOF will be added to the first interval duration. Also, the "MOE 1 Clock" and the "MOE 2 Clock" will be adjusted by the amount of the change in the first interval, EPSOF, and the "Offset Change Flag" will be set for subsequent use in Routines T and G.

2.22.3 Repetition Rate

This routine is entered, if required, from Routine T, Interval Advance Routine, which is executed once per 1/2 second for each local controller in the system.

2.22.4 Cross Reference

Routine U is called, as a subroutine, by Routine T, Interval Advance Routine, at the start of interval one provided that,

1. No BPS extension is being granted on this controller

2. No transition is requested or is in progress.

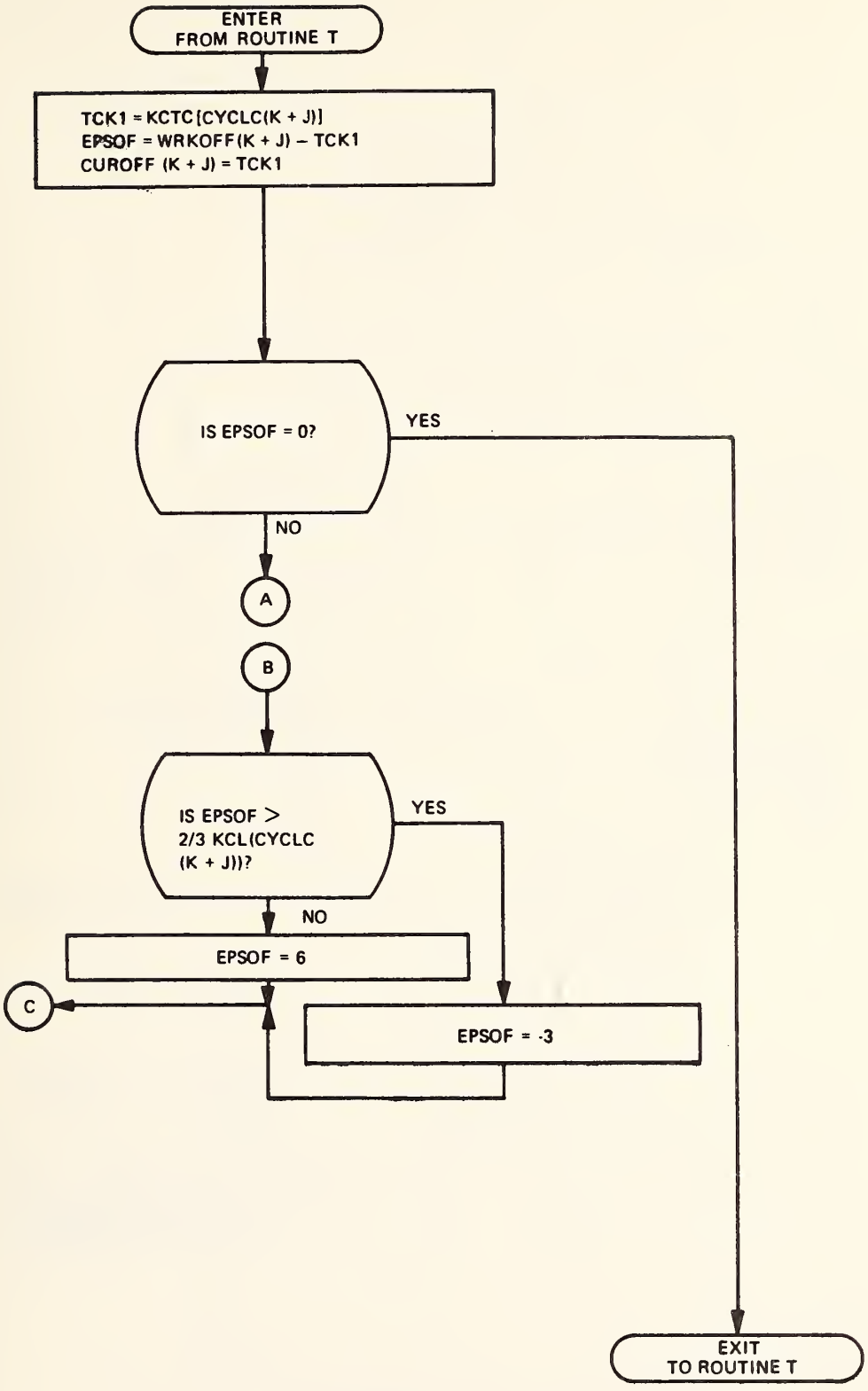


FIGURE 2.22.5.1 ROUTINE U FLOW CHART

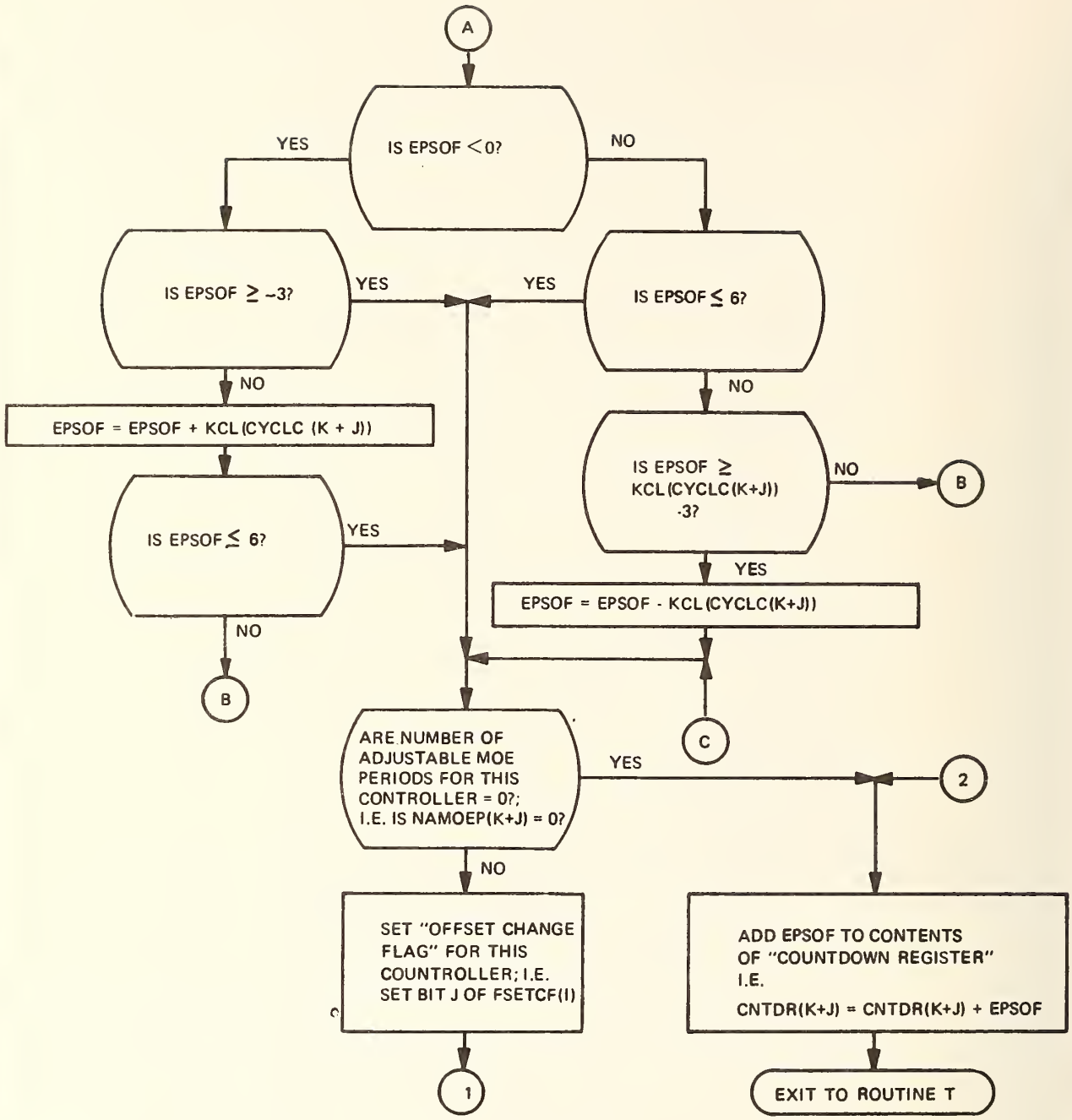


FIGURE 2.22.5.1. ROUTINE U FLOW CHART

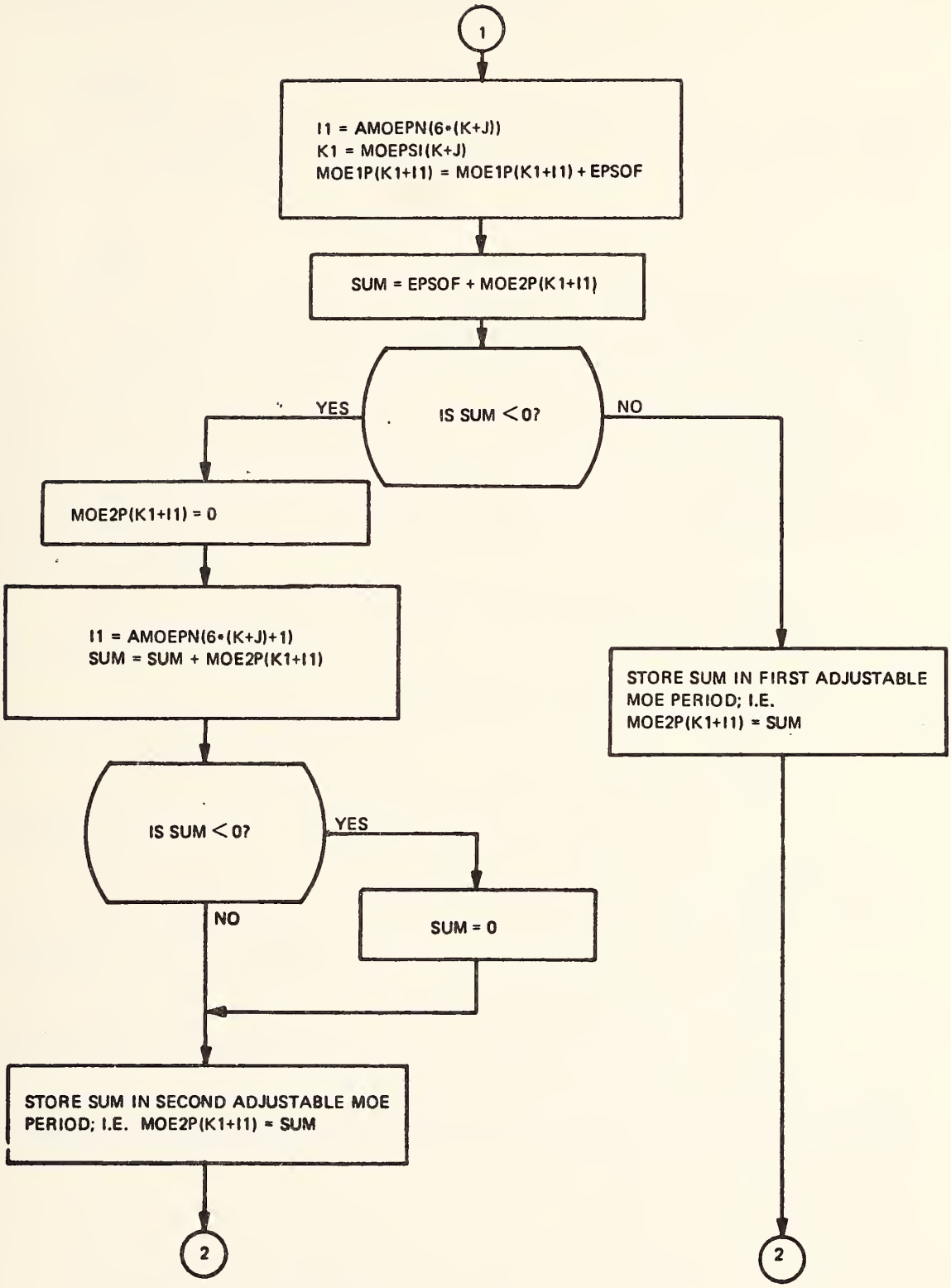


FIGURE 2.22.5.2. ROUTINE U SPECIFICATION

2.23 Routine V (Critical Intersection) Specification

2.23.1 Purpose

The purpose of this routine is to apportion the split of the critical phases of an operational critical intersection according to the measured vehicular demand on these phases.

2.23.3 Method

Routine V is one of the routines comprising the controller Do-Loop (defined in Routine A1, Do-Loop Routine) and is scheduled by the Do-Loop Routine at the beginning of the first programmed controller interval. Routine A1 passes a 32 bit configuration (in general register 8), indicating which of the 32 controllers are starting their first programmed interval. Routine V scans for a "1" in any bit position of register 8 indicating the start of interval 1 for the corresponding controller. The Routine will perform the critical intersection computations for this controller provided all the following conditions are satisfied.

- The intersection has been designated by the operator as a critical intersection ("CICSF" FLAG).
- The intersection has the required detector complement for CIC operation ("NQL" number of critical links array).
- The intersection may operate as a CIC at the present time of day ("CICTODF" FLAG).
- The detectors on all critical links feeding the intersection are functioning properly, and the volumes and queues on all these links are being computed by Routine D, computation of stops ("QVOK" array).
- The intersection is not starting either a transitional cycle or the first cycle following a transition ("CICBYP" FLAG and "BPTRANF" FLAG).
- The demand on at least one of the critical links has exceeded a threshold constant stored in arrays GUABC and GLABC as described in the following paragraphs.

- A normal operator offset change has not been introduced at the start of this cycle ("FSETCF" FLAG.)

If the above conditions are satisfied Routine V performs the following computations:

- The green demand time (GD) is computed for each selected critical link feeding the critical intersection by calling the Green Demand Subroutine with the QCIC, QK, VO, and RR as inputs (defined in I/O list.) See Appendix 4.7.9 for computation of Green Demand Time.

- If a controller phase has two critical links assigned to it (indicated by contents of the "LDSET" array) the green demand time will be set equal to the larger of the two link demand times, as described in Appendix 4.7.9.

- The green demand time on all of the critical links are checked to determine if at least one exceeds an upper threshold ("GUABC" array) before initiation of CIC control begins. To maintain CIC Control, once initiated, at least one of the critical links must exceed a lower threshold ("GLABC" array). These two thresholds provide a hysteresis correction to prevent switching back and forth between area and critical intersection control.

- The determination of the green time for each critical phase is carried out according to the algorithm described in Appendix 4.7.9.

- The adjustable intervals associated with each critical phases will be corrected by the amount of change in that phase and Routine G, Controller Link Cross Reference and Timing will be entered to adjust the duration of the associated MOE period.

2.23.3 Repetition Rate

This routine is entered whenever the start of interval 1 is sensed by Routine A1.

2.23.4 Cross Reference

This routine is part of the Level 2 controller Do-Loop Routines. It follows Routine T and exits to Routine A1.

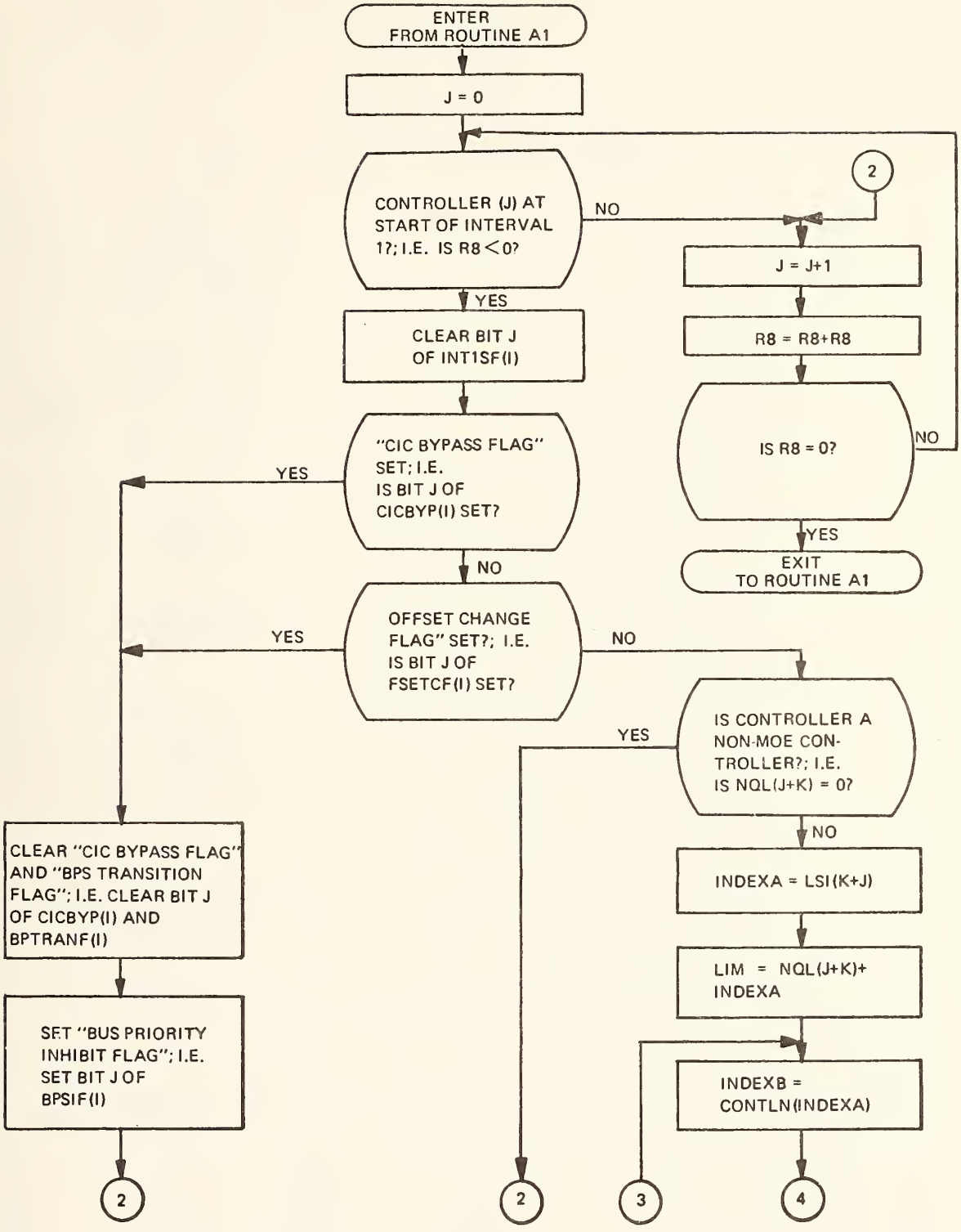


FIGURE 2.23.5.1. ROUTINE V SPECIFICATION

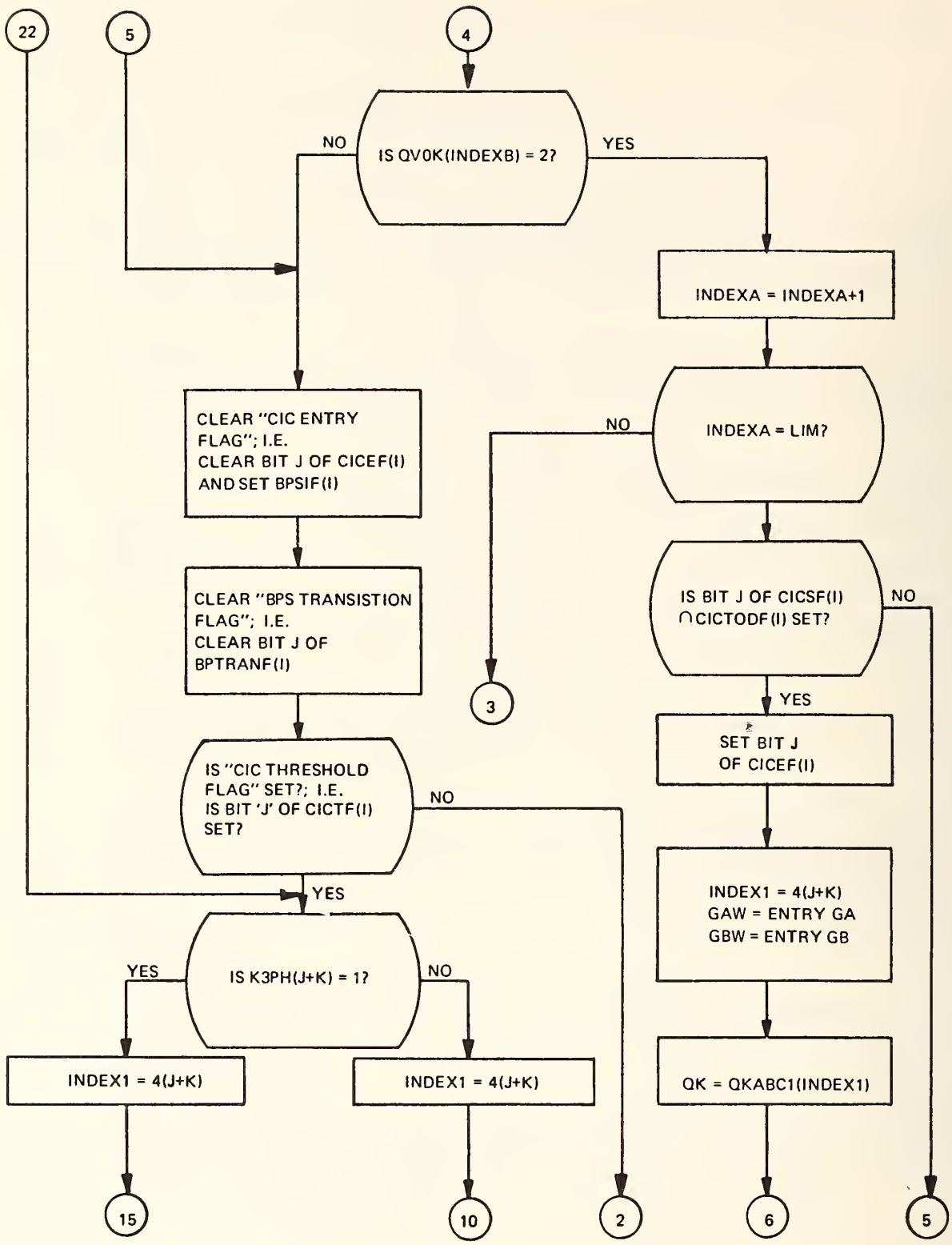


FIGURE 2.23.5.2. ROUTINE V SPECIFICATION

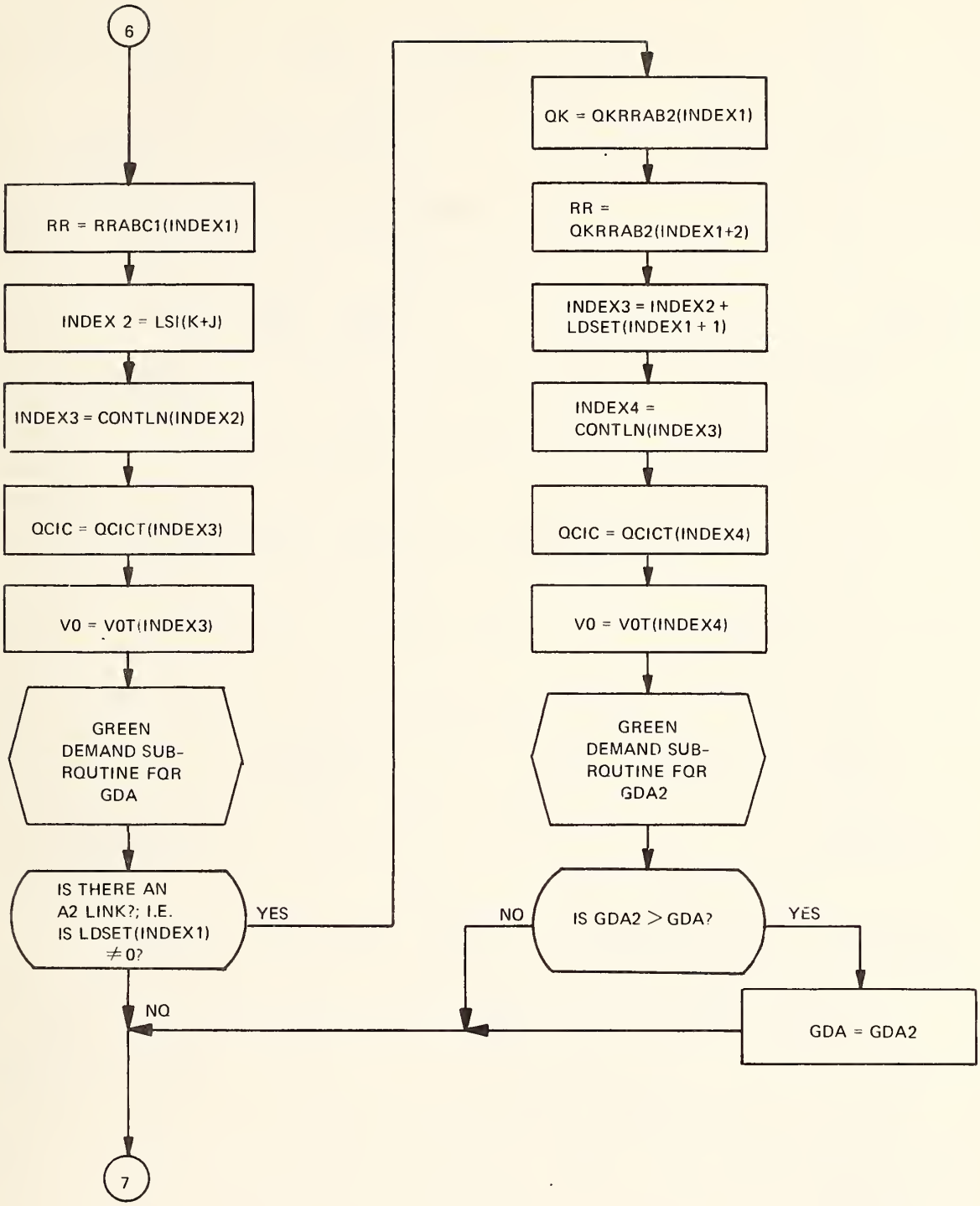


FIGURE 2.23.5.3. ROUTINE V FLOW CHART

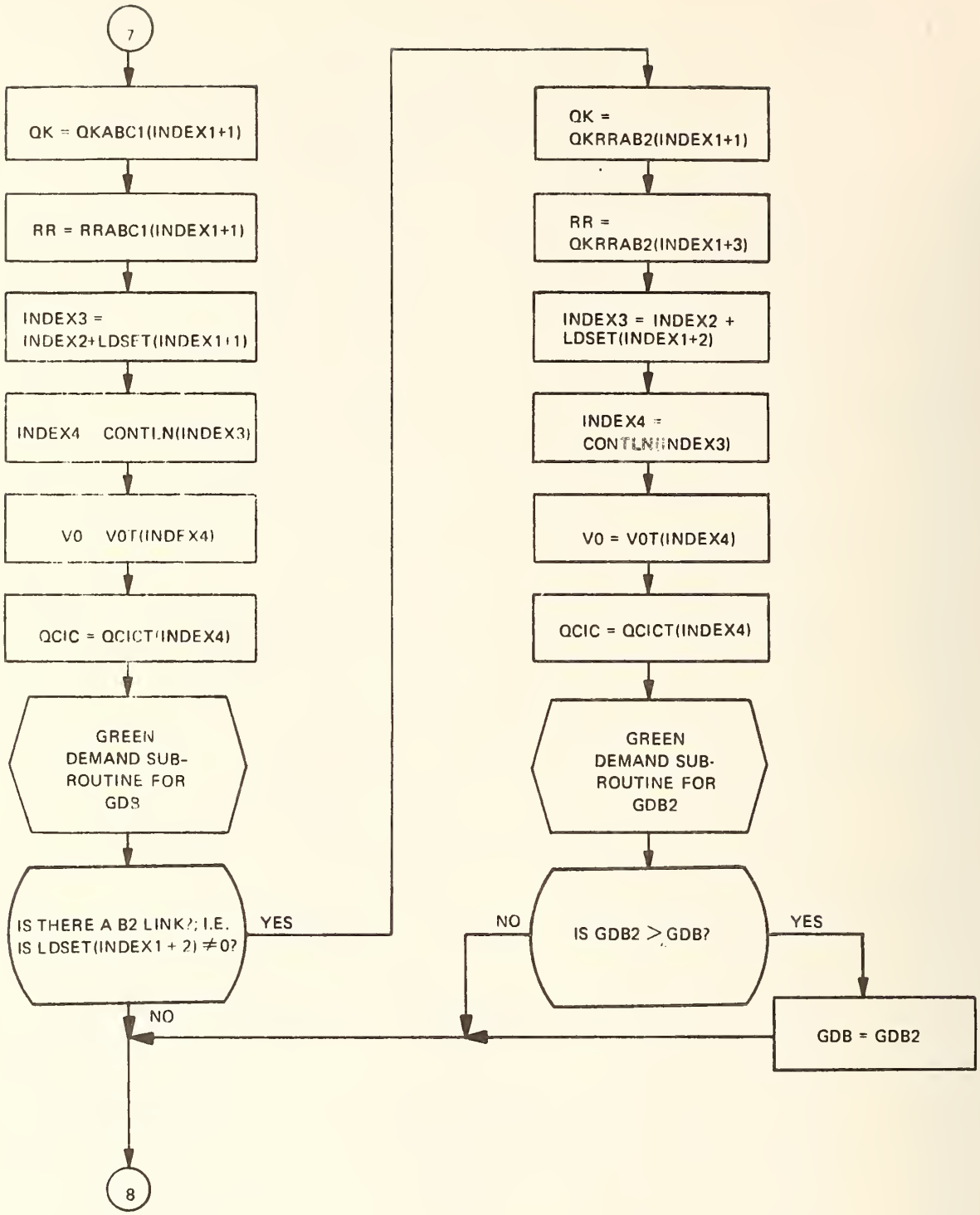


FIGURE 2.23.5.4. ROUTINE V FLOW CHART

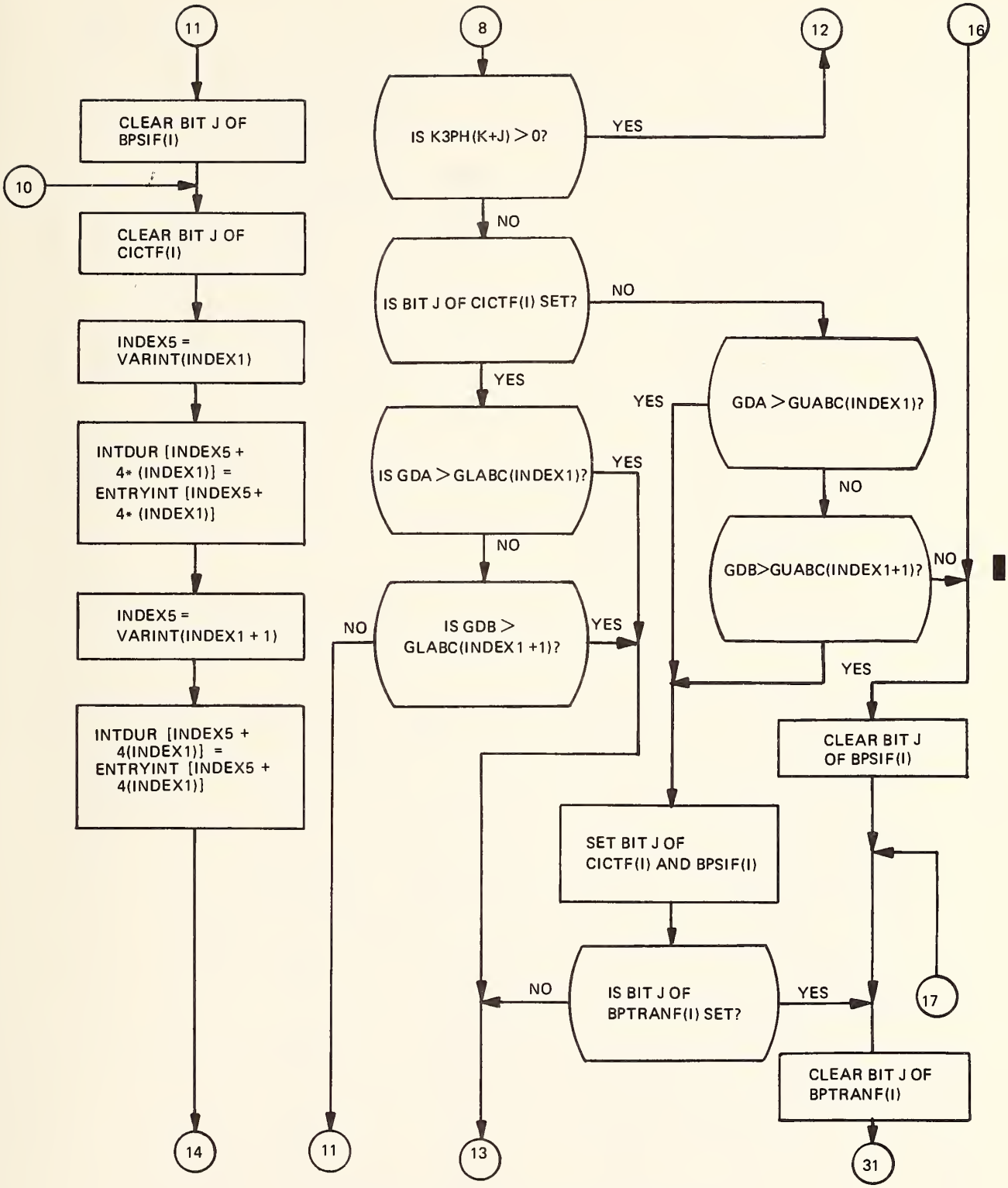


FIGURE 2.23.5.5. ROUTINE V FLOW CHART

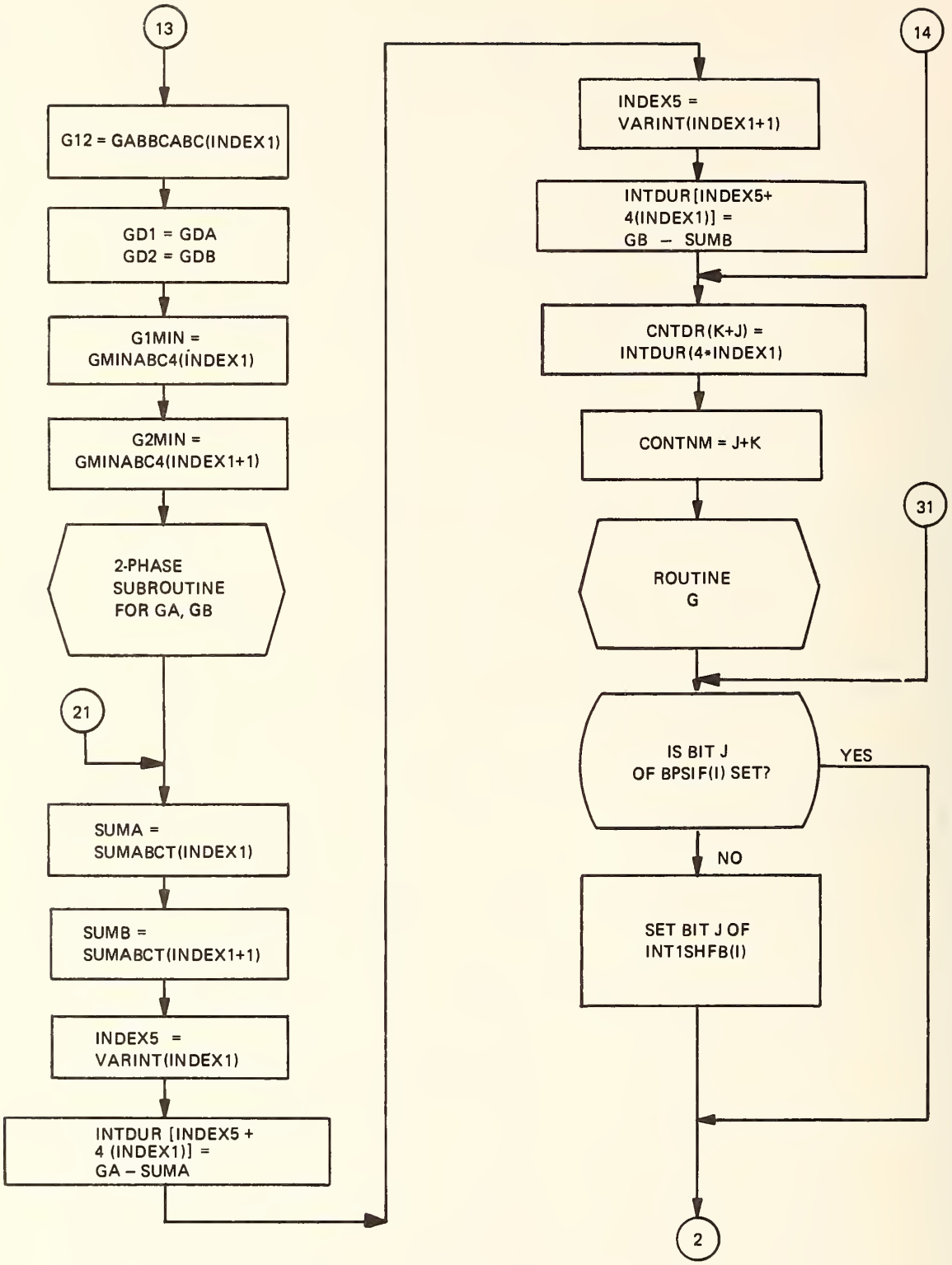


FIGURE 2.23.5.6. ROUTINE V FLOW CHART

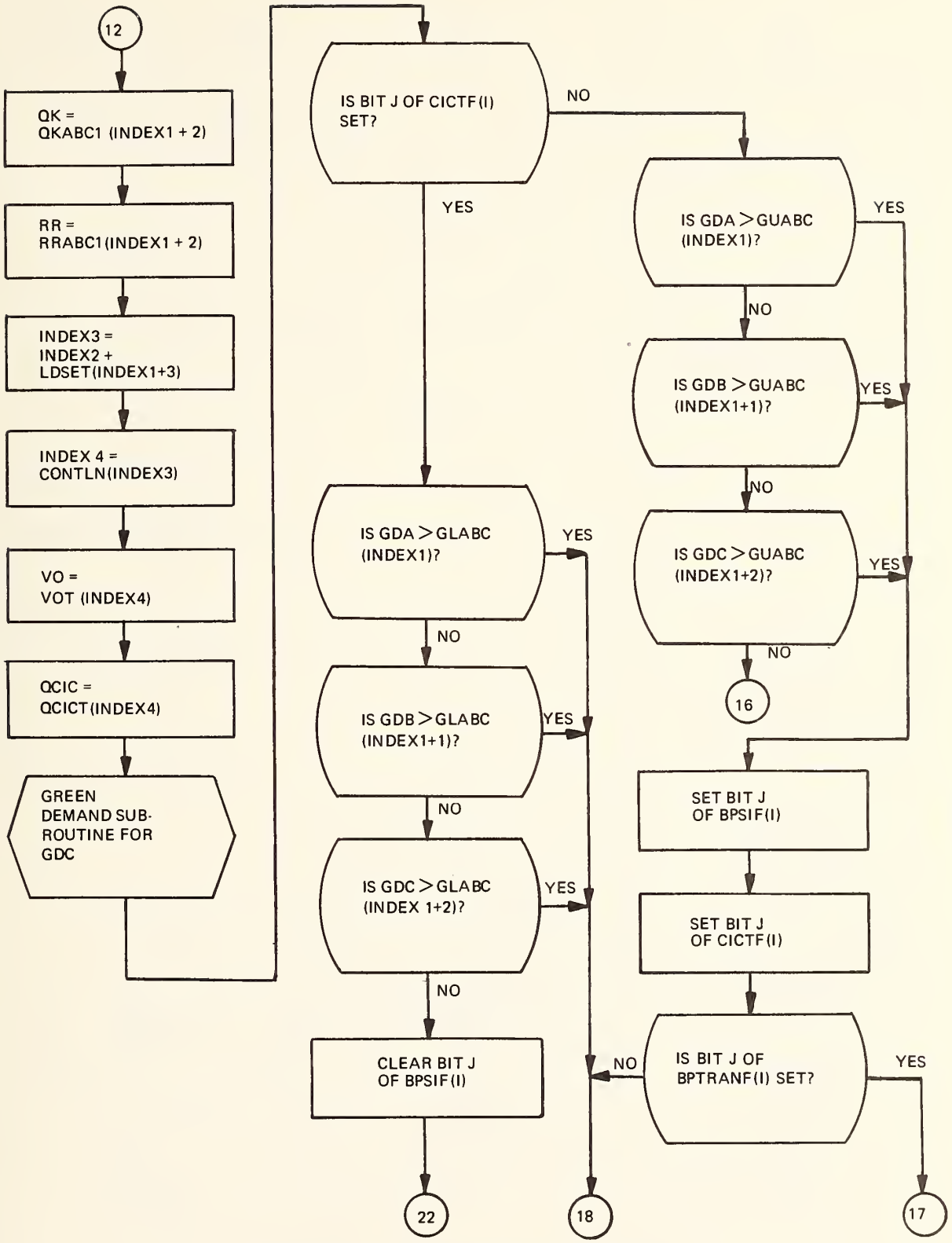


FIGURE 2.23.5.7. ROUTINE V FLOW CHART

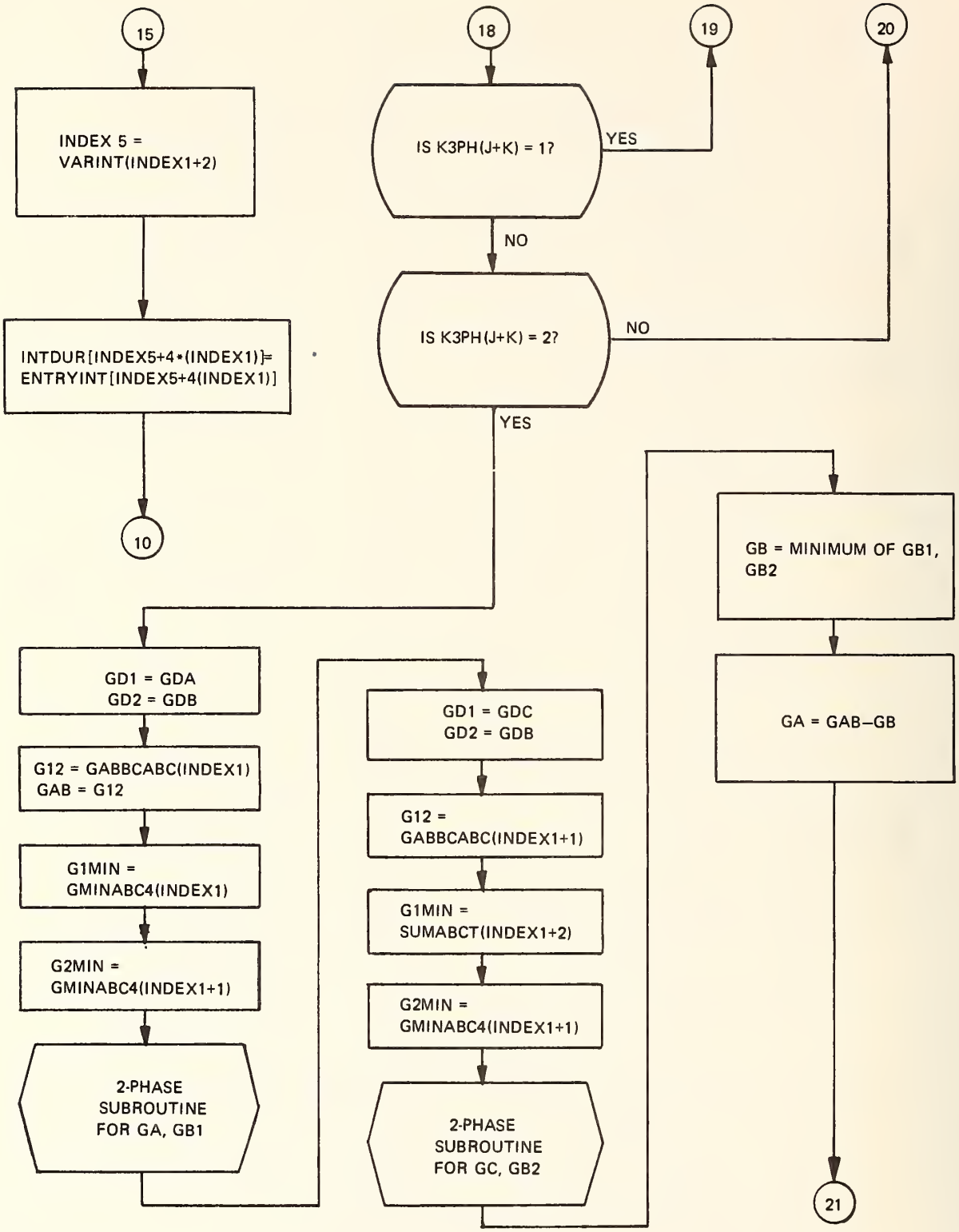


FIGURE 2.23.5.8. ROUTINE V FLOW CHART

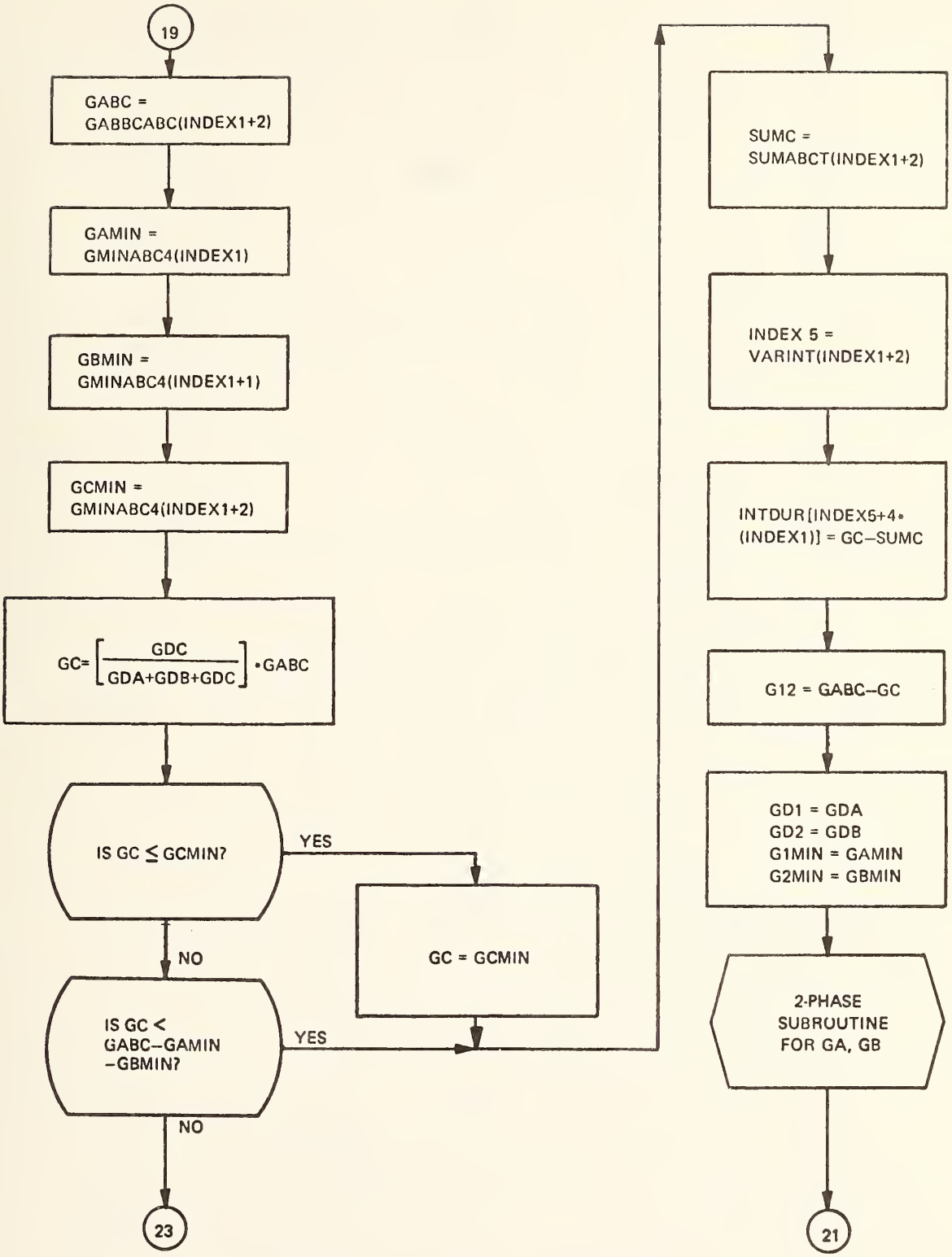


FIGURE 2.23.5.9. ROUTINE V SPECIFICATION

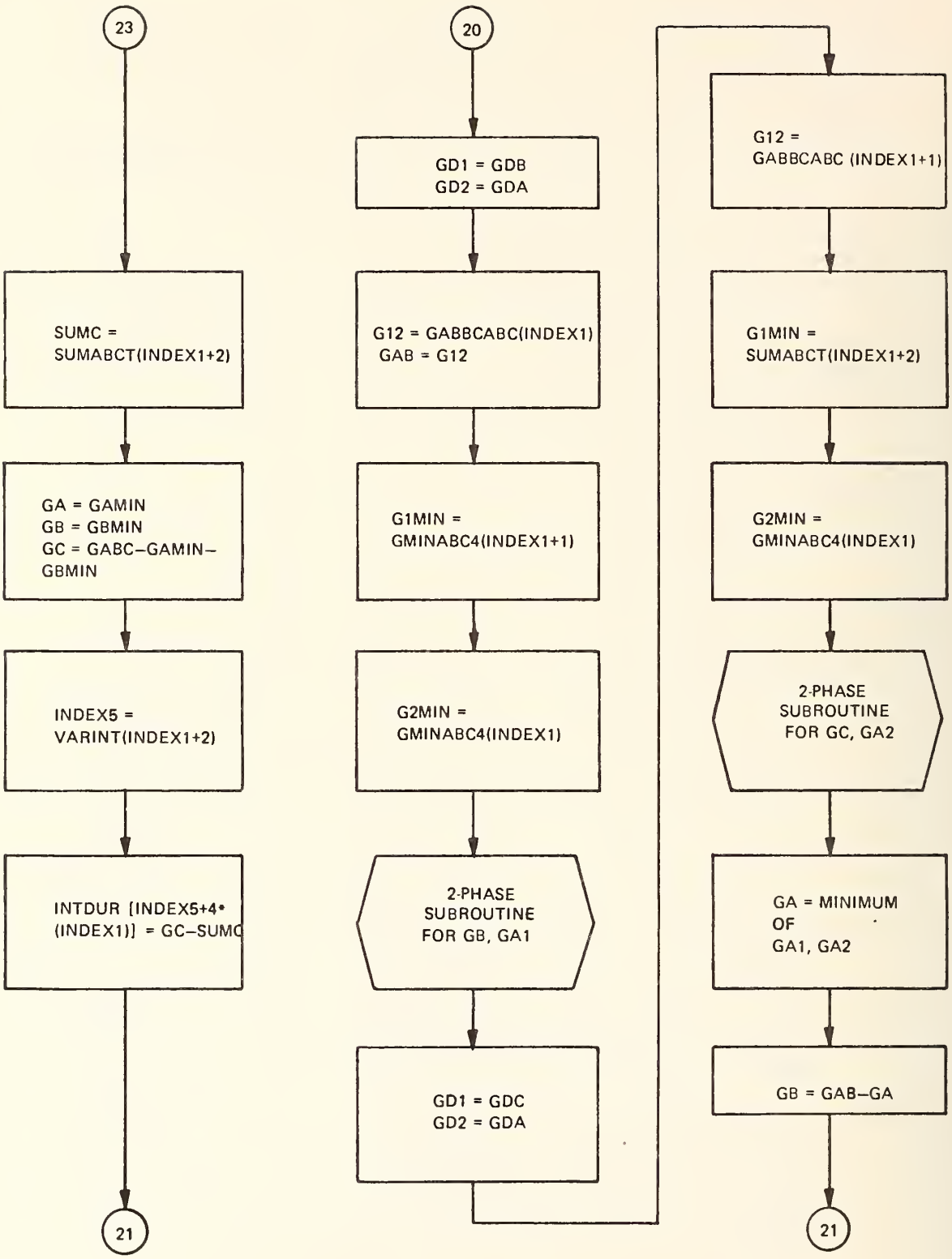


FIGURE 2.23.5.10. ROUTINE V SPECIFICATION

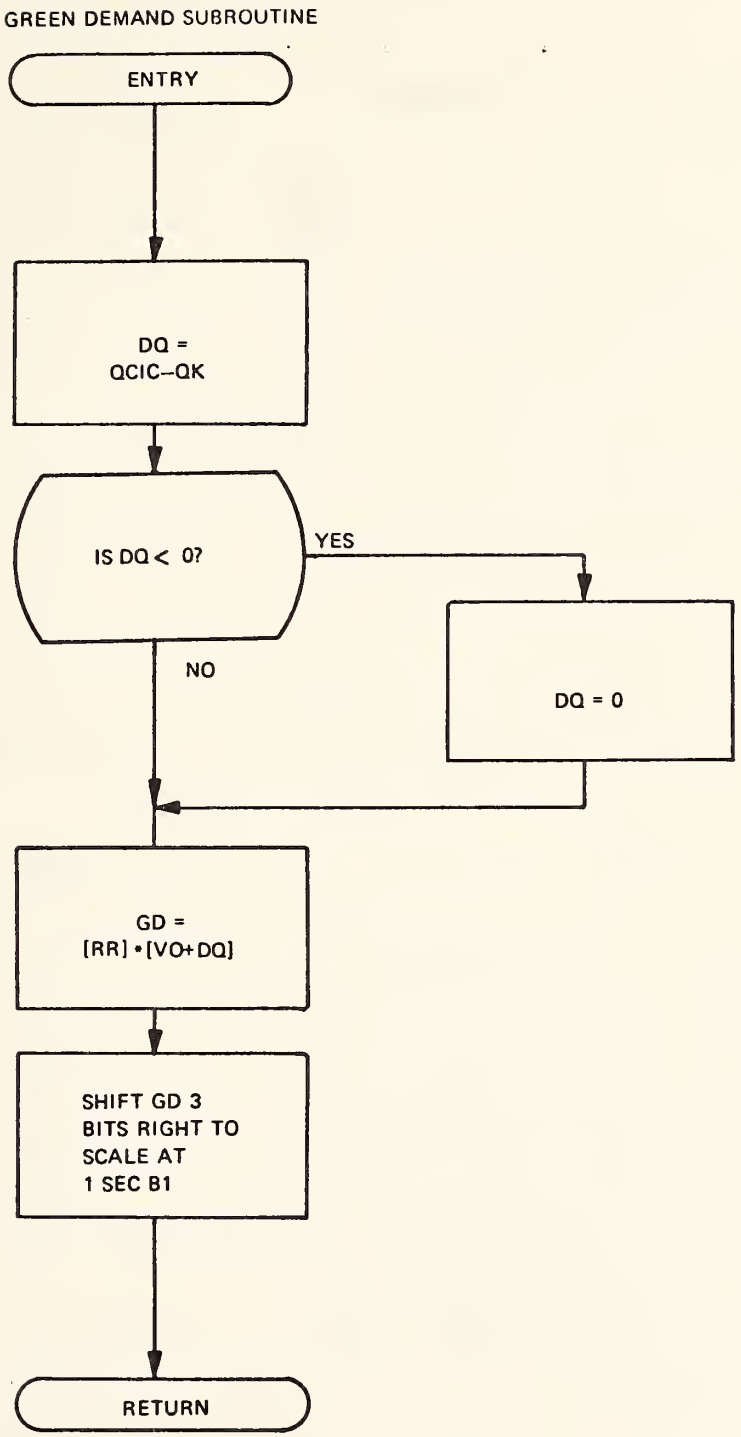


FIGURE 2.23.5.11. ROUTINE V SPECIFICATION

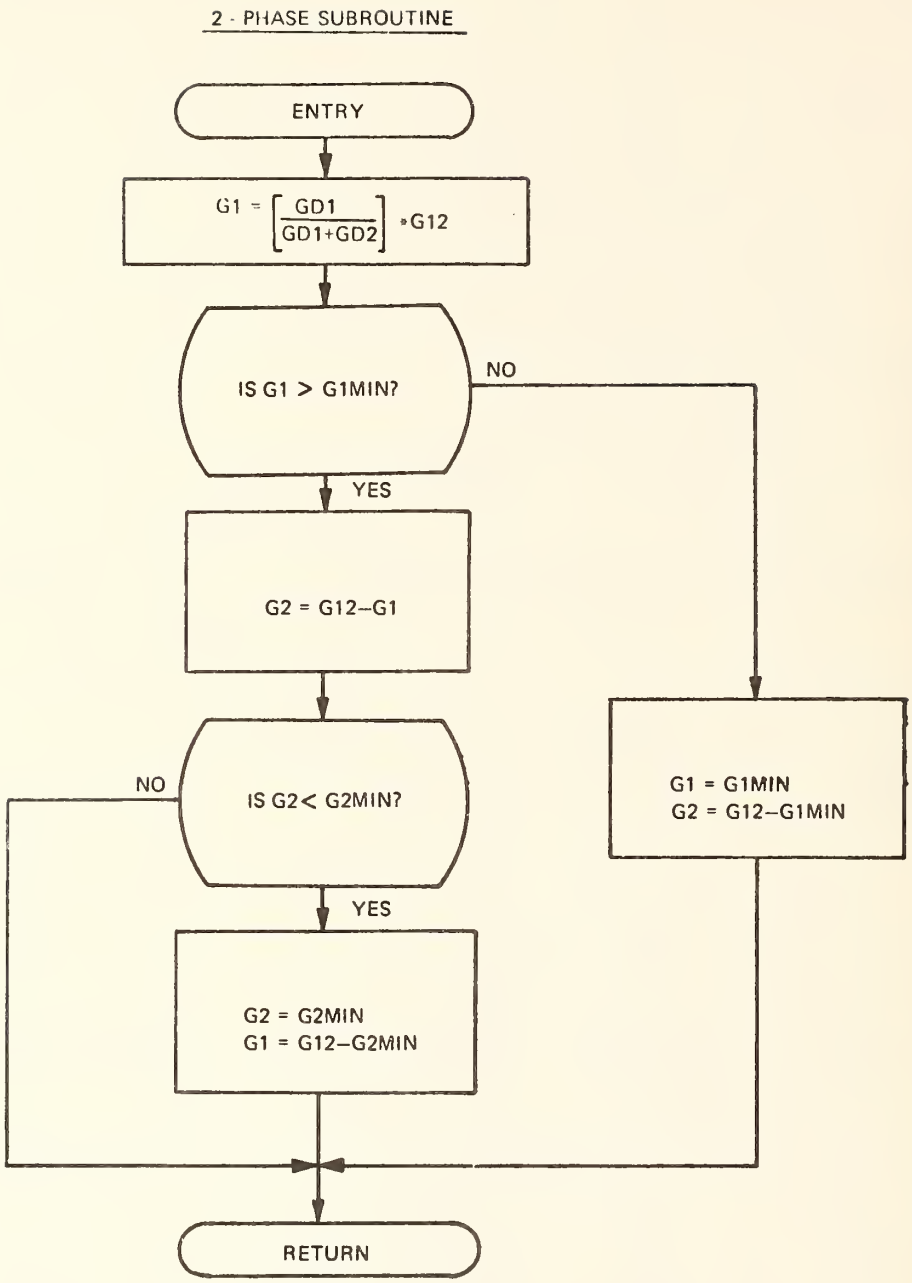


FIGURE 2.23.5.12. ROUTINE V SPECIFICATION

2.24 Routine W (Controller Parameter Selection) Specification

2.24.1 Purpose

The purpose of this routine is to provide logic for selecting one of the following area control techniques for each section:

- Time of day selection of pattern
- Manual operator selection of pattern
- Automatic selection of pattern by traffic responsive algorithm
- Inhibits bus priorities when working controllers are in transition
- Inhibits CIC operation during certain periods in the day at those intersections where prevailing conditions require such action.

The routine reformats controller parameters from disk into arrays for use in other routines. It reformats the link parameters used by Routine V and the bus priority parameters entered from the RAD for use by the BPS routines, and it sets up flags and arrays required by the controller and data processing routines.

2.24.2 Method

In the TR algorithm, the computer may choose a pattern to be used from among a maximum of four different patterns, one of which is always the TOD pattern. The volume plus weighted occupancy (VPLUSKO) values are calculated by the equation:

$$VPLUSKO = V_i + 20\ (O_i)$$

where V_i = the volume for link i in vph

O_i = the occupancy for link i in percent

As shown in Fig. 2.24.2.1 the first word contains the four eligible pattern numbers from which the computer may select a TR pattern for Selection 1. The next three words contain the numbers of the patterns eligible for manual pattern selection (MPS) for Section 1. The left most byte of the first of these three words contains the TOD pattern number. The next 12 words repeat this information for each of the three remaining sections. The next word (four bytes) contains the four VPLUSKO's for link one corresponding to the four eligible TR patterns. The next words are the values for Link 2 and so on to Link 256.

The Routine W first reads in four sets of histories (HSBUF) from the RAD. These history entries contain volume plus weighted occupancy for each link; applicable to the current time of day and day of week. It then determines, from the operator set flags, which mode of control is desired and if this constitutes a change from the current mode. For time-of-day and manual selection, the appropriate pattern, if different from the current one, is read from the RAD. For automatic selection, current link data is compared with each of the applicable histories to obtain the loss function TEST(NN):

$$TEST\ (NN) = \sum_{I=1}^{\text{No. of Sections}} \left| VPLUSKO(I) - \left[V(I) + K * O\ (I) \right] \right|$$

where VPLUSKO(I) is the volume plus weighted occupancy history for link I

V(I) is the current smoothed volume for link I

O(I) is the current smoothed occupancy for link I

The best pattern is the one corresponding to the history for which TEST(NN) is a minimum. The pattern matching (goodness-of-fit computation) is performed by summing the absolute value of the differences between each link's stored VPLUSKO value and the current 15 minutes calculated value of VPLUSKO for every link in every eligible TR pattern. The pattern with the lowest sum is then a candidate for selection. If the candidate pattern is the pattern currently in use, the routine continues on with other functions. If not, the absolute difference sum (ADS) of the candidate pattern is compared to the current pattern's ADS for significant difference. The significant difference is determined by comparing the candidate pattern's ADS with the current pattern's ADS which has been increased by the factor KH. If the candidate pattern's ADS is greater than or equal to the current pattern's scaled ADS, then the current pattern remains as the "best" fit and no further action is taken. However, if the candidater pattern's ADS is less than the current pattern's scaled ADS, the new pattern is loaded into the system and the system will then transition into that pattern.

The intent of the scaling factor KH is to provide the capability of removing frequent pattern changes due to the disruptive effects of transitioning by assuring that the candidate pattern is significantly "better" than the current pattern. See Figure 2.24.2.2 for format of pattern.

After a pattern has been read in from disk for any mode of control, the controller parameters are reformatted into entry storage arrays, and intersection constants and link constants are reformatted for use by Routines S and V.

In addition, the bus link clocks, bus action period flags, maximum extensions, MOE 1 and 2 period reduction cross-reference tables, and the controller interval cross-reference table, as a function of link, are set up for the BPS routines.

2.24.3 Repetition Rate

This routine is entered once every 15 minutes or whenever the operator calls for a new Manual or Time-of-Day Pattern(s).

2.24.4 Cross Reference

This routine is scheduled by Routines A, H or M and entered from Routine A. It exits to Routine A.

BYTE 0	BYTE 1	BYTE 2	BYTE 3	
1ST PATTERN NO.	2ND PATTERN NO.	3RD PATTERN NO.	4TH PATTERN NO.	SECTION 1
*FOUR	MANUAL	PATTERN	NUMBERS	
FOUR	MANUAL	PATTERN	NUMBERS	
FOUR	MANUAL	PATTERN	NUMBERS	
● ● ●	● ● ●	● ● ●	● ● ●	
1ST PATTERN NO.	2ND PATTERN NO.	3RD PATTERN NO.	4TH PATTERN NO.	SECTION 4
*FOUR	MANUAL	PATTERN	NUMBERS	
FOUR	MANUAL	PATTERN	NUMBERS	
FOUR	MANUAL	PATTERN	NUMBERS	
VPLUSKO	VPLUSKO	VPLUSKO	VPLUSKO	LINK 1
● ● ●	● ● ●	● ● ●	● ● ●	● ●
VPLUSKO	VPLUSKO	VPLUSKO	VPLUSKO	
● ● ●	● ● ●	● ● ●	● ● ●	●
VPLUSKO	VPLUSKO	VPLUSKO	VPLUSKO	
● ● ●	● ● ●	● ● ●	● ● ●	●
VPLUSKO	VPLUSKO	VPLUSKO	VPLUSKO	LINK 256

NOTE: VPLUSKO = HISTORY VALUE OF VOLUME + WEIGHTED OCCUPANCY
BYTE 0 CONTAINS HISTORY SIGNATURE OF 1ST TRAFFIC RESPONSE PATTERN
BYTE 1 CONTAINS HISTORY SIGNATURE OF 2ND TRAFFIC RESPONSE PATTERN
BYTE 2 CONTAINS HISTORY SIGNATURE OF 3RD TRAFFIC RESPONSE PATTERN
BYTE 3 CONTAINS HISTORY SIGNATURE OF 4TH TRAFFIC RESPONSE PATTERN

*TIME OF DAY PATTERN NUMBER STORED IN THIS POSITION

FIGURE 2.24.2.1. HSBUF FORMAT

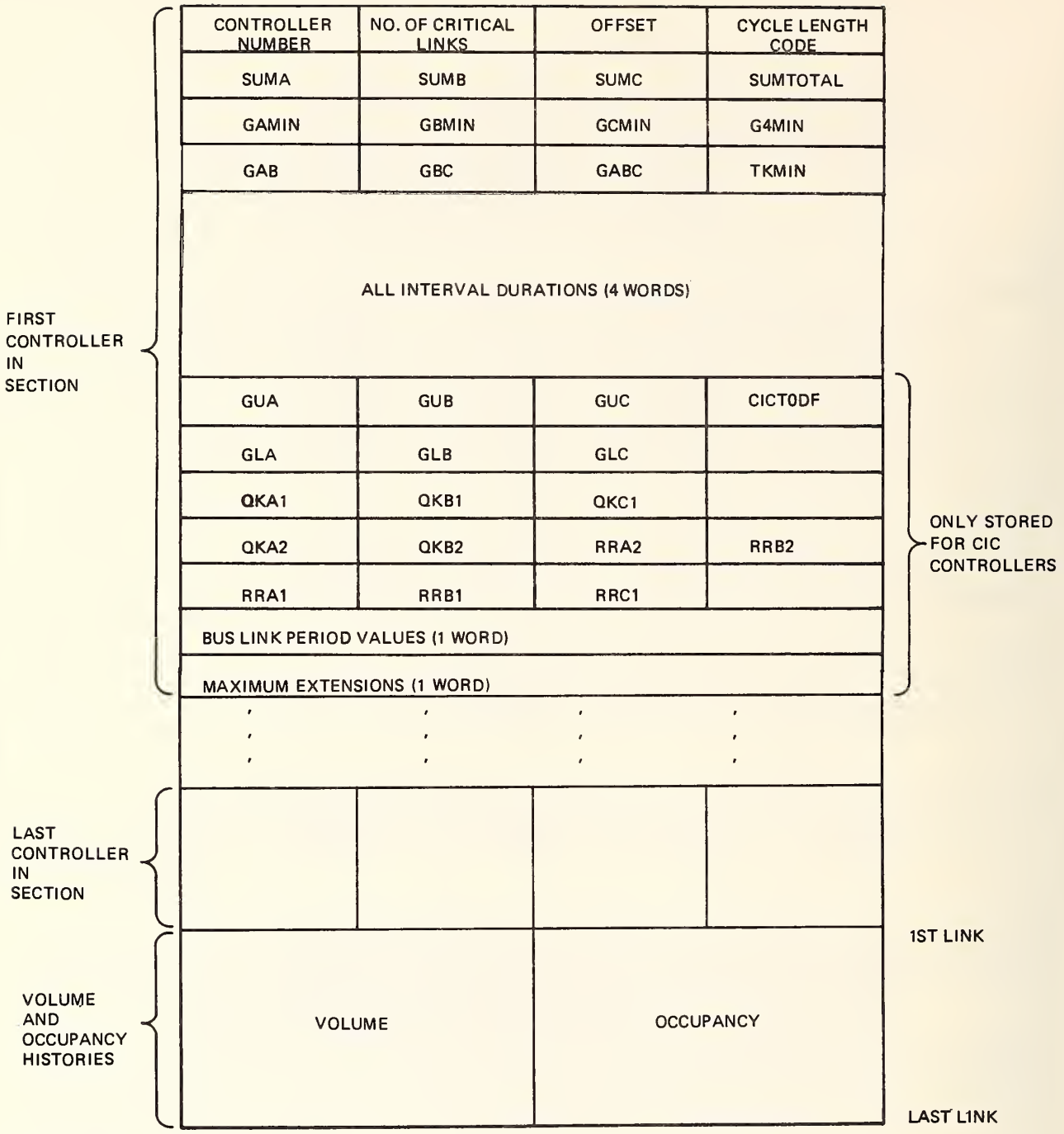


FIGURE 2.24.2.2. PTN FORMAT

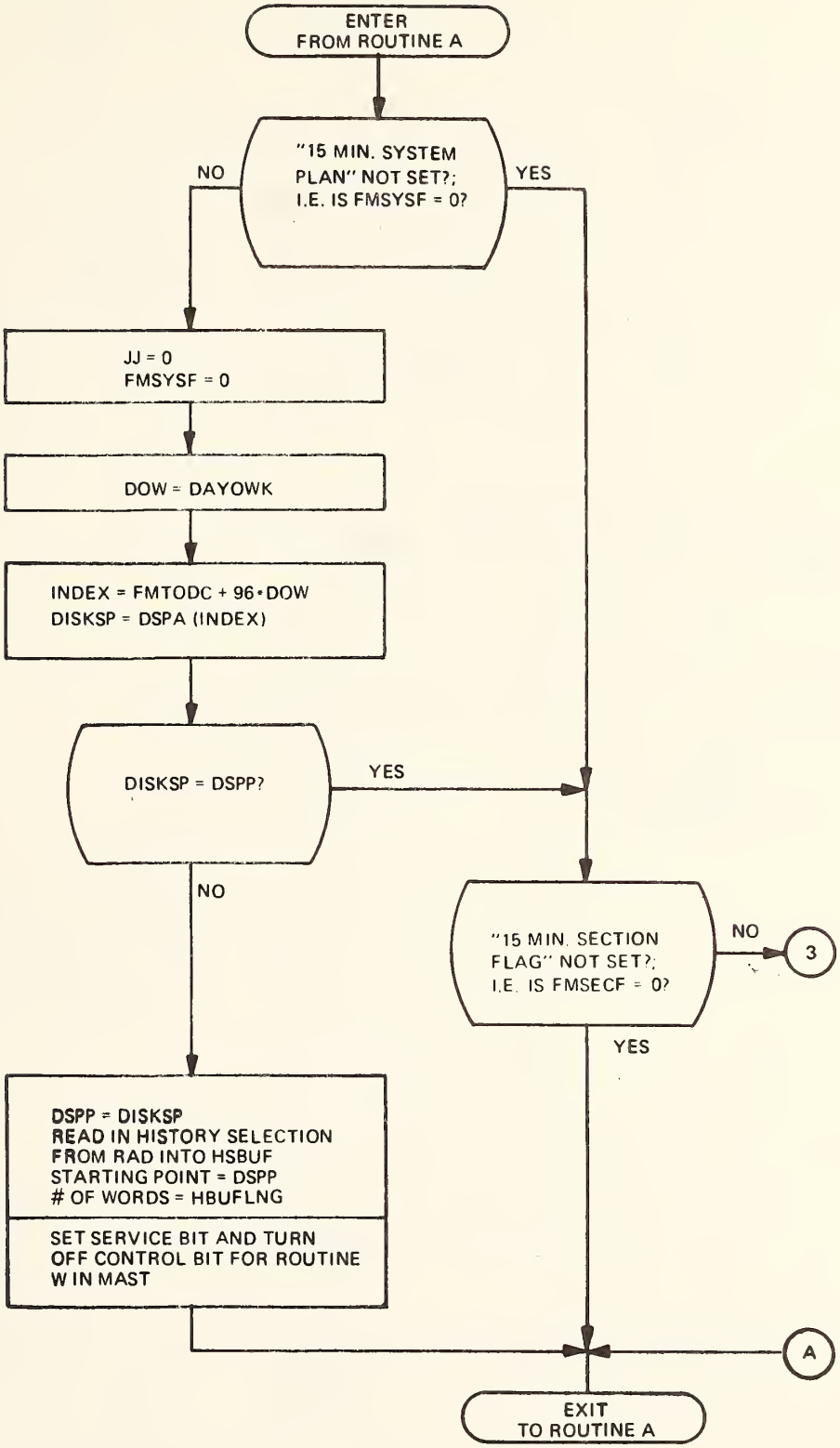


FIGURE 2.24.5.1. ROUTINE W FLOW CHART

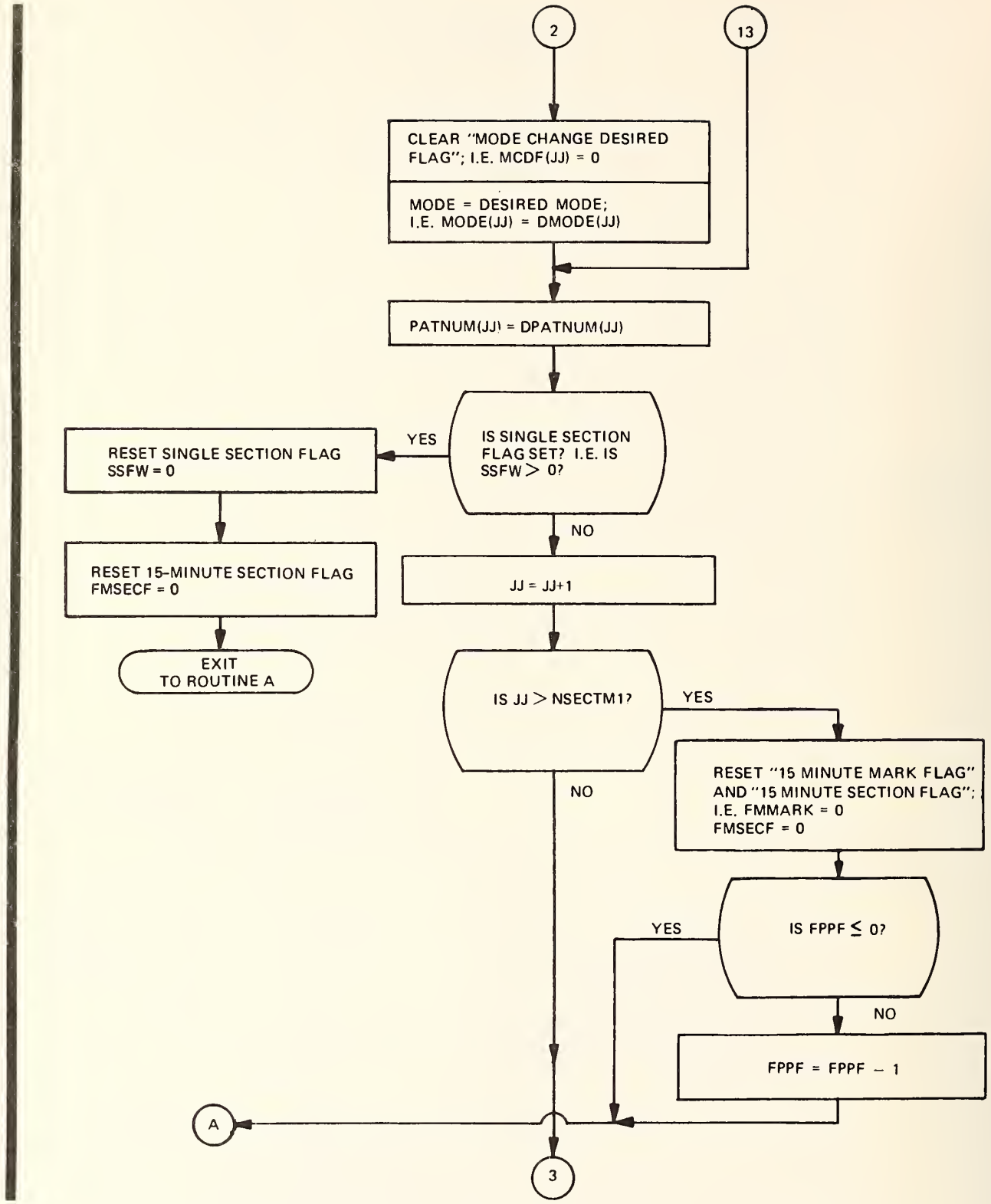


FIGURE 2.24.5.1 ROUTINE W FLOW CHART

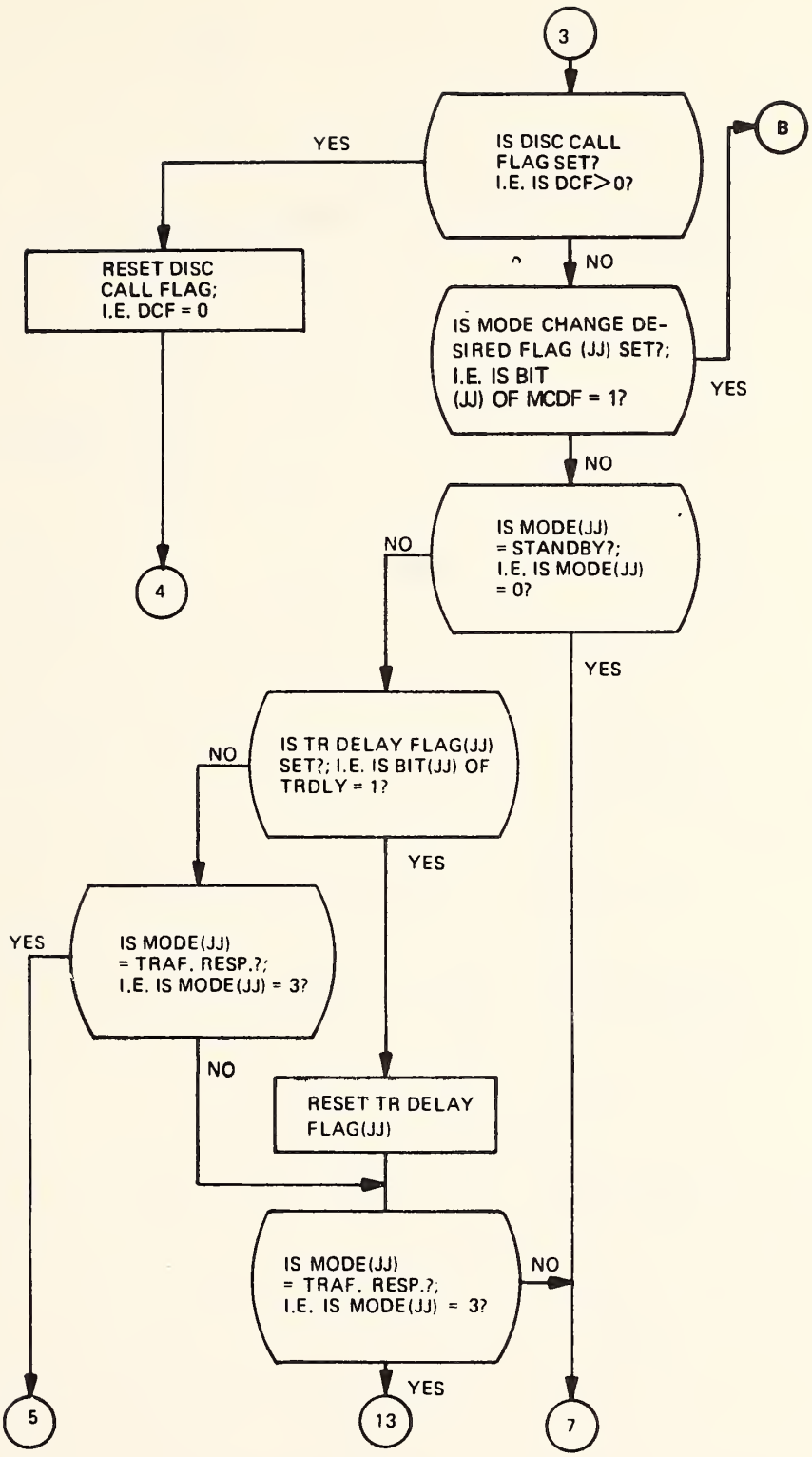


FIGURE 2.24.5.2 ROUTINE W FLOW CHART

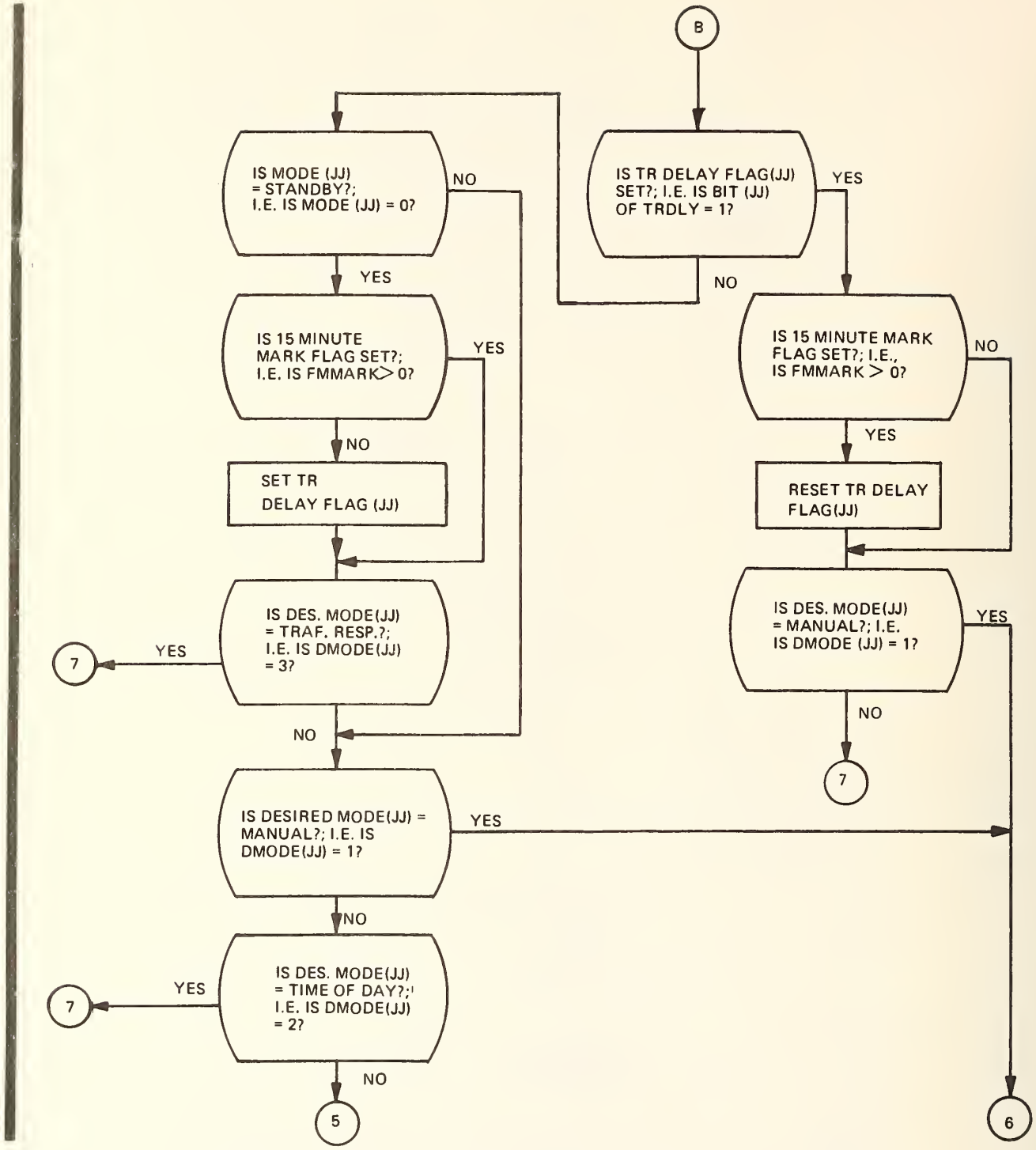


FIGURE 2.24.5.2 ROUTINE W FLOW CHART

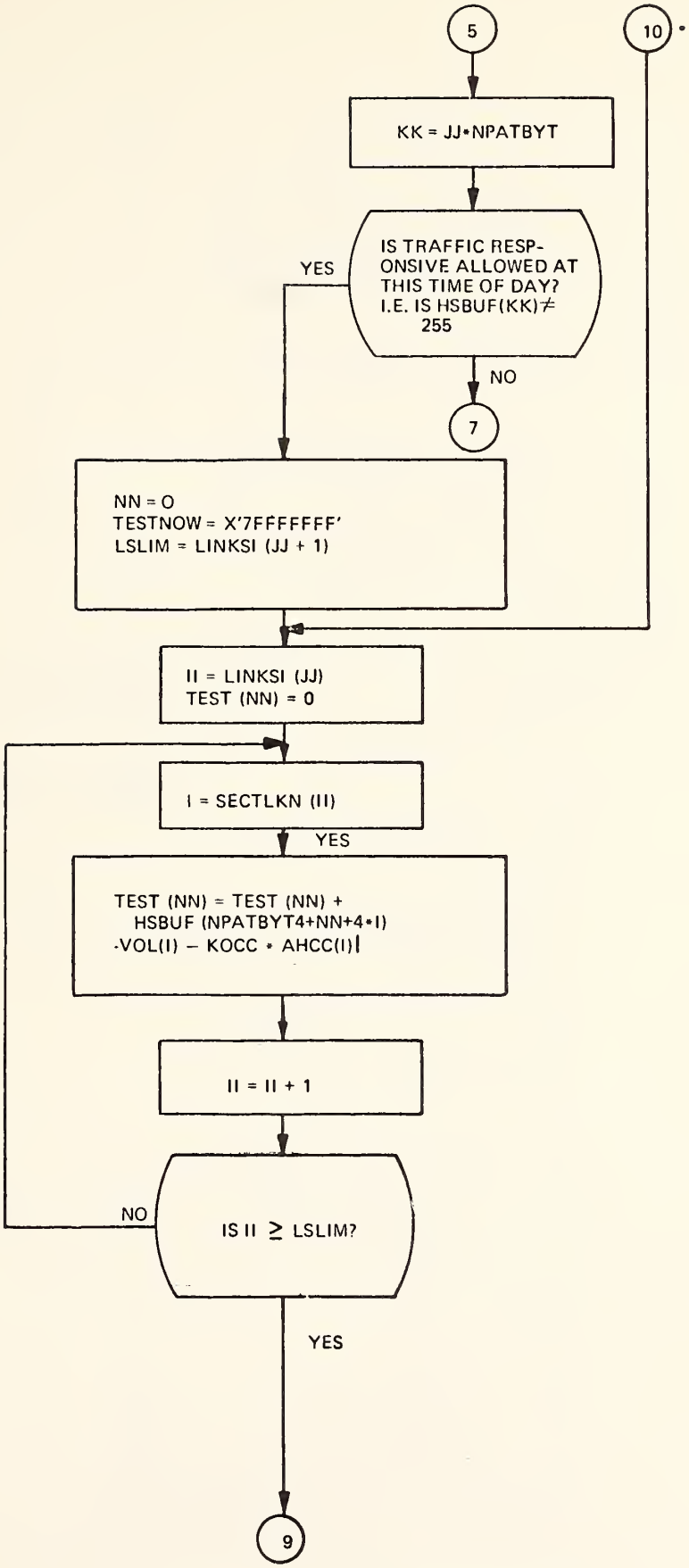


FIGURE 2.24.5.3. ROUTINE W SPECIFICATION

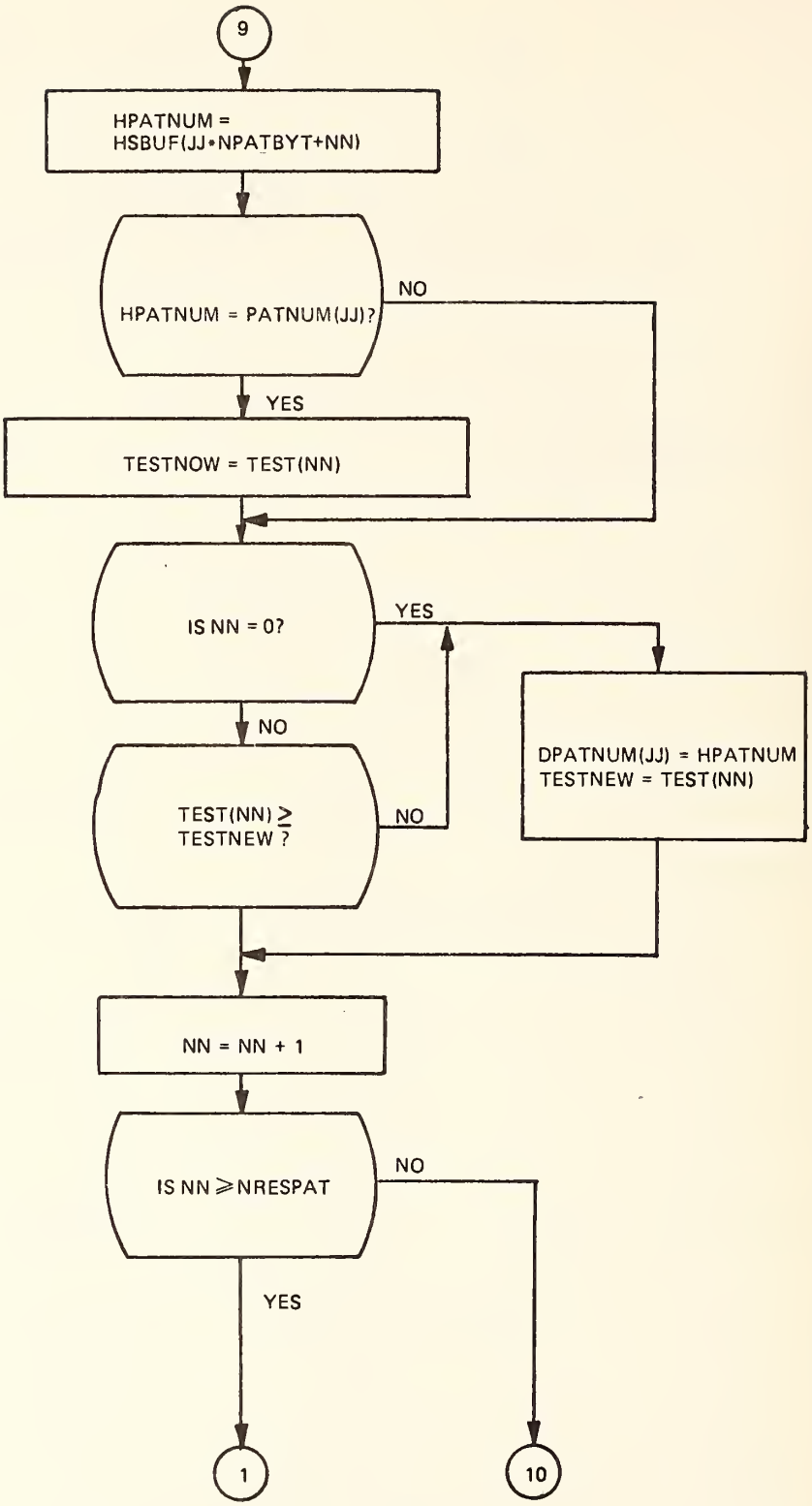


FIGURE 2.24.5.4. ROUTINE W SPECIFICATION

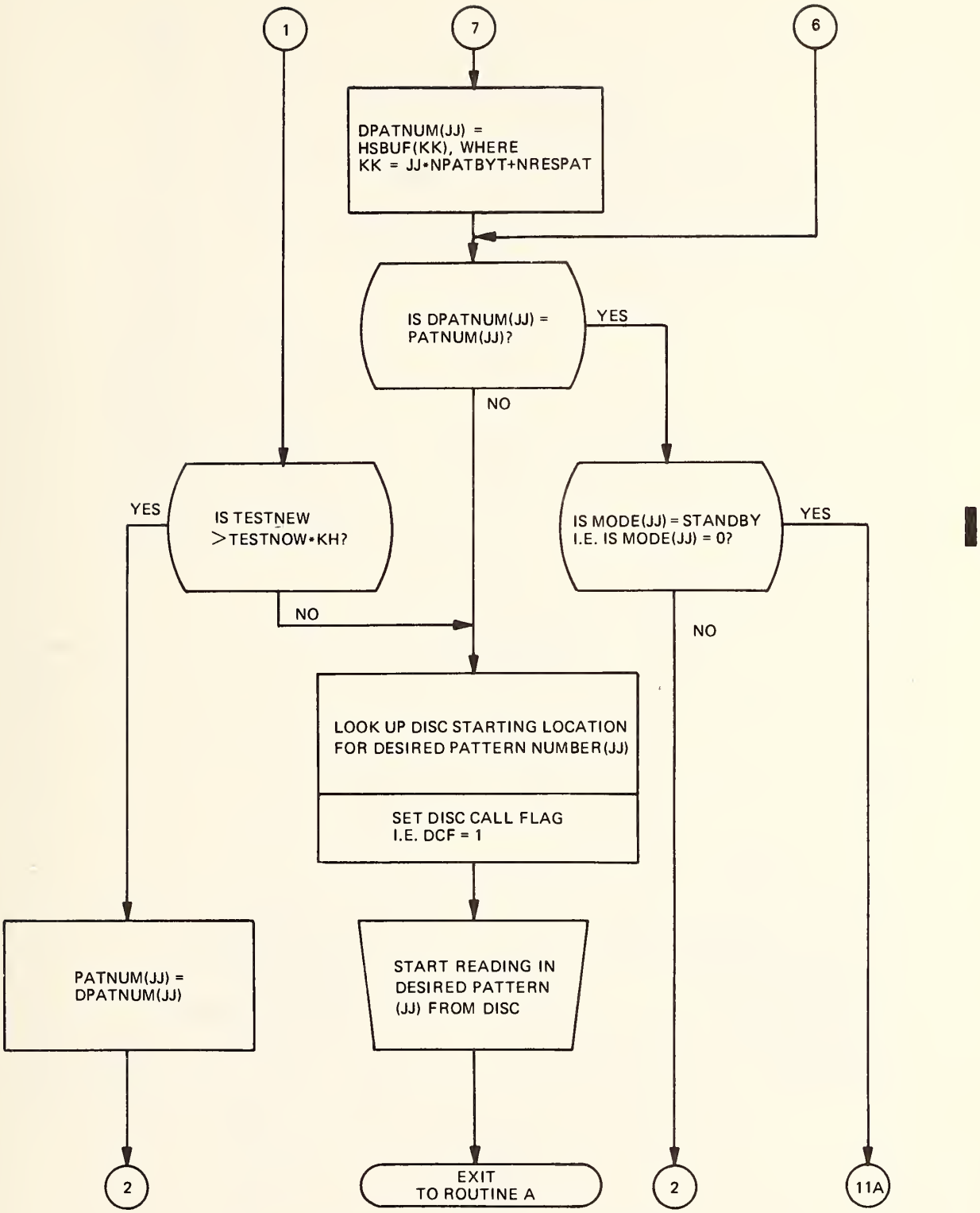


FIGURE 2.24.5.5. ROUTINE W FLOW CHART

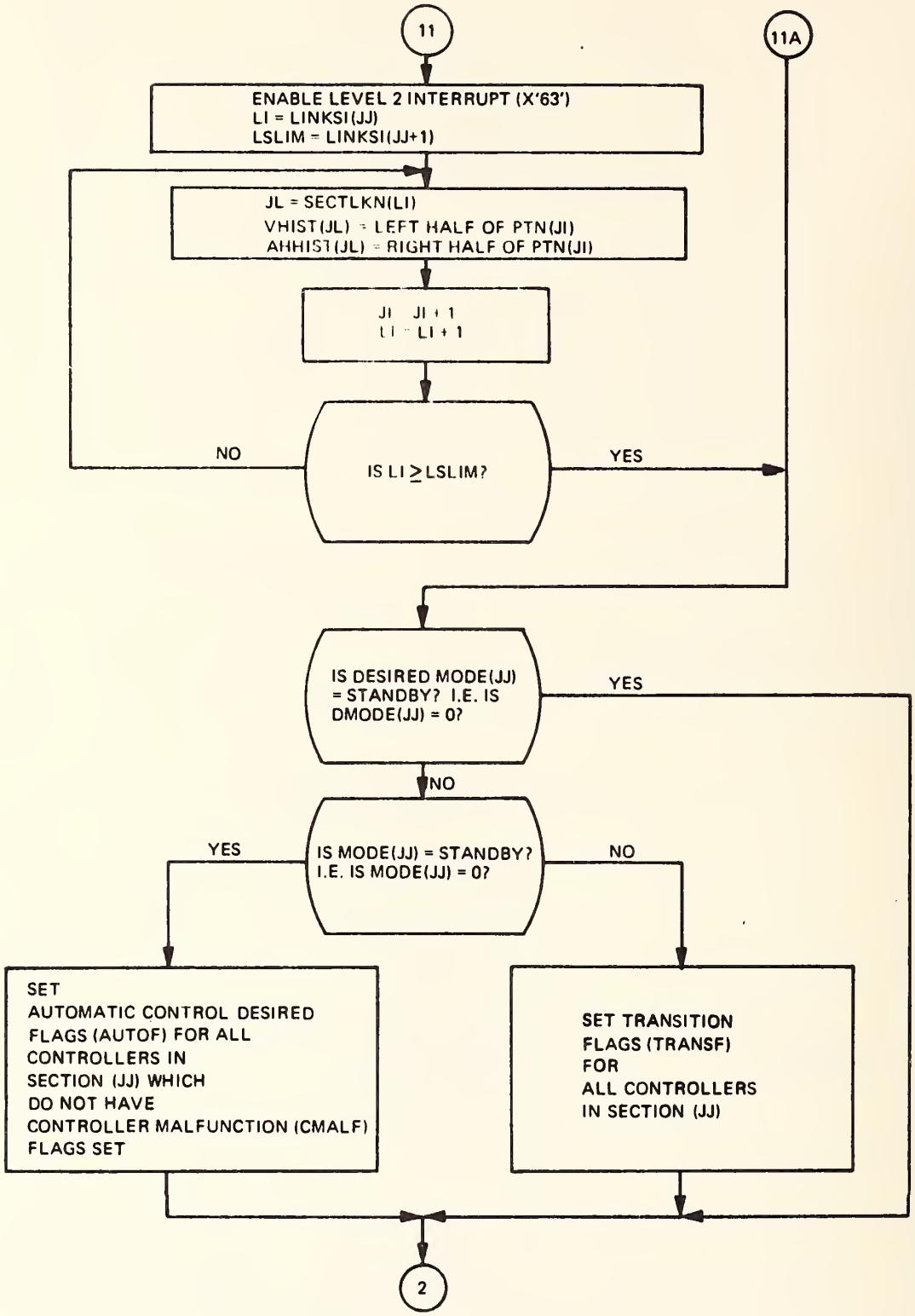


FIGURE 2.24.5.6. ROUTINE W FLOW CHART

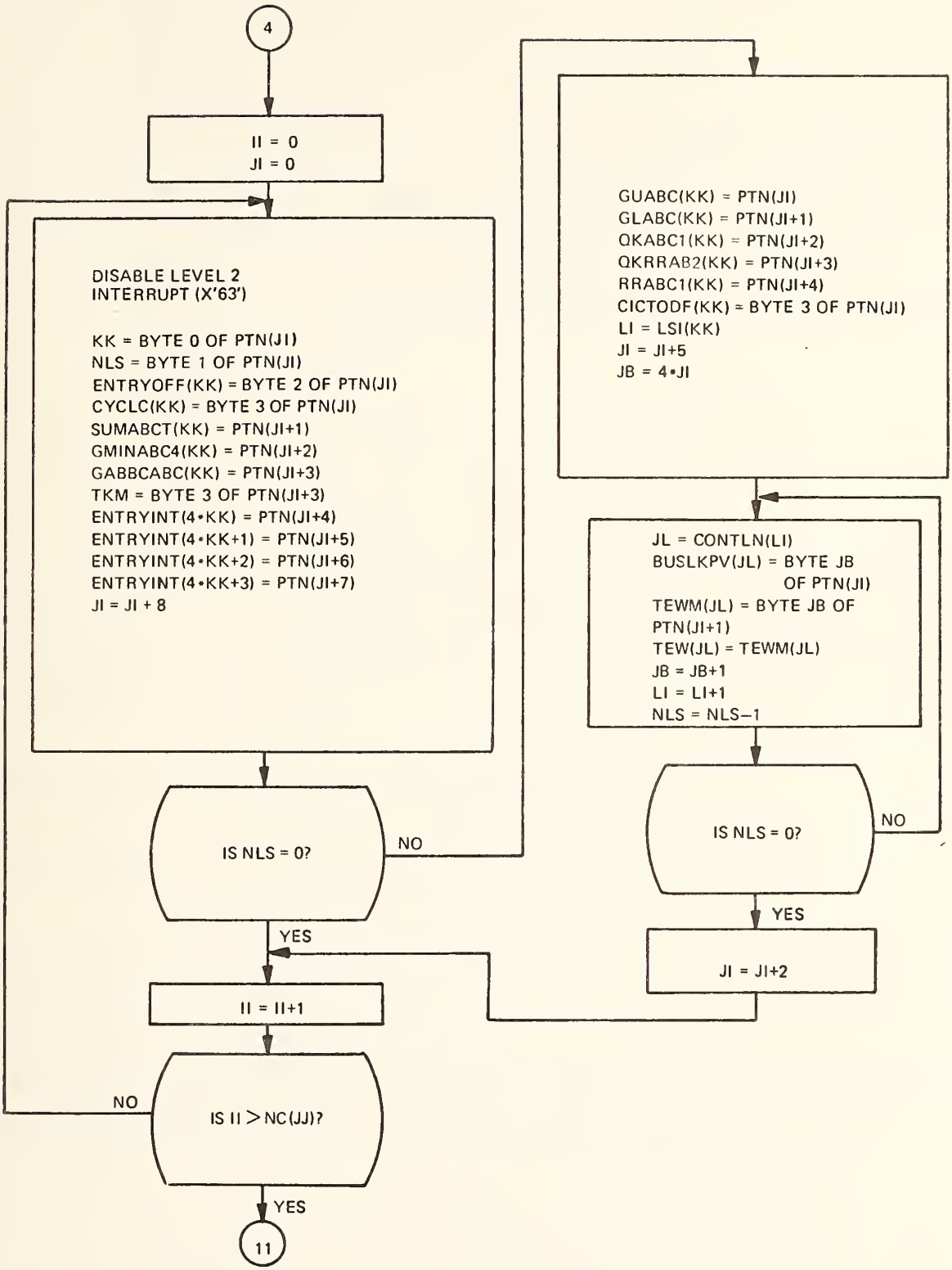


FIGURE 2.24.5.7. ROUTINE W SPECIFICATION

2.25 Routine X (Semi-Actuated Controller) Specification

2.25.1 Purpose

Semi-actuated controllers normally remain in A-phase green, and go through a B-phase vehicle or pedestrian sequence (or a combination thereof) only when a vehicle or a pedestrian demand is present at a specified time within the controller cycle. The proposed UTCS computer program will transmit a yield pulse to the semi-actuated controller on a once-per-cycle basis. The controller will use this pulse to initiate one of the following B-phase sequences as a function of the existing demand at the intersection:

1. Pedestrian sequence
2. Vehicle sequence
3. Combination of the above two sequences
4. No B-phase sequence

For (1), (2), or (3) above, the local controller will initiate and time the A-phase clearance intervals and the required B-phase vehicle or pedestrian intervals. The total time required for the sum of these intervals will vary as a function of the demand, but the requested sequence will always be completed within a prescribed maximum time duration after the yield pulse.

The function of the semi-actuated part of the UTCS computer program is to generate the yield pulse which will meet the following requirements:

1. Maintain the same cycle length at the semi-actuated controller as that which is in effect at the adjacent controllers in the section.

2. Transmit the yield pulse at such a time that the subsequent A-phase clearance intervals and the longest B-phase intervals will cause the next sequential beginning of A-phase green to occur at the desired main street offset time.

The procedure of (2) will maintain the desired main street vehicle progression speeds. The start of A-phase green may occur earlier than the offset time for the case of shorter B-phase intervals, but it will never occur later than this time.

The specific functions performed by Routine X, Semi-Actuated Controller Routine, are summarized briefly in the following lines:

1. Transfer the semi-actuated controller from standby to computer control smoothly.

2. Time the intervals required to transmit the yield pulse to the controller.

3. Perform controller state error detection to verify that the controller is returning to A-phase green.

4. Maintain the required offset relationship with respect to the adjacent controllers in the section.

5. Provide a smooth transition, under computer control, from one selection of cycle length and offset to another.

6. Transfer the semi-actuated controller from computer control back to standby smoothly.

2.25.2 Method

The Semi-Actuated Controller Routine will perform the following series of computations. Refer to Routine X Flow Chart Semi-Actuated Controller Routine, for a detailed functional flow chart of these computations.

1. The semi-actuated controller will be picked up from standby when the Automatic Control Desired Flag (AUTOF) is set, and the controller is in A-phase green. The A-phase green will be extended by the amount required to synchronize the controller to the computer-selected cycle length and offset, Entry Cycle Length Code (CYCLC) and Entry Offset (ENTRYOFF), respectively.

2. The computer will time the following two intervals:

   a. The first interval, GA, will extend from the desired offset time to the beginning of the first A-phase clearance interval, at which time the "Yield Pulse" will be set. The controller will then initiate the A-phase clearance intervals if a B-phase vehicle or/and pedestrian demand is present.

b. The second computer-timed interval, GB, will extend from the beginning of A-phase pedestrian clear up to the desired offset time. It should be noted that this computer-timed interval corresponds to the summation of the following intervals at the semi-actuated controller:

- A-phase clearance intervals.
- Maximum B-phase vehicle or pedestrian passage intervals.
- B-phase clearance intervals.

3. The computer program will perform controller state error detection by checking for the presence of A-phase green during the 1/2 second time period prior to the normal transmission of the "Yield Pulse". If this return is not present, the program will take the following steps:

a. Place the controller into standby (HOLD = 0)

b. Set the "Controller Malfunction Flag."

c. Call the CRT Failure Table Add subroutine, which is part of Routine K, CRT Control and Data Formatting.

4. The computer will compare the desired offset, Working Offset (WRKOFF), with the measured offset, Tc_k, at the beginning of the first computer-timed interval. If an adjustment is required due to either an operator offset change or an offset error, the program will adjust the first interval by the required amount subject to the constraints that the change be greater than -4 seconds and less than cycle minus 4 seconds. It should be noted that these restrictions also apply to a transition, which is described below.

5. The program will provide a smooth transition from one selection of cycle length and offset to another at the start of the first programmed interval. At this time, the following data transfers will take place:

- Entry $_{GA}$ to GA
- Entry $_{GB}$ to GB
- "Entry Cycle Length Code" to "Working Cycle Length Code".
- "Entry Offset" to "Working Offset".

The actual transition will be effected by either decreasing (up to four seconds) or increasing the first computer-timed interval.

6. The semi-actuated controller will be transferred from computer control back to standby at the end of the first computer-programmed interval, GA, when the "Standby Desired Flag" is set. This technique will maintain at least as much A-phase green at the controller as that which existed under computer control. The initial A-phase green may be longer than this duration by as much as one controller standby cycle length when there are vehicle and/or pedestrian demands present at the intersection. The A-phase green may extend indefinitely if there is no demand.

Routine X is called by the Level 2 Executive routine, Routine A1. Routine A1 calls Routine X if there is at least one semi-actuated controller in the group of 32 controllers being processed. Upon entry, Routine X examines each of the 32 controllers, with array SEMMSK, to determine if it is a semi-actuated type. When a semi-actuated controller is located, array HOLD is examined to see if the controller is in standby. A semi-actuated controller in standby is brought on line if the automatic control desired flag, AUTOF, and corrected A-phase green return, AOG, are set.

After a semi-actuated controller has been brought on line, AUTOF is reset and the countdown register, CNTDR, is counted down from its initial value of ENTRYINT (1+16 * CONTRN) which contains duration entry GB. Entry GB extends from the beginning of A-phase pedestrian clearance up to the desired offset time. This interval is composed of the A-phase clearance intervals, maximum B-phase vehicle or pedestrian passage intervals, and B-phase clearance intervals.

After CNTRN has counted down to zero, the interval number, INTNUM, is set to 1, and an adjustment is made for the required offset relationship with respect to the adjacent controllers in the section. The desired offset, WRKOFF, is compared with the measured offset, KCL-KCTC, to form deviation EPSILON. If an adjustment is required (EPSILON≠0) due to either an operator offset change or an offset error, the program will adjust the first interval by the required amount subject to the constraints that the change be greater that -4 seconds and less than the cycle length minus 4 seconds.

If the transition flag, TRANSF, is on, a smooth transition is provided from one selection of cycle length and offset to another at the start of the first interval, by transfer of appropriate entry data to working storage. These operations are performed prior to the offset corrections described in the previous paragraph.

After the offset corrections are made, the count-down register is set to entry GA plus the final offset correction, if any. Entry GA extends from the desired offset time to the beginning of the first A-phase clearance interval. After CNTDR has counted down, INTNUM is set to 2 and AOG is examined. If AOG is zero, the controller is assumed to have malfunctioned. At this time the controller malfunction flag, CMALF is set and the controller is dropped into standby by setting HOLD to zero. After this operation, the ADD FAILURE UPDATING SUBROUTINE is called to record this failure. If AOG is a "one" and the standby desired flag, STBYD, is set, the flag is reset and the controller is placed in standby. If AOG is set and STBYD is not set, CNTDR is set to entry GB and the yield pulse, YIELD, is set.

For each call to Routine X, the above operations are repeated for each of the 32 controllers being examined. Upon examining all 32 controllers, the routine is exited.

2.25.3 Repetition Rate

This routine is executed following the completion of Routine V, Critical Intersection, which is the last routine in the Do-Loop for traffic-adjusted controllers. The routine is executed once per 1/2 second for each semi-actuated controller in the system.

2.25.4 Cross Reference

This routine is part of the controller loop Level 2 Routines. It follows Routine V.

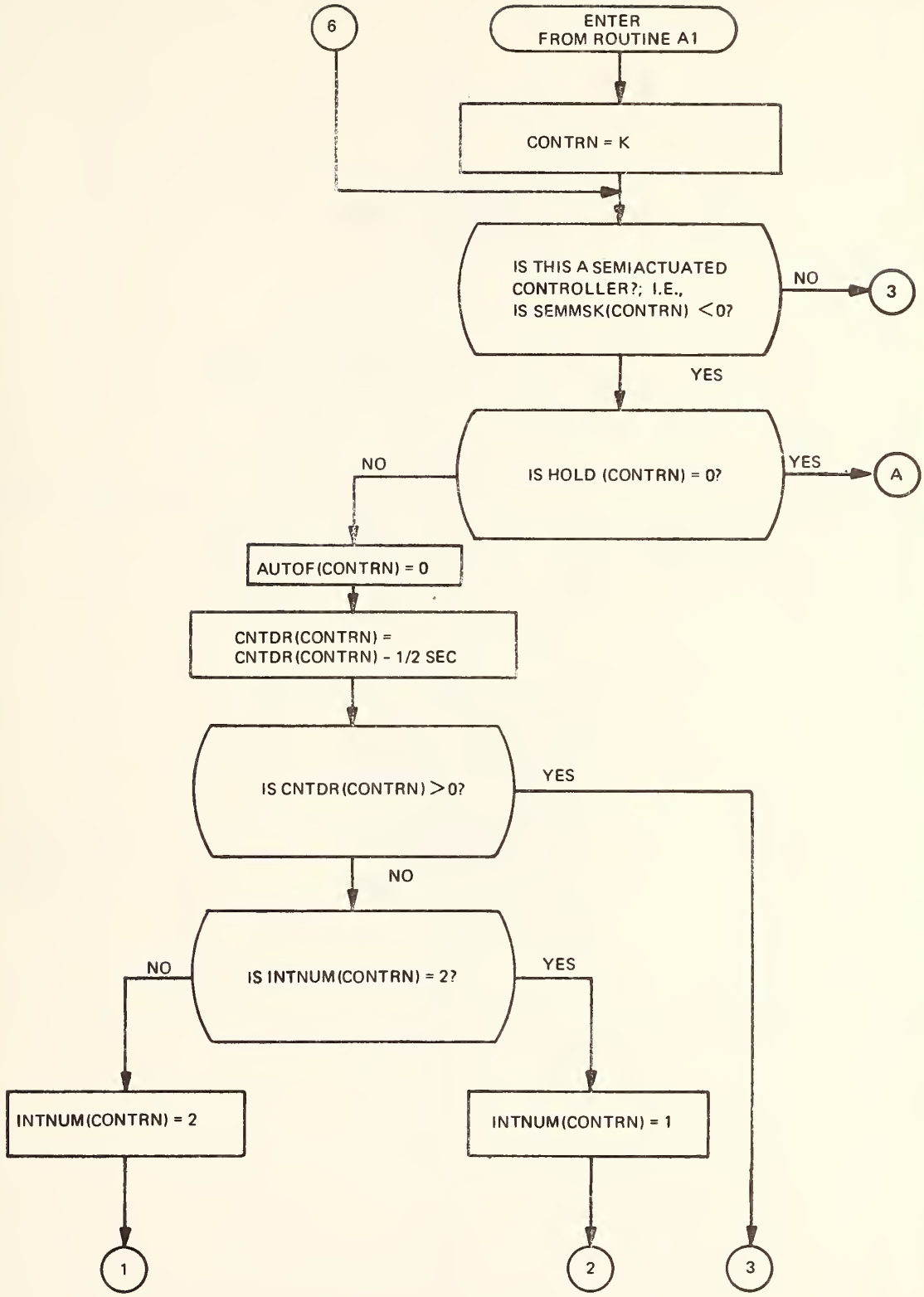


FIGURE 2.25.5.1. ROUTINE X FLOW CHART

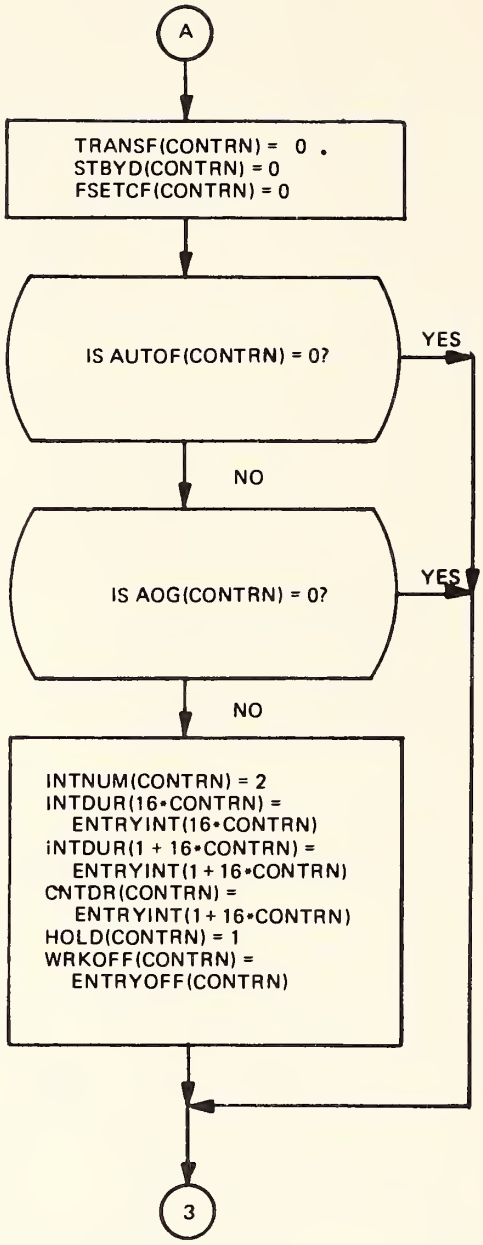


FIGURE 2.25.5.1. ROUTINE X FLOW CHART

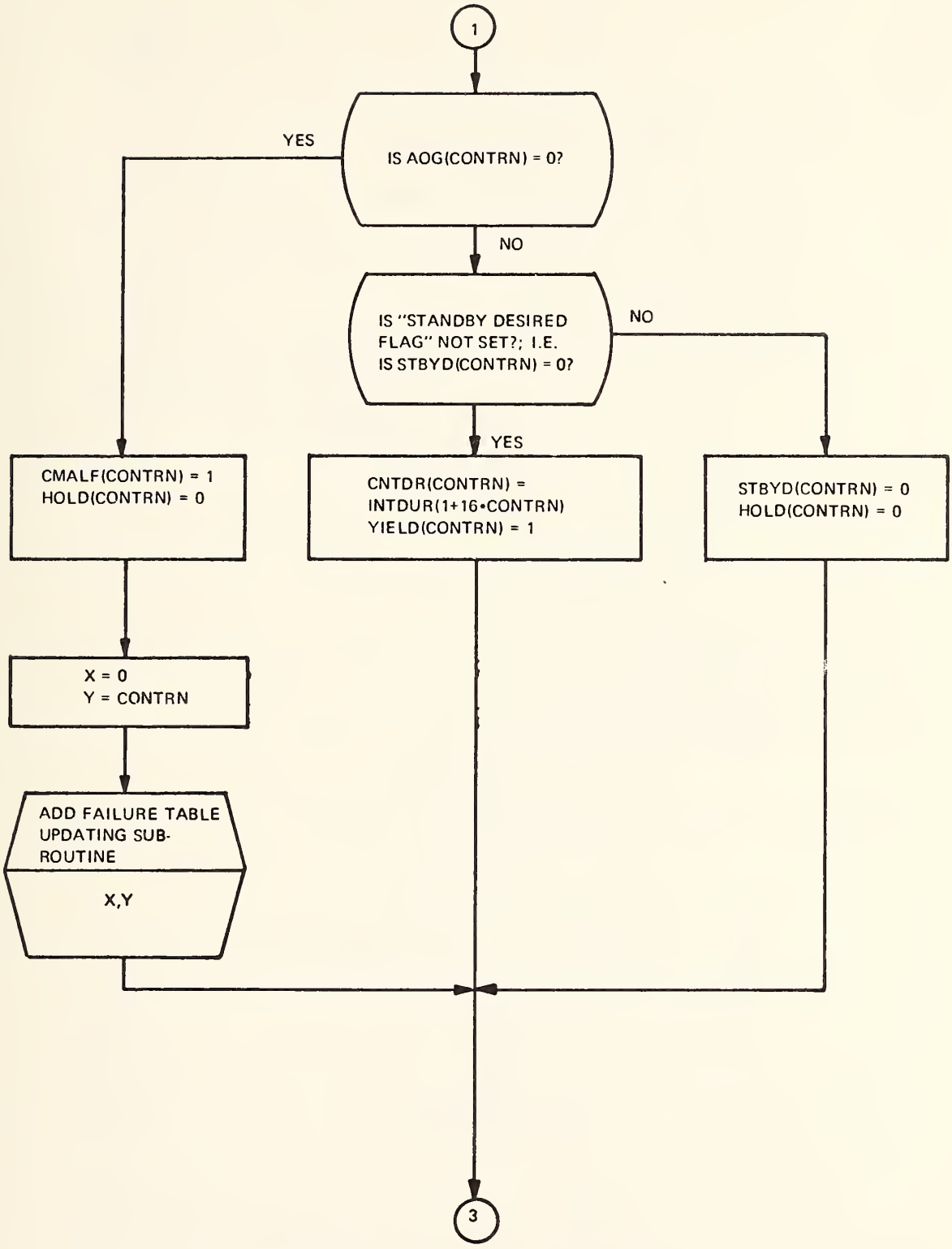


FIGURE 2.25.5.2. ROUTINE X SPECIFICATION

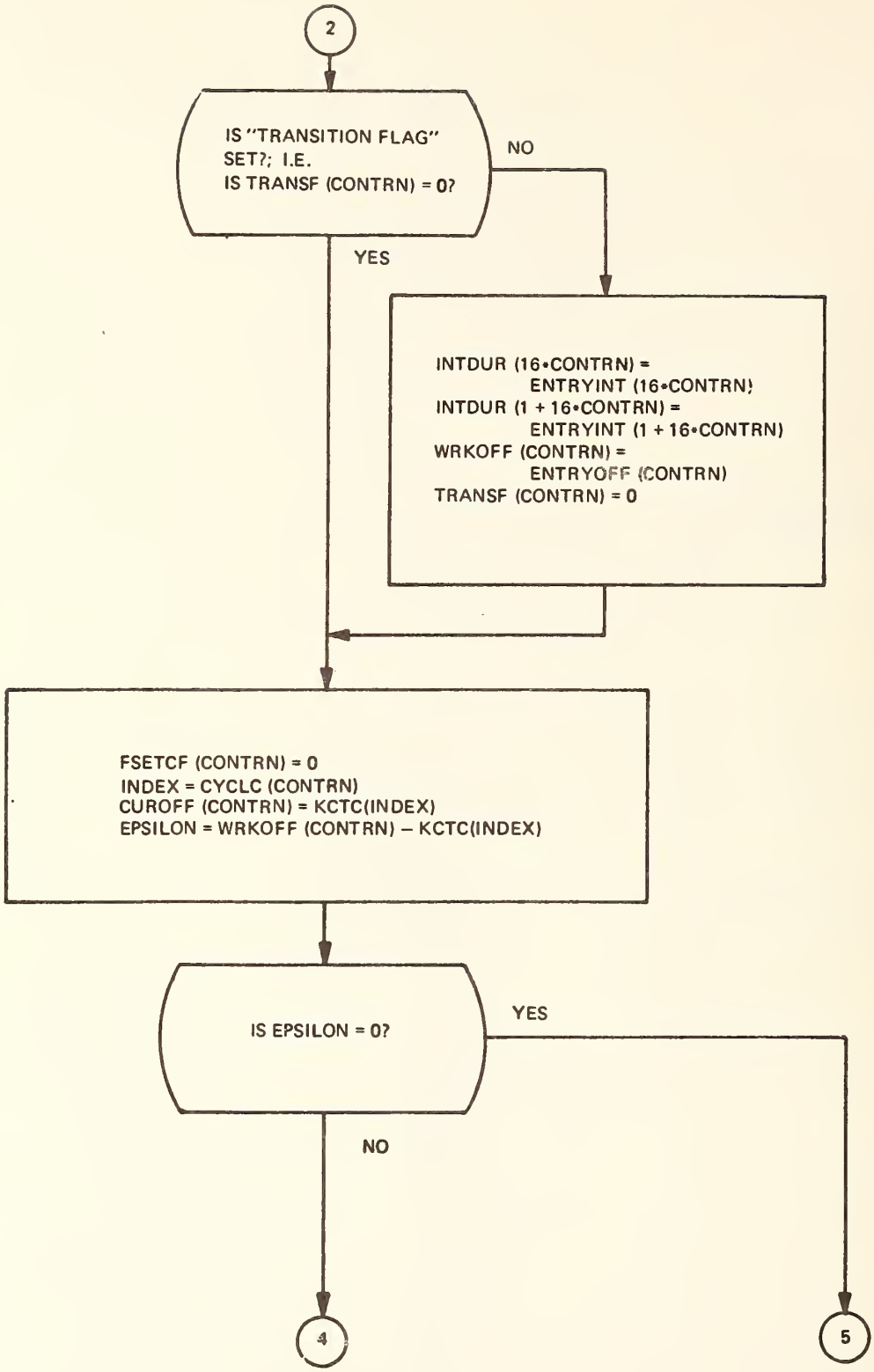


FIGURE 2.25.5.3. ROUTINE X SPECIFICATION

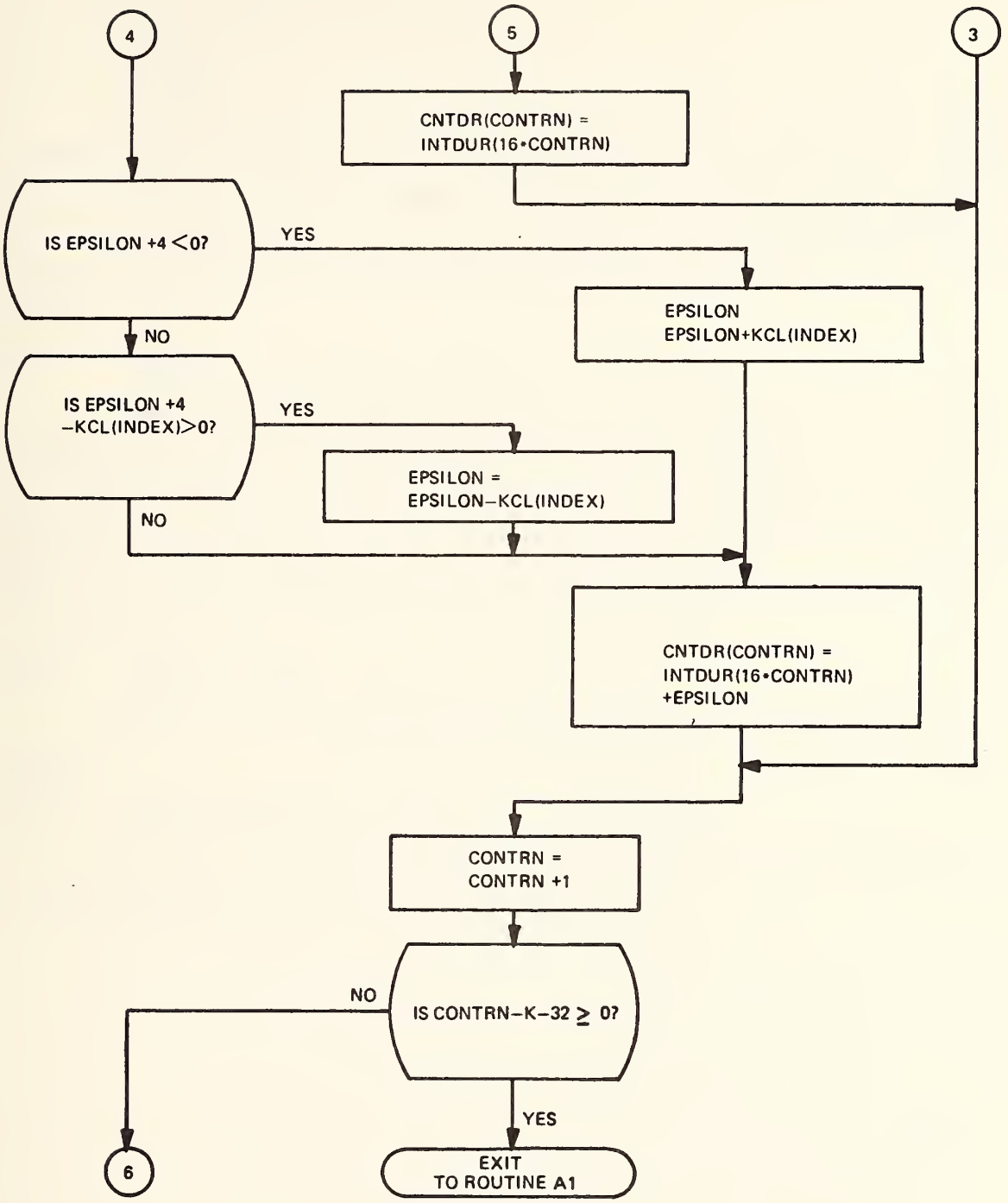


FIGURE 2.25.5.4. ROUTINE X SPECIFICATION

2.26 Routine Y (Start-Up) Specification

2.26.1 Purpose

The Start-Up Routine is entered at the start of real time operations. After the program is read in from disc, this routine requests CRT System Status page and initializes the displayed data. The Start-Up Routine contains data for constants, fixed and variable arrays, and assigns reserve areas for dynamic storage. The constants and arrays are initialized by the assembler and the dynamic storage area is initialized, to zero, by this routine.

2.26.2 Method

When the program is read in from the disc, at operator request, it initializes all dynamic arrays to zero. The arrays stored at shut down are read in from disc if sense switch 4 is in the down position. The routine then initializes the TOD clocks as per the operator inputted TOD. It then transfers directly to the Level 1 executive initialization loop of Routine A which sets up the priority structure of the program and begins the real time processing.

2.26.3 Repetition Rate

Routine is only entered when system operation under computer control is initiated.

2.26.4 Cross Reference

The start-up procedure is requested by the operator through a monitor key-in. Upon completion it exits to the start of Level 1.

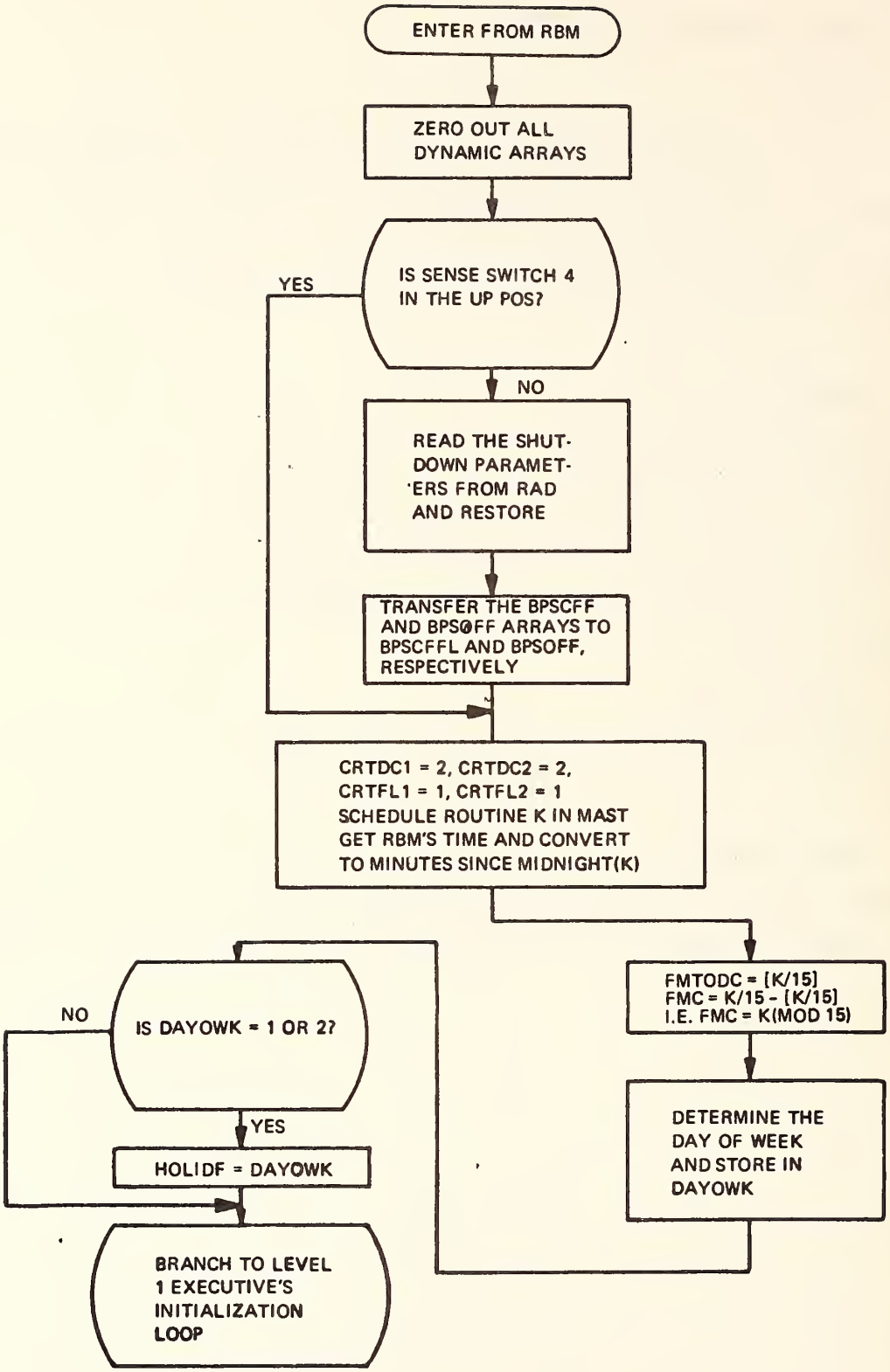


FIGURE 2.26.5.1. ROUTINE Y SPECIFICATION

2.27 Routine BA (BPS Executive) Specification

2.27.1 Purpose

The purpose of routine BA is to perform the following major functions:

- Write History Tape
- Maintain the program timing based on 1/32 second interprocessor interrupt and timing flags set by the UTCS CPU.
- Call routines in accordance with timing and sequence requirement.
- Save and restore the status of interrupted routine.

2.27.2 Method

The BPS Executive Routine (BA) consists of three tasks, each associated with an interrupt.

The highest task (interprocessor input interrupt task) is triggered each 1/32 second by the interprocessor interrupt. This task saves the status of the interrupted program and checks to see if the raw history data tape is being written. If it is, the necessary raw history data (see tape format in Figure 2.27.2.1) is collected and is outputted every half second to the tape unit in compressed 7-track binary form. The format of the Bus Data, Vehicle Data, A-Phase Green Return Data, Control Panel Input Data, Hold Signal Data and Control Panel Output Data is the same as the format of the data is the arrays listed in Table 2.27.1 and defined in the Glossary (Section 3).

Table 2.27.1 RAW HISTORY DATA TAPE FORMAT

Data	Glossary Symbol With Same Format
BUS	BARR
Vehicle	P1, P2, P3 or P4
A-Phase Green Return	AOG
Control Panel Input	CPANIN
Hold Signal	HOLD
Control Panel Output	CPANOUT

The Radio-Synch Signal is in a bit array indexed by radio central cycle length code (presence is a "1") and the Advance Pulse Data is in a bit array indexed by controller (advance is a "1"). The half second flag is checked and if it is set, priority Level 1 is triggered. The task then restores the status of the interrupted routine routine before releasing control.

Priority Level 2 task is triggered every second by the Level 1 task. This task saves the status of the interrupted program and calls the Level 2 routines. The Level 2 routines are called in the following order: Bus Link Timing (BD), Bus Priority Algorithm (BE), and Malfunction Detection (BF). In addition once each minute Routine B is entered for computer evaluation.

The executive routine restores the status of the interrupted routine before releasing the Level 2 priority task.

2.27.3 Repetition Rate

This routine is entered every 1/32 second.

2.27.4 Cross Reference

This routine controls the entry of all other bus priority routines.

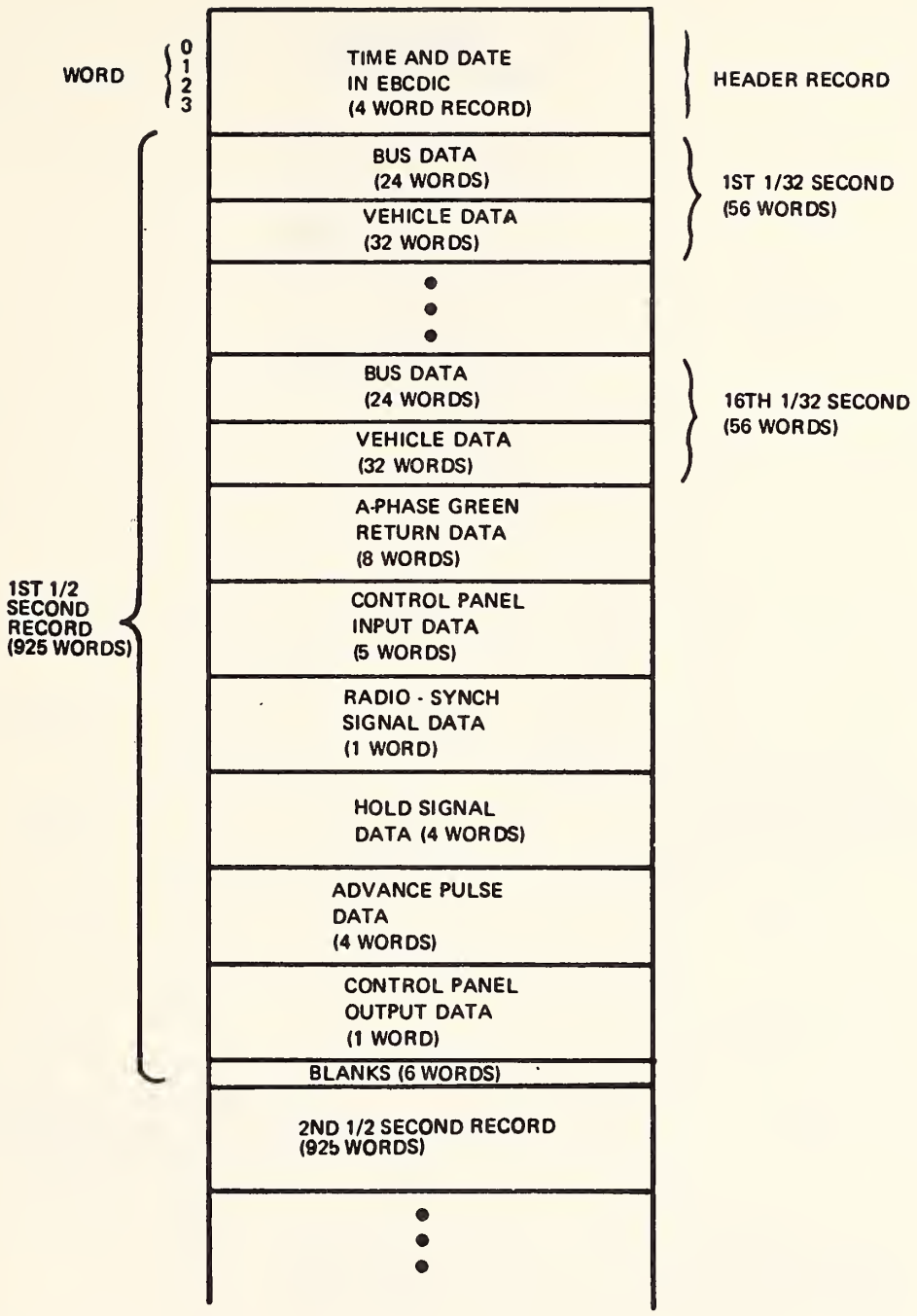


FIGURE 2.27.2.1. RAW HISTORY DATA FORMAT

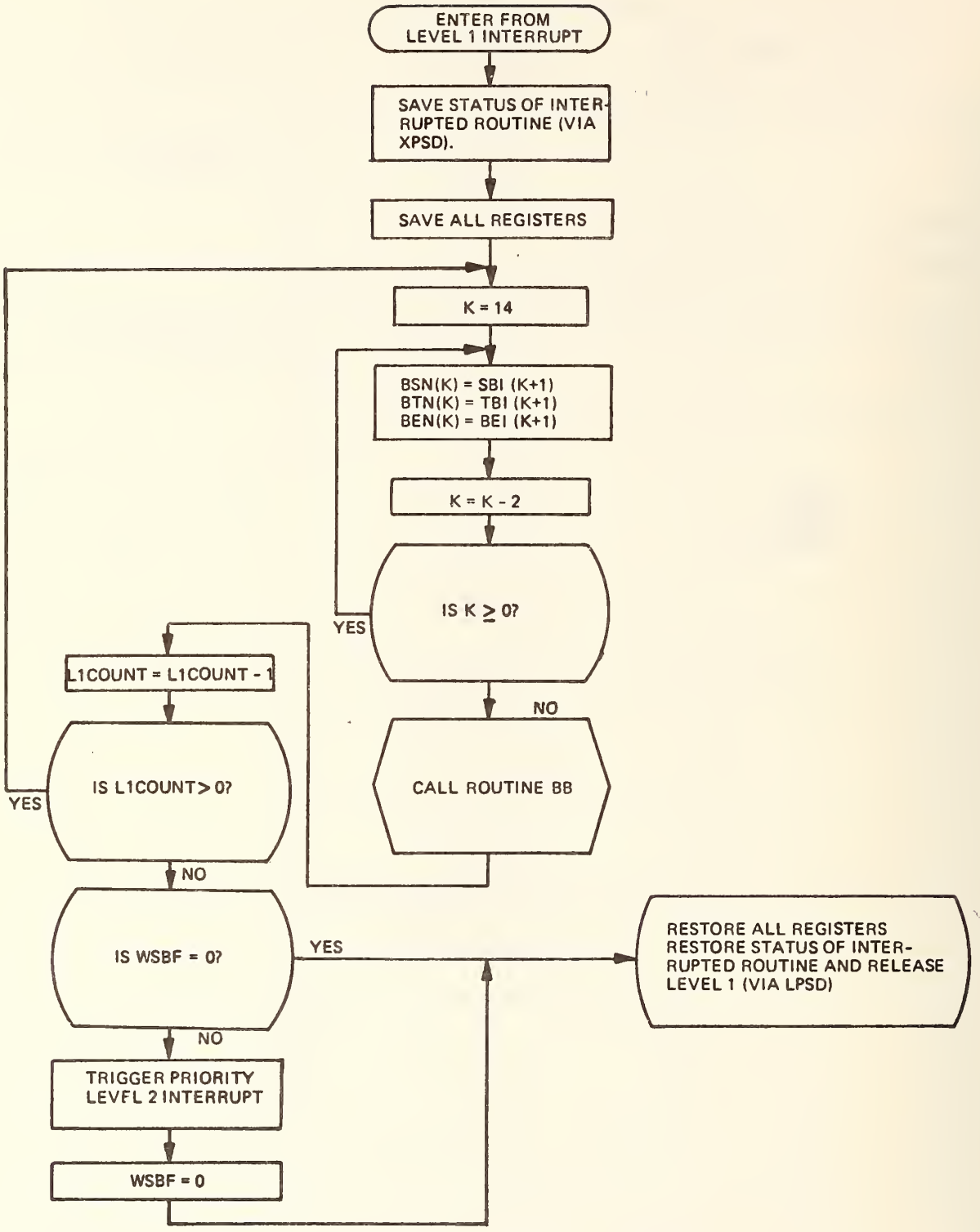


FIGURE 2.27.5.1. ROUTINE BA SPECIFICATION

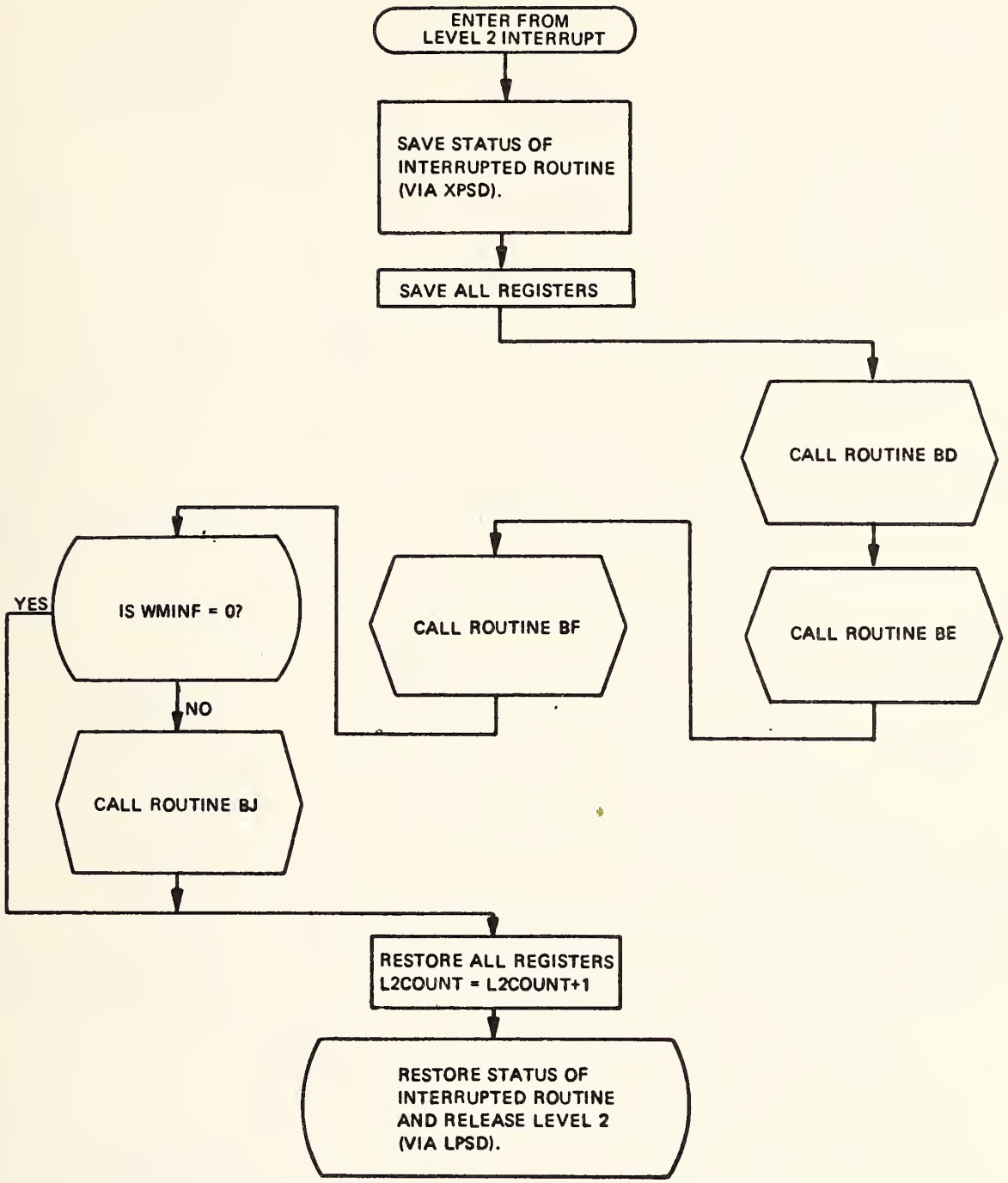


FIGURE 2.27.5.2. ROUTINE BA SPECIFICATION

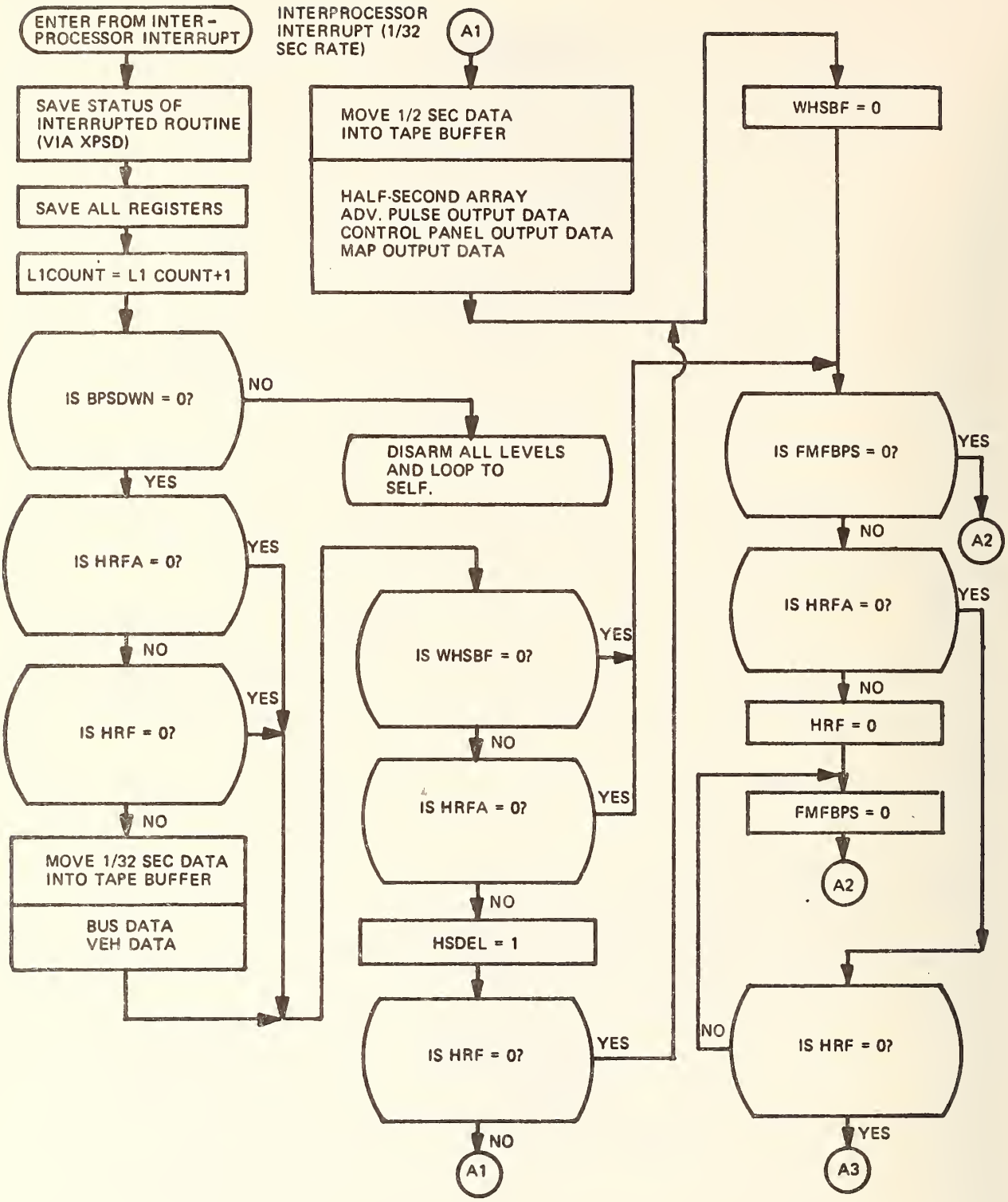


FIGURE 2.27.5.3. ROUTINE BA SPECIFICATION

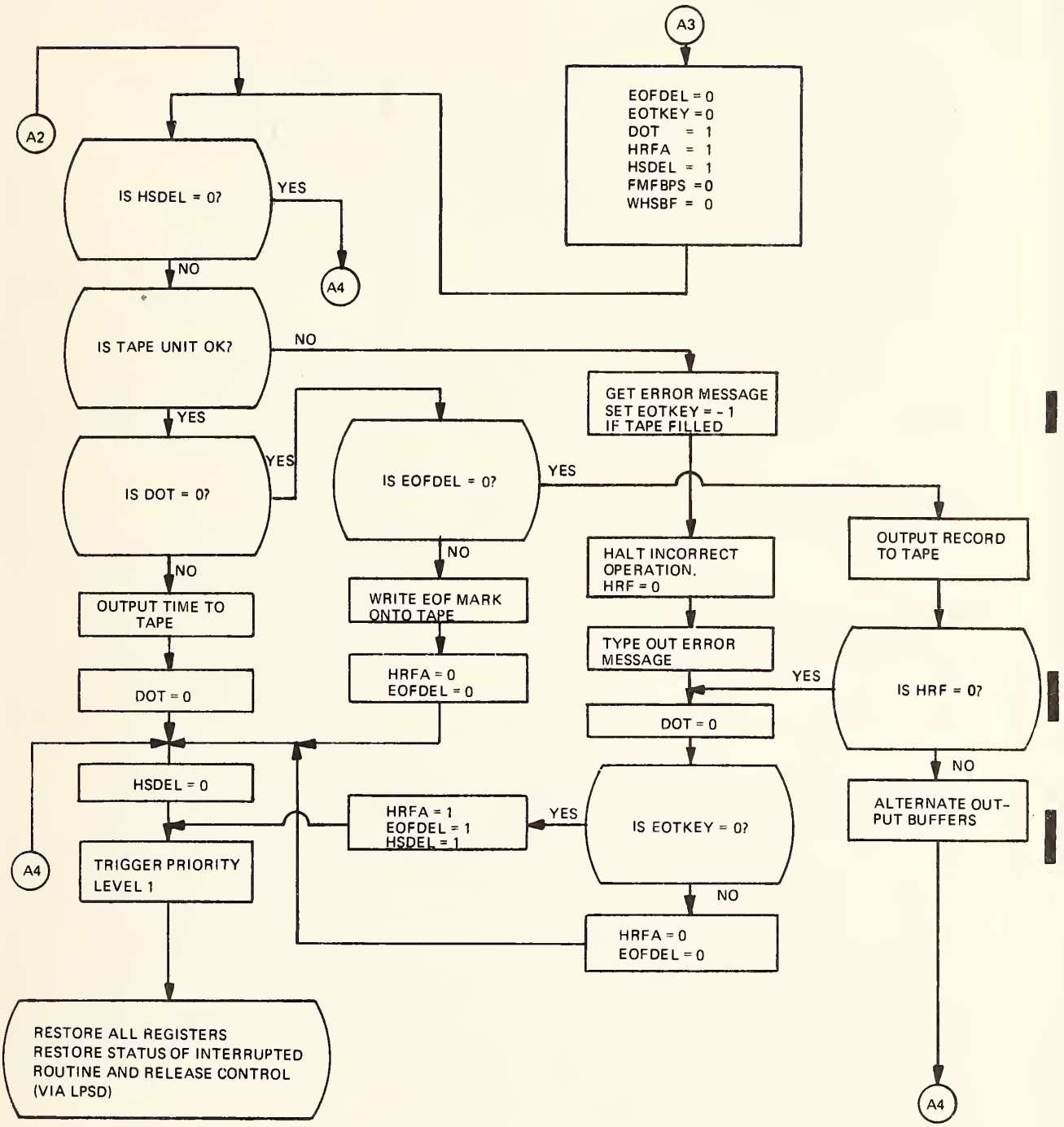


FIGURE 2.27.5.4. ROUTINE BA FLOW CHART

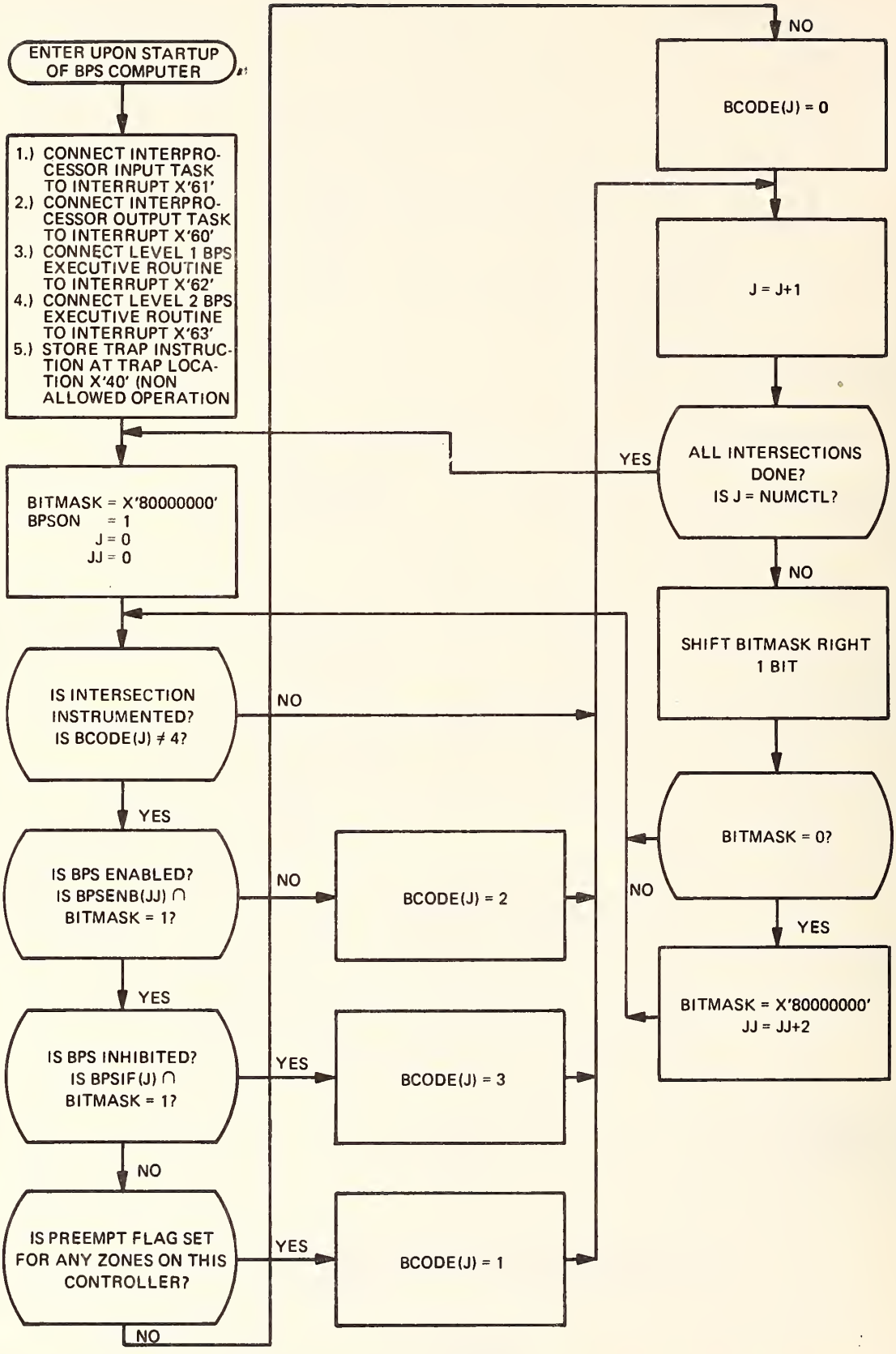


Figure 2.27.5.4. Routine BA Flow Chart Startup and Idle of BPS Computer

2.28 Routine BB (BPS Detector Data Input) Specification

2.28.1 Purpose

The purpose of routine BB is to perform the following major functions:

- Sense and record detector communications failures
- Sense the passage of a bus over a bus detector
- Enter Routine BC (Once Per Bus) each time a bus passage is detected and the corresponding detector failure flag and communication failure flag are not set.

2.28.2 Method

This routine is called by the executive routine BA, each 1/32 second. Two sets of values of raw bus detector data are available, one set stored by the UTCS Executive routine (A) representing the present iteration values the other saved by this routine representing last iteration values. The raw bus detector data is divided into three, word-interleaved arrays. Each array consisting of 8 words, carrier array (BEN), stop bus array (BSN) and thru bus array (BTN). The previous iteration values are formatted identically (BEL, BSL, BTL).

The routine first examines the carrier bits (on a whole word basis) to determine whether a communication failure has occurred as evidenced by a change of state from a one bit, carrier present, to a zero bit, carrier absent. Failures are recorded in the BPS communication failure flag array (BPSCFF).

Routine BB then proceeds to process the stop bus data. Simple logical handling of current stop bus words (BSN) with those stored from the previous iteration (BSL) permits detection of a stop bus upon the instant its presence over a detector ceases to be evidenced (as indicated by a change of state from a 0 bit, vehicle present, to a 1 bit, vehicle absent). This procedure guards against false counts since the 50 msec bus presence pulse can be sensed over two successive 1/32 second sampling intervals. Routine BC, once per bus, is entered upon detection of a stop bus and the absence of a communication or detector failure. Routine BC has two entry points. For stop bus and

thru bus. The even and odd bit positions in the entry word to routine BC correspond to the upstream and downstream bus detectors.

Routine BB proceeds through an identical series of operations on the through bus raw data.

2.28.3 Repetition Rate

This routine is entered every 1/32 second.

2.28.4 Cross Reference

This routine is called every 1/32 second by the BPS Executive Routine, Routine BA. It calls the Once per Bus Routine, Routine BC. After completion, control is passed to the BPS Executive Routine.

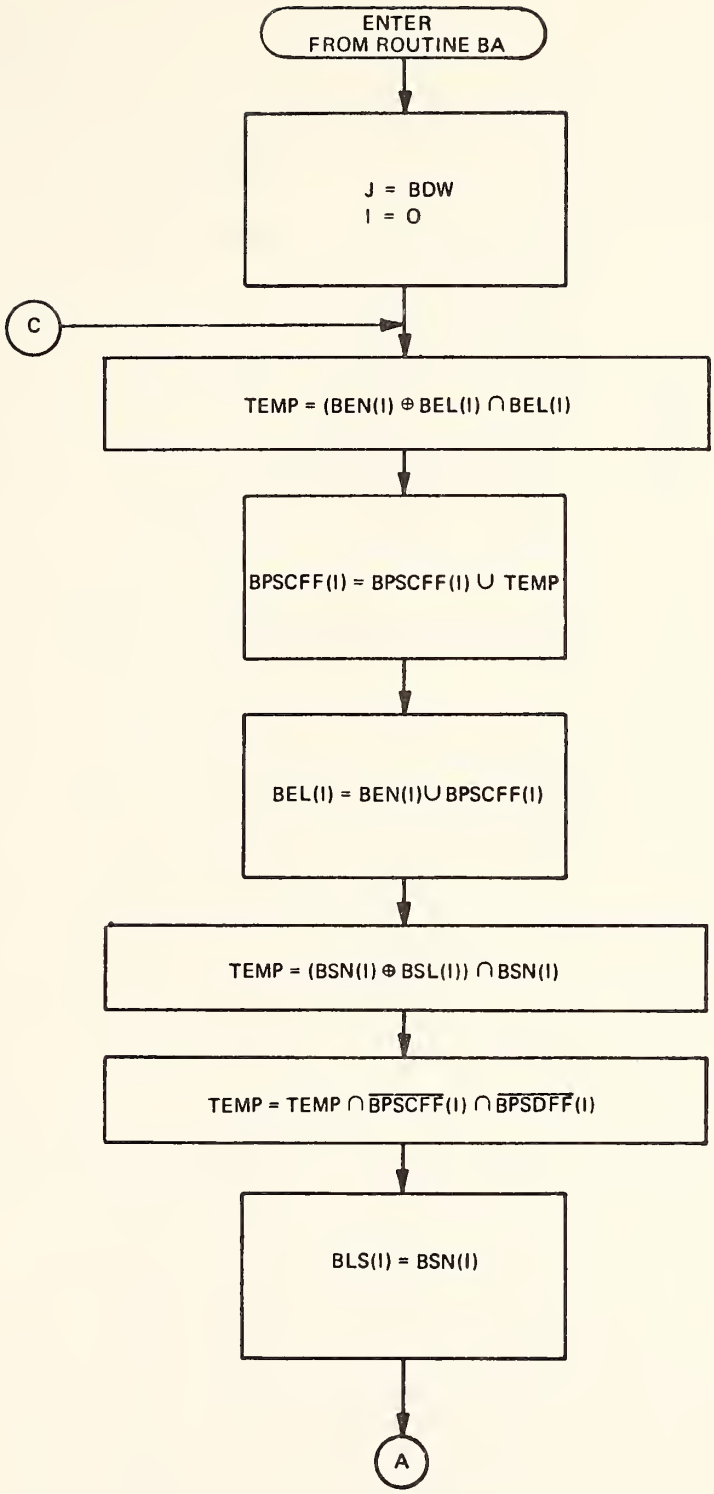


FIGURE 2.28.5.1. ROUTINE BB SPECIFICATION

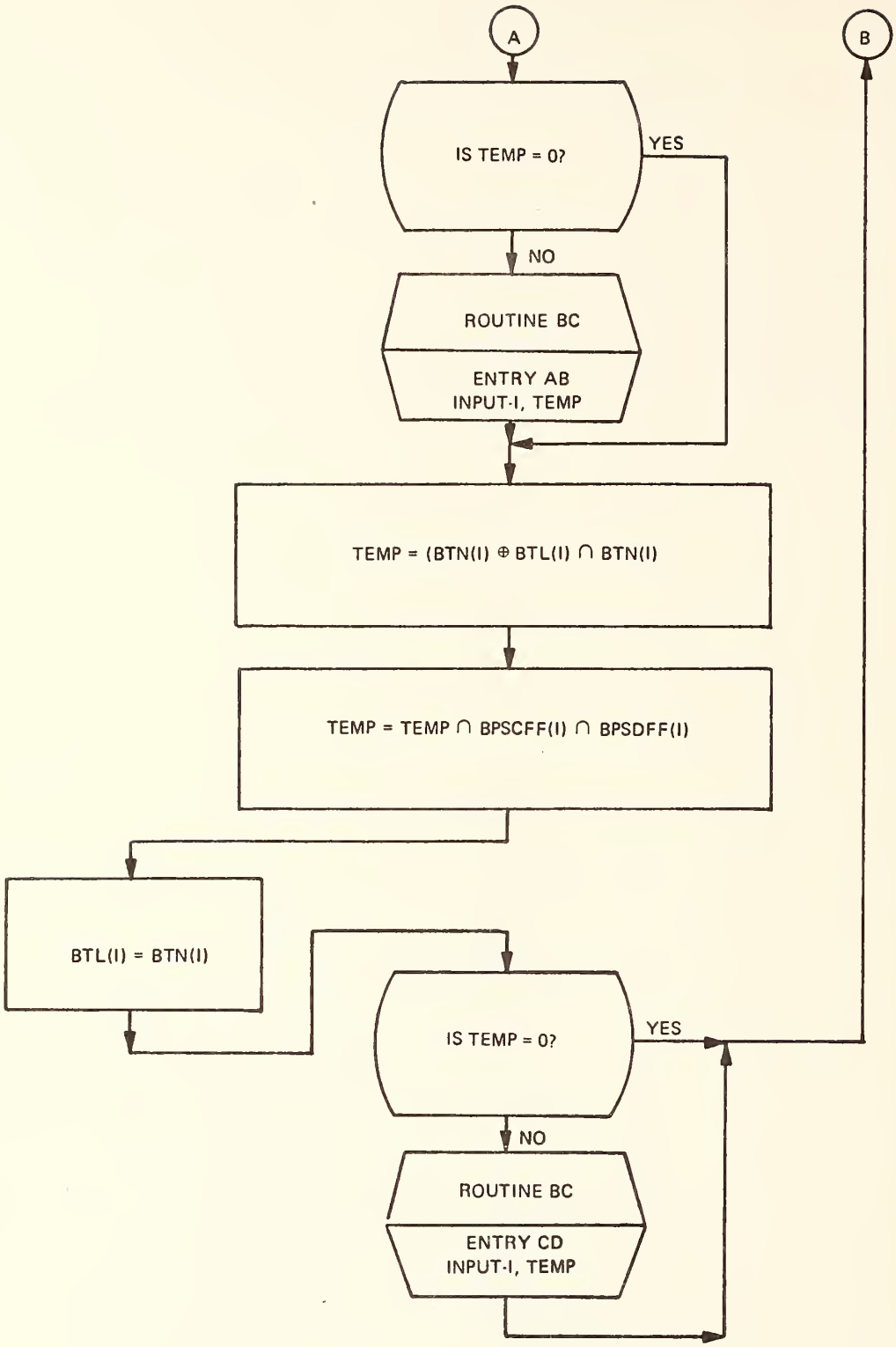


FIGURE 2.28.5.2. ROUTINE BB SPECIFICATION

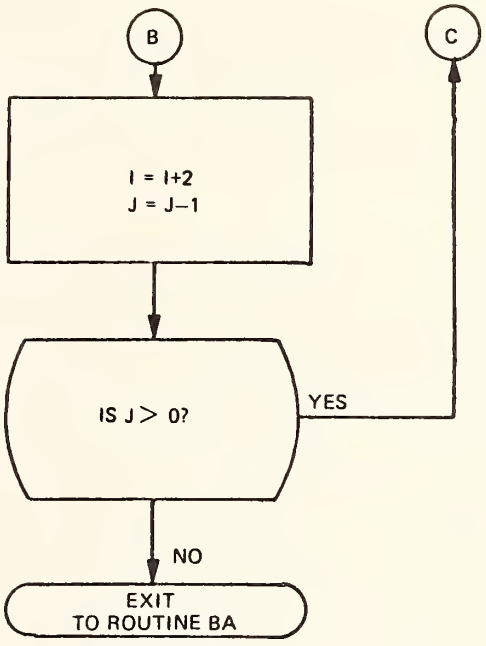


FIGURE 2.28.5.3. ROUTINE BB SPECIFICATION

2.29 Routine BC (Once Per Bus) Specification

2.29.1 Purpose

Routine BC carries out the following functions for each bus detected:

- Computes a continuous zone count including both stop and through buses.
- Performs upstream and downstream detection malfunction checks based on out of normal zone counts.
- Resets "No bus in cycle" flags orginally set in routine BD to guard against bus errors developing in zone counts.
- Accumulates 15 minute stop and thru bus volume counts for printout and display.
- Accumulates 15 minute stop and thru bus "Eligible" and "helped" bus counts for printout and display.

2.29.2 Method

Routine BC is entered at one of two entry points each time a bus is detected in routine BB. The two entry points correspond to whether the bus detected was a stop (AB entry) or a through (CD entry) bus. At each entry point, the ABFLAG is set to indicate the type of entry. Register R4 contains the bus detector states of the detector word index contained in register R3. The even numbered bits of R4 represent the upstream detectors and the odd numbered bits represent the downstream detectors. The computations are performed in accordance with the flow chart of section 2.29.3.

Branches A and C correspond to stop and thru bus detections over an upstream detector, respectively, and thus indicate an entry into the bus zone. The routine checks the detector and communications failure status* before proceeding to update zone count and performing a downstream, detector failure test based on an excessive positive zone count. If a failure is detected, a flag is set to key Routine BF-BPS Malfunction Detection Routine BF. If no failure is noted, BPS enabled and BPS inhibited flags are examined to determine whether BPS operation is in effect at that intersection and requires further data

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*Malfunctions are sensed automatically by the computer, but repairs must be entered manually by the operator.

processing. If BPS operation is not in effect an exit is made back to Routine BB. Otherwise, the "No Bus in Cycle" flag originally set by Routine BD -BPS Link Timing Routine- is reset and the stop or thru bus 15 minute volume count is incremented. The eligible stop or thru bus flags are then examined to establish whether the appropriate eligible bus count should be incremented. For the first eligible stop or thru bus in each cycle a corresponding stop or thru bus clearance clock is initialized to allow clearance of buses already in the zone before the eligible bus count is decremented by downstream bus detector inputs.

Branches B and D correspond to stop and thru bus detections over a downstream detector, respectively, and thus indicate an exit from the bus zone. The routine again tests detector and communications failure and takes appropriate action as before. In the absence of failure indications, the zone count is decremented and an upstream detector failure test is carried out based on excessive negative zone count. If a failure is detected a flag is set to signal Routine BF as before and an exit is made to Routine BB. If no failure is noted, BPS enabled and BPS inhibited flags are examined to determine whether further data processing is necessary. If BPS operation is in effect at the intersection, the stop or thru bus clearance clock is tested to see whether the eligible bus count should be decremented. In either case the bus clock is also tested to see whether the helped bus count should be incremented.

It should be noted that Routines BB and BC initiate BPS detector and communications failure checks on all BPS intersections whenever the BPS computer is active. All other detector input data processing takes place only if BPS is in effect at a given intersection. Special attention should also be given to the definition of eligible and helped buses. Eligible buses are counted in during the period the eligible bus flag is set. No eligible buses are counted out until the first such bus arriving each cycle can logically proceed out of the bus zone. This definition is necessary to prevent erroneous eligible bus counts tracing to the clearing of zone by buses arriving in the non-eligible period. Helped buses are defined as those clearing the bus zone after the bus clock runs out; i.e., after the end of normal green.

2.29.3 Repetition Rate

This routine is asynchronous. It is entered each time the Bus Detector Data Input and Interpretation Routine detects a bus.

2.29.4 Cross Reference

This routine is called by Routine BB and returns to that routine.

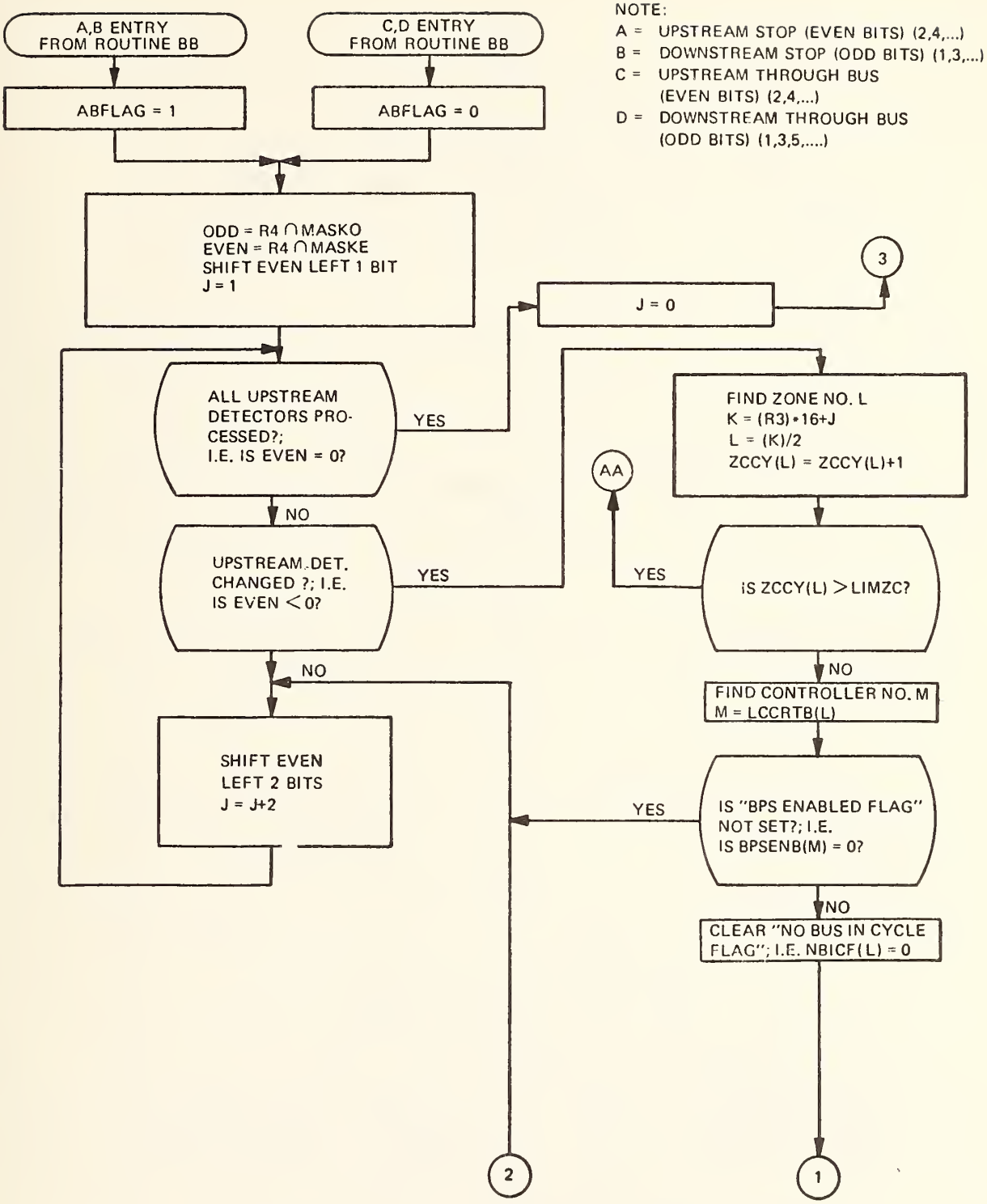

FIGURE 2.29.5.1. ROUTINE BC SPECIFICATION

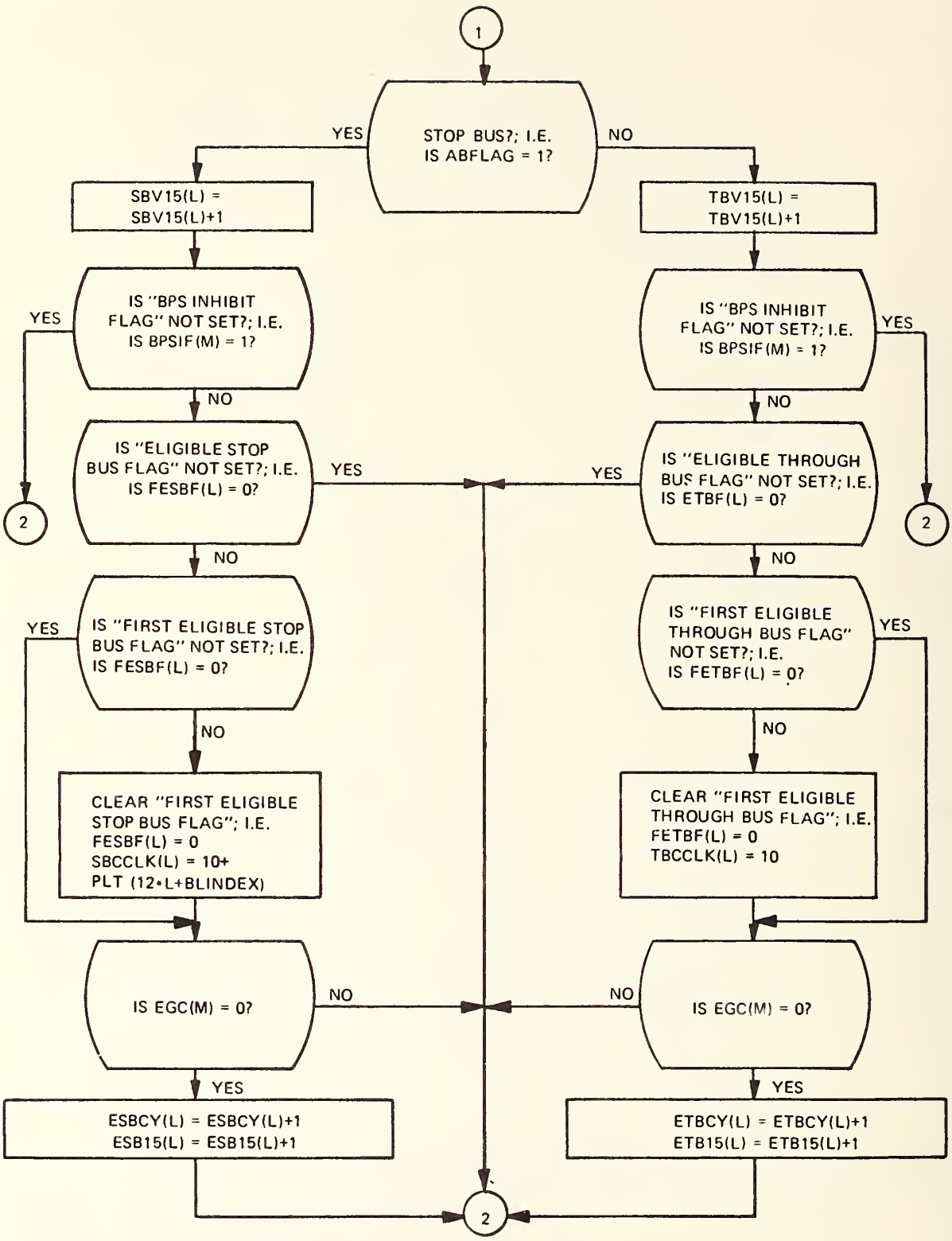

FIGURE 2.29.5.2. ROUTINE BC SPECIFICATION

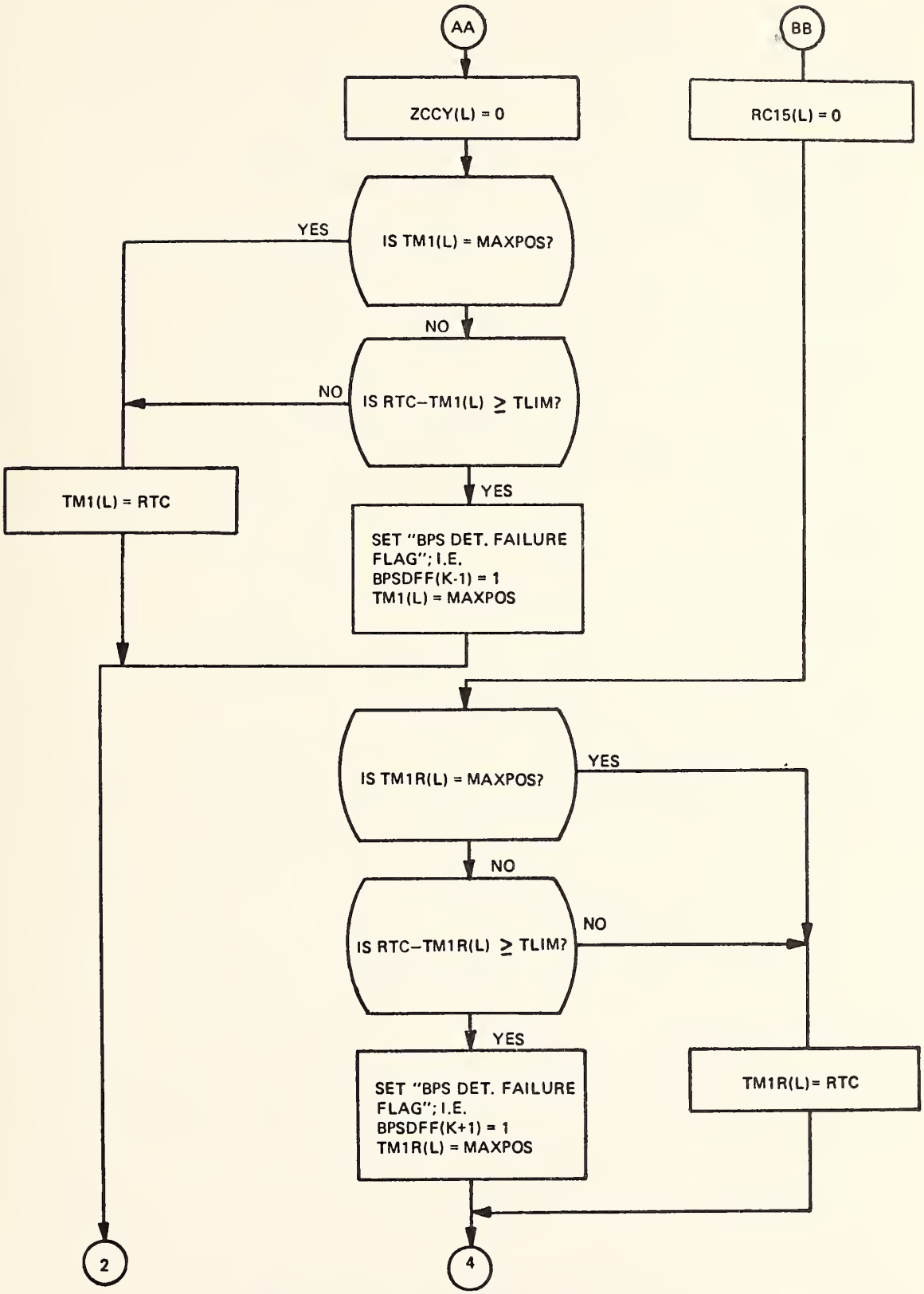

FIGURE 2.29.5.3. ROUTINE BC SPECIFICATION

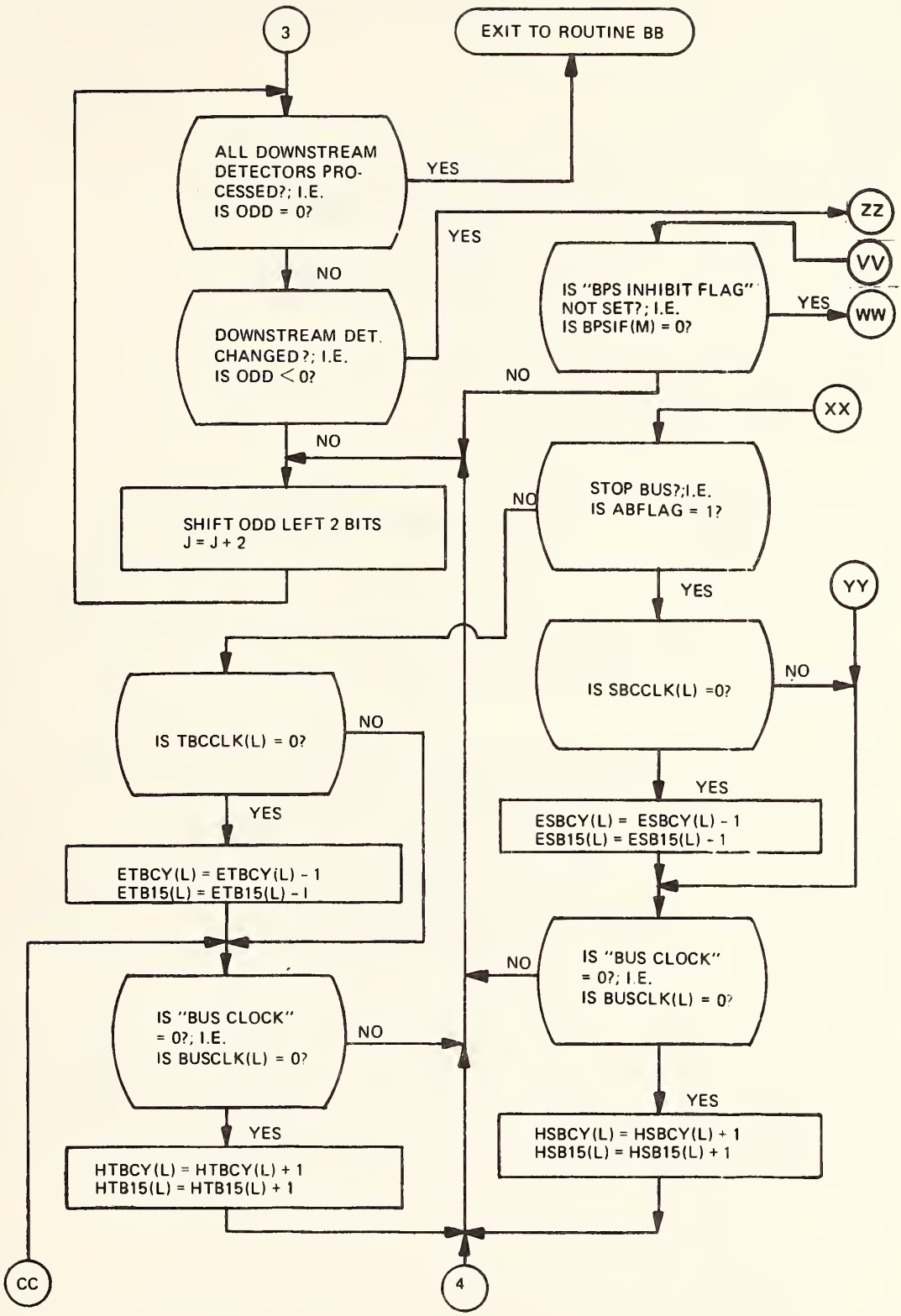

FIGURE 2.29.5.4 ROUTINE BC FLOW CHART

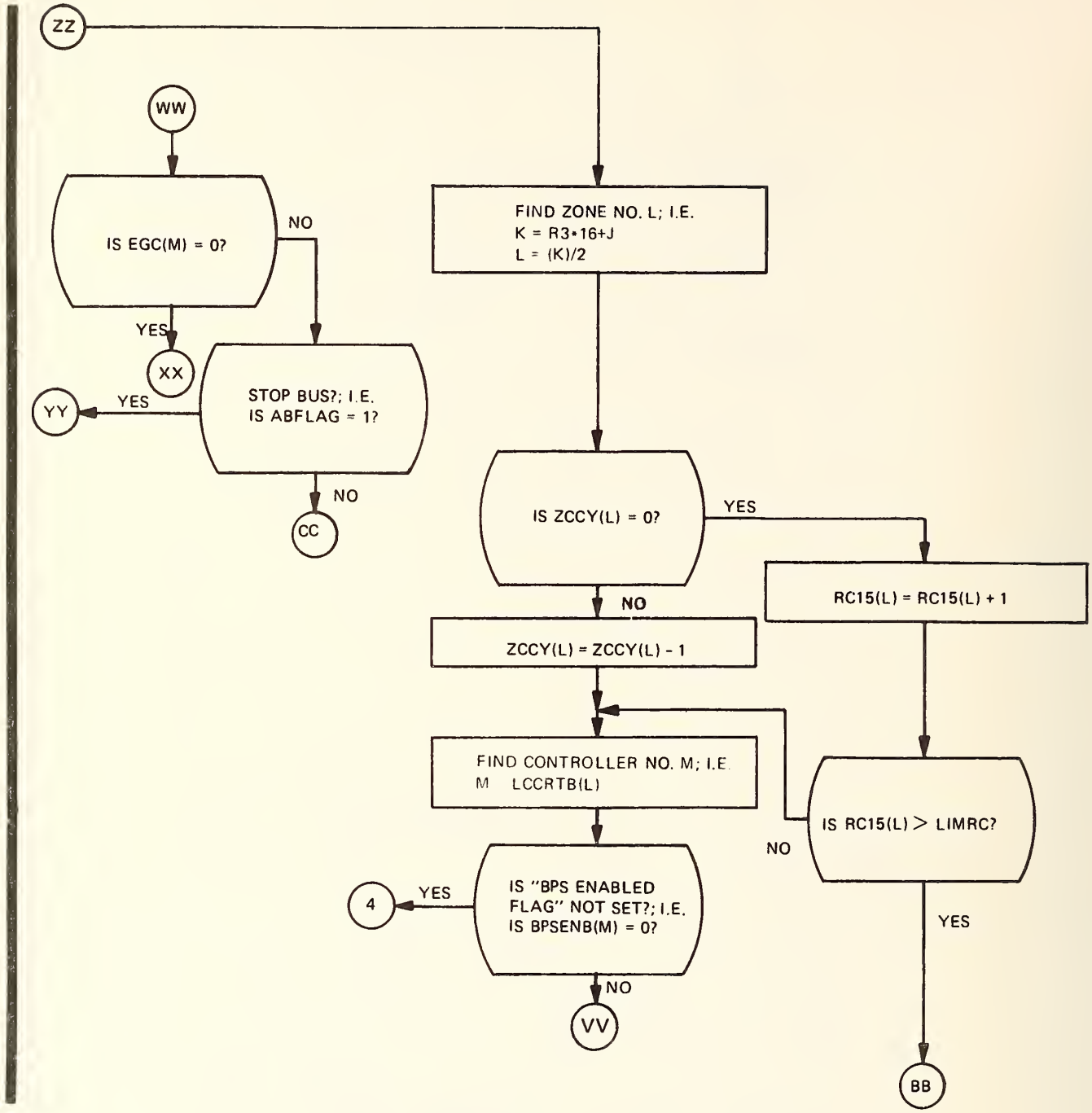

FIGURE 2.29.5.4 ROUTINE BC FLOW CHART

2.30 Routine BD (BPS Link Timing) Specification

2.30.1 Purpose

Routine BD carries out the following functions:

- Initialize BPS zone counts and MOE 1 time intervals once each cycle at the start of A-Phase Green for each BPS intersection.
- Initialize eligible bus counts, helped bus counts and bus clocks at the start of each bus action period during a cycle.
- Compute eligible bus entry period durations for each bus action period.
- Load and count down MOE 1 periods and bus clocks for each bus action period.
- Set flags to identify when eligible bus entry periods exist and when BPS algorithmic calculations should be made.

2.30.2 Method

This routine is called for once every second by the BPS Exective Routine, Routine BA. Upon completion of the two main branches of Routine BD, an exit is made back to the executive routine.

The first branch encountered upon entry to the routine is controller oriented, each controller being processed in succession. Each of the controllers is first checked to establish whether a valid BPS operation has been set up. If so, an initialization process is carried out when the Interval 1 Start Hold flag is set by the UTCS CPU. This includes initializing the MOE 1 period index number and zeroing all bus zone counts where no bus entries have occurred in the previous cycle.

If a bus action period coincides with the MOE 1 period referenced by the MOE 1 period index number, a further series of initialization steps are taken. These steps include zeroing eligible and helped bus counts, initializing bus clocks and setting up for MOE 1 countdown. When a bus action period is not called for, these last initialization steps are not taken. In either case, however, the appropriate MOE 1 period is loaded

in the MOE 1 clock (a value of zero is used when no bus action period is involved) and the MOE 1 period index number is advanced to prepare for later MOE 1 period entries. A check is also made of the period reduction flag so that the MOE 1 period just loaded can be reduced, if a previous BPS green extension for cross street traffic required such action to maintain a fixed cycle length.

All MOE 1 clocks are then decremented once each second. As each clock reaches zero, a new cycle of initialization occurs for the next MOE 1 period. The last MOE 1 period in a controller cycle is not counted down fully. Instead it is terminated by a new Interval 1 Start Hold flag which reintiates the first initialization process and the entire timing cycle once again.

After all MOE 1 clocks have been decremented, the second link oriented branch of Routine BD is entered. Here all the bus clocks initialized during passage through the first controller oriented branch are decremented once each second. The contents of the bus clock are then compared with preset values which define the end of eligible bus entry periods. As each clock reaches zero, entry to the BPS Algorithm Routine, Routine BE, is flagged. After all bus clocks have been decremented, an exit is made back to the BPS Executive routine.

2.30.3 Repetition Rate

This routine is entered once per second from the Executive Routine.

2.30.4 Cross Reference

This routine is called by and exits to the BPS Executive Routine.

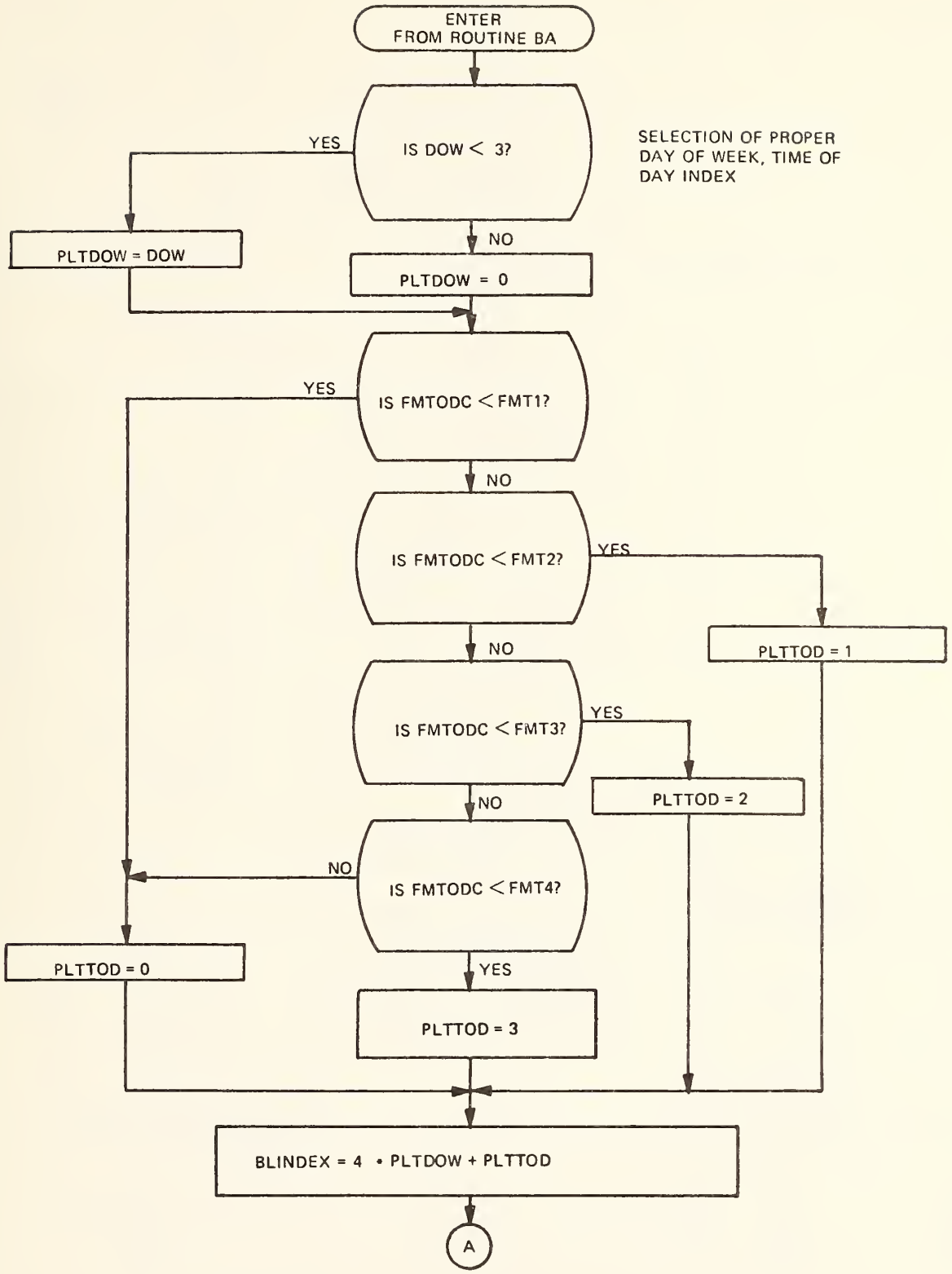

FIGURE 2.30.5.1 ROUTINE BD SPECIFICATION

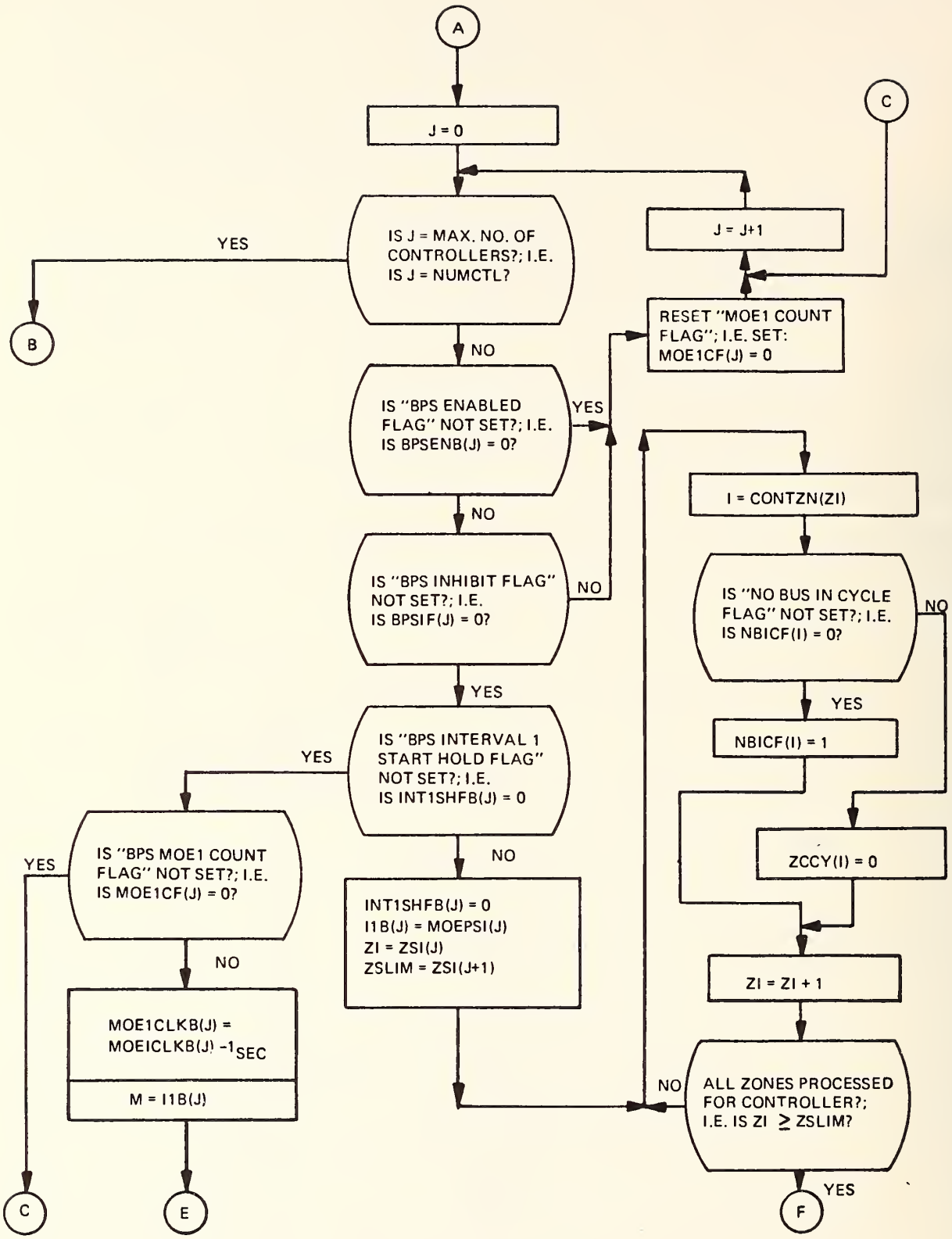

FIGURE 2.30.5.2. ROUTINE BD SPECIFICATION

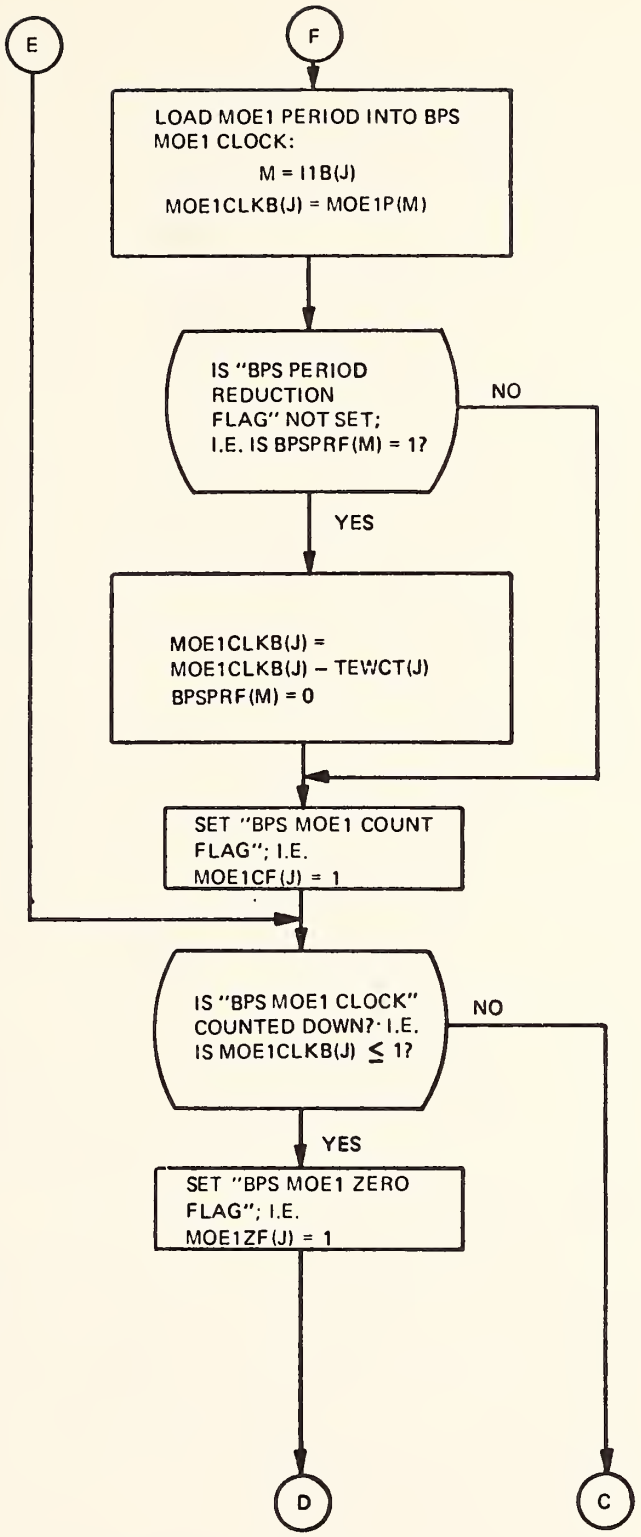

FIGURE 2.30.5.3. ROUTINE BD SPECIFICATION

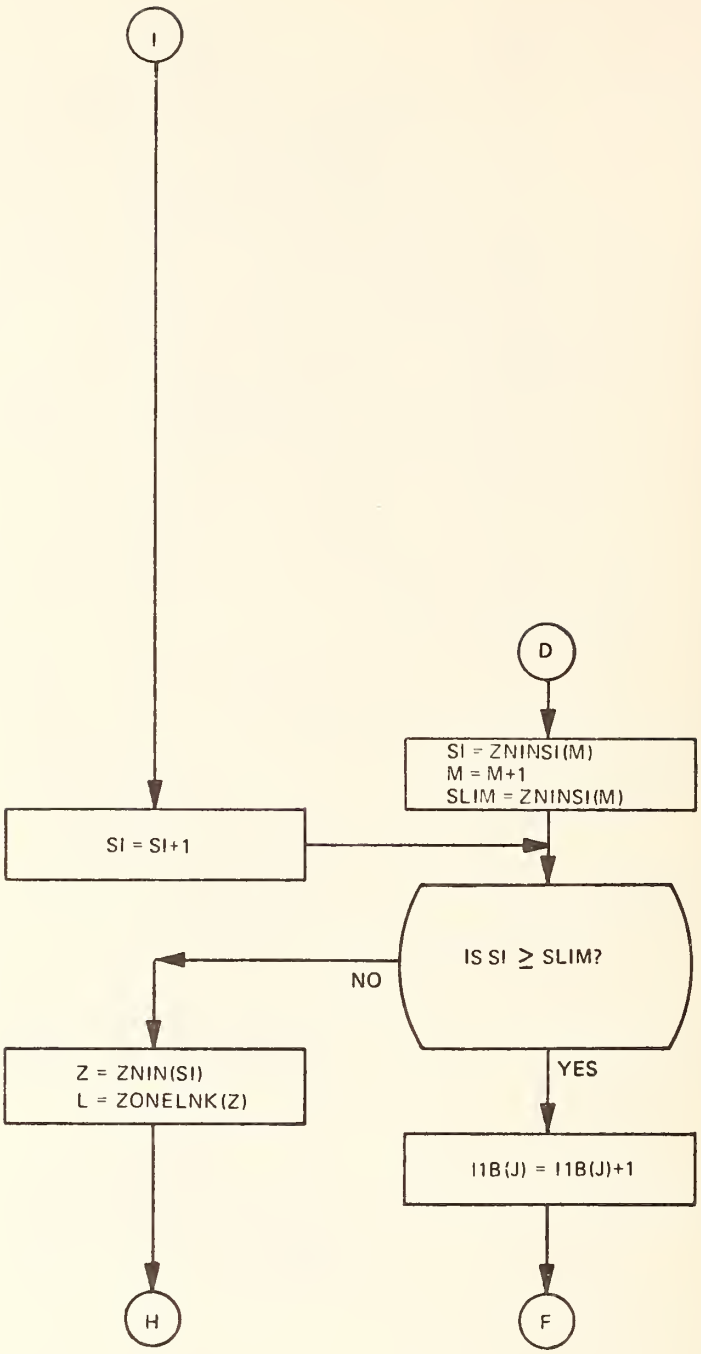

FIGURE 2.30.5.4 ROUTINE BD SPECIFICATION

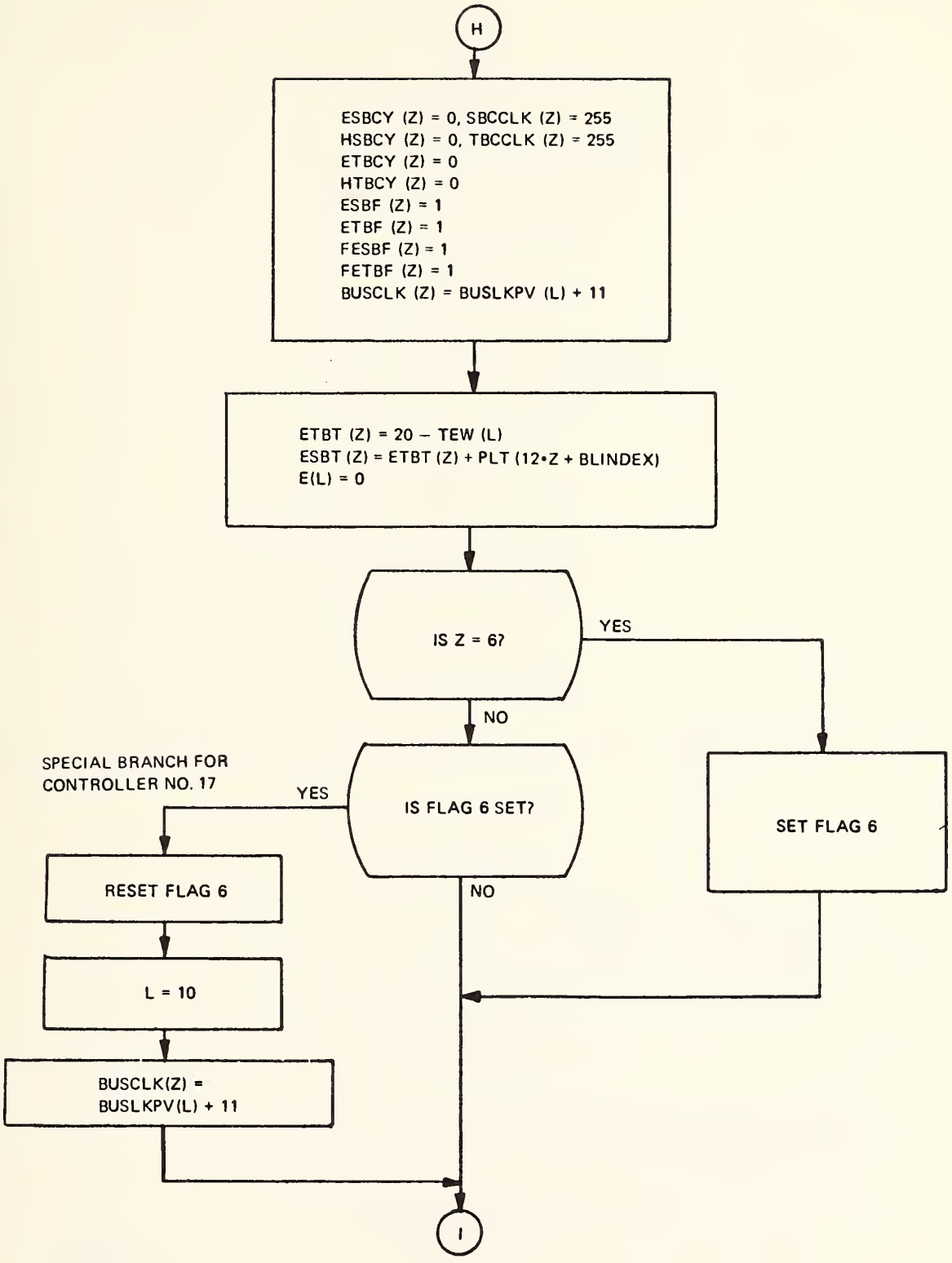

FIGURE 2.30.5.5. ROUTINE BD SPECIFICATION

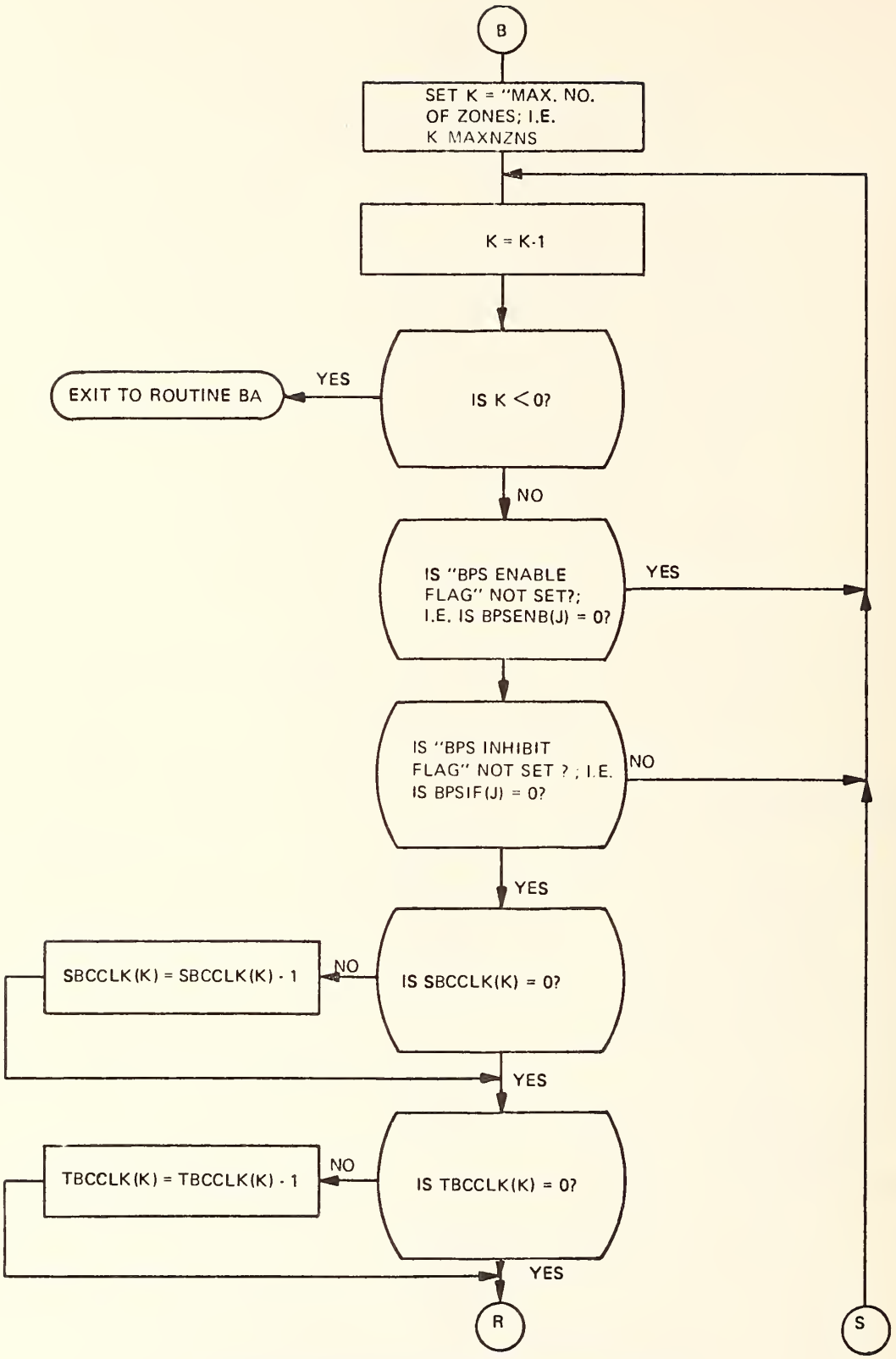

FIGURE 2.30.5.6. ROUTINE BD SPECIFICATION

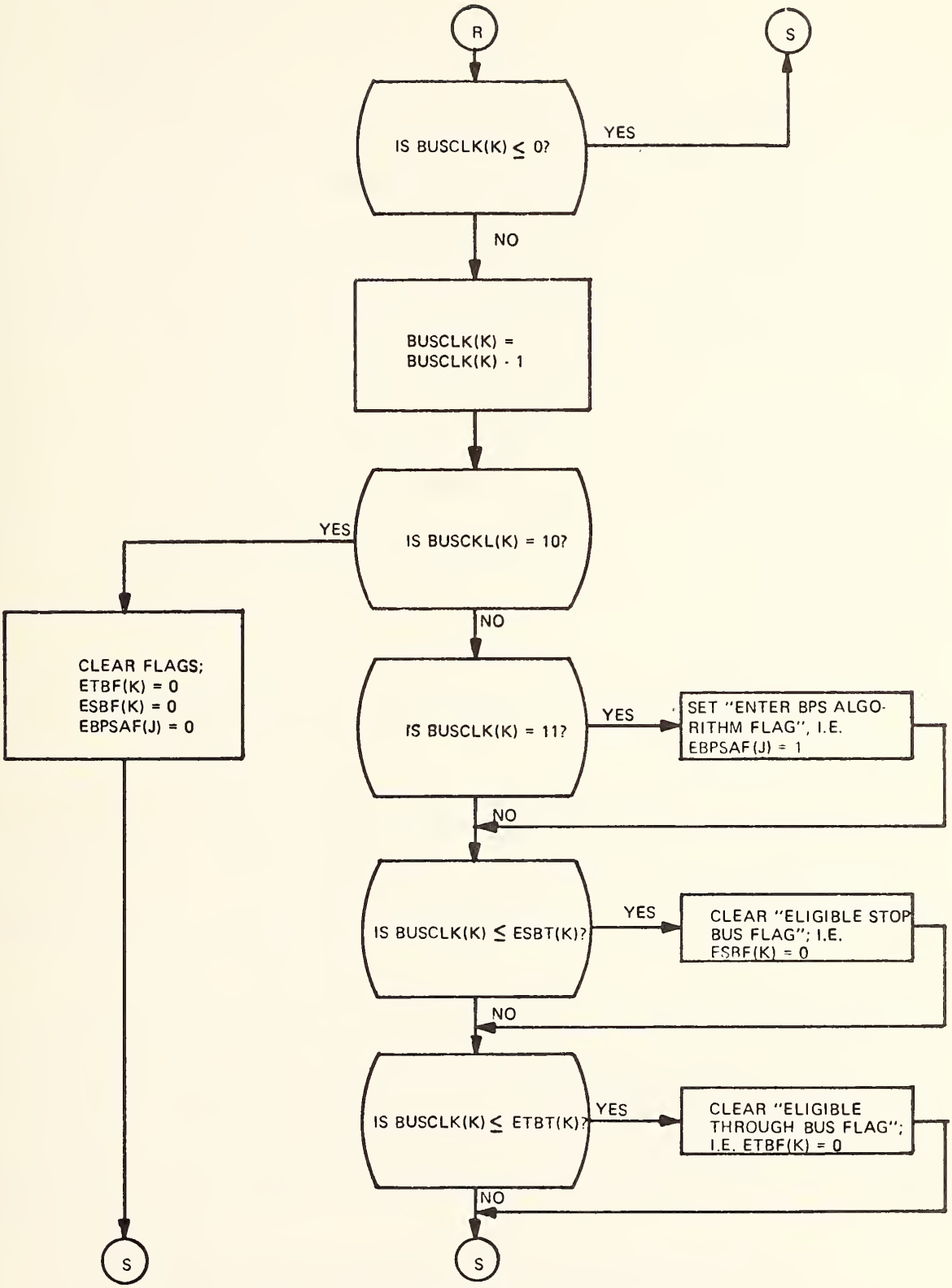

FIGURE 2.30.5.7. ROUTINE BD SPECIFICATION

2.31 Routine BE (BPS Algorithm) Specification

2.31.1 Purpose

The function of this routine is to initiate or overrule a green extension to favor bus traffic at an intersection. The routine determines the value of such an alteration in split one second prior to the start of amber on all links carrying bus traffic into a BPS intersection. (A special circumstance arises for pre-empt operation of BPS. Here, the simple presence of an eligible bus results in a favorable decision for a green extension without resorting to an actual measure of its value.) In normal operation the following conditions must be met to result in a decision favoring a green extension:

- The BPS Enable Flag must be set for the intersection
- The UTCS/BPS inhibit Flag must not be set for the intersection
- One full cycle time must have elapsed since the previous extension at the intersection.
- Cross street queues must not exceed a preset limit (as indicated by UTCS Stop Flag 3)
- Eligible buses are present to take advantage of the green extension
- The intersection gain associated with a green extension must exeeed a preset threshold value.

The request for a BPS extension is made known to UTCS by the setting of the extension flag for all multi detector links which will turn green at the end of the current MOE period. The mechanics of providing the extension are carried out in UTCS Routine D by making the necessary UTCS timing adjustment in accordance with a preset extension interval for each BPS link.

Following the granting of an extension and one second before its expiration, Routine BE repeats the intersection gain calculations. The value computed on this second pass is a more accurate representation of the true worth of the extension because helped rather than eligible bus counts are used and because queue values are updated to those existing at the end of the extension interval. Finally, an apportionment of the intersection gain is made to those links benefiting from the extension on the basis of bus helped counts per link.

The routine is entered once each second from the BPS executive.

2.31.2 Method

Upon entry a series of flags is examined for each controller in succession to determine whether certain of the conditions summarized earlier are satisfied. For each particular controller where this is the case the MOE 1 period index number set by Routine BD is looked up. The going green (GGRN) and going red (GRED) links associated with that MOE 1 period (and any following zero duration MOE 1 periods) are then looked up. The BPS pre-empt flag is checked to see whether an extension should be granted out right. When the pre-empt flag is not set, the possibility of an extension is further examined by entering the Intersection Gain subroutine. (Appendix 4.8 describes the Intersection Gain Algorithm in detail).

The IG value computed in the subroutine is compared against a preset threshold value for the controller. A value lower than the threshold rules out an extension, a higher value results in entering the Link Index subroutine to set the extension flags for the red links and thus signal UTCS for further action. The BPS extension granted clock is also set to the controller cycle length at this time to inhibit additional extensions for that period.

2.31.3 Repetition Rate

This routine is entered every second.

2.31.4 Cross Reference

This routine is called by and exits to the BPS Executive Routine.

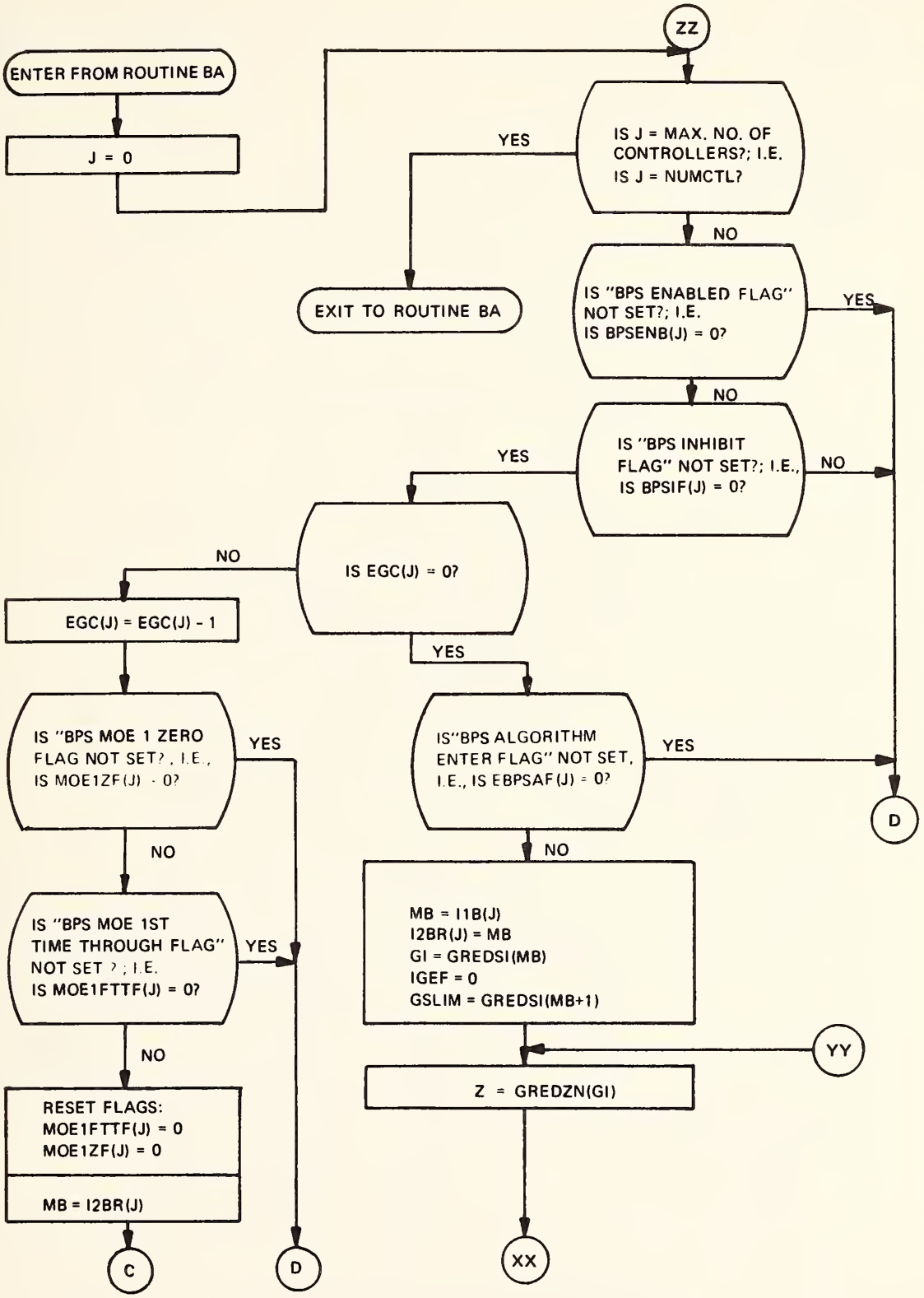

FIGURE 2.31.5.1. ROUTINE BE FLOW CHART

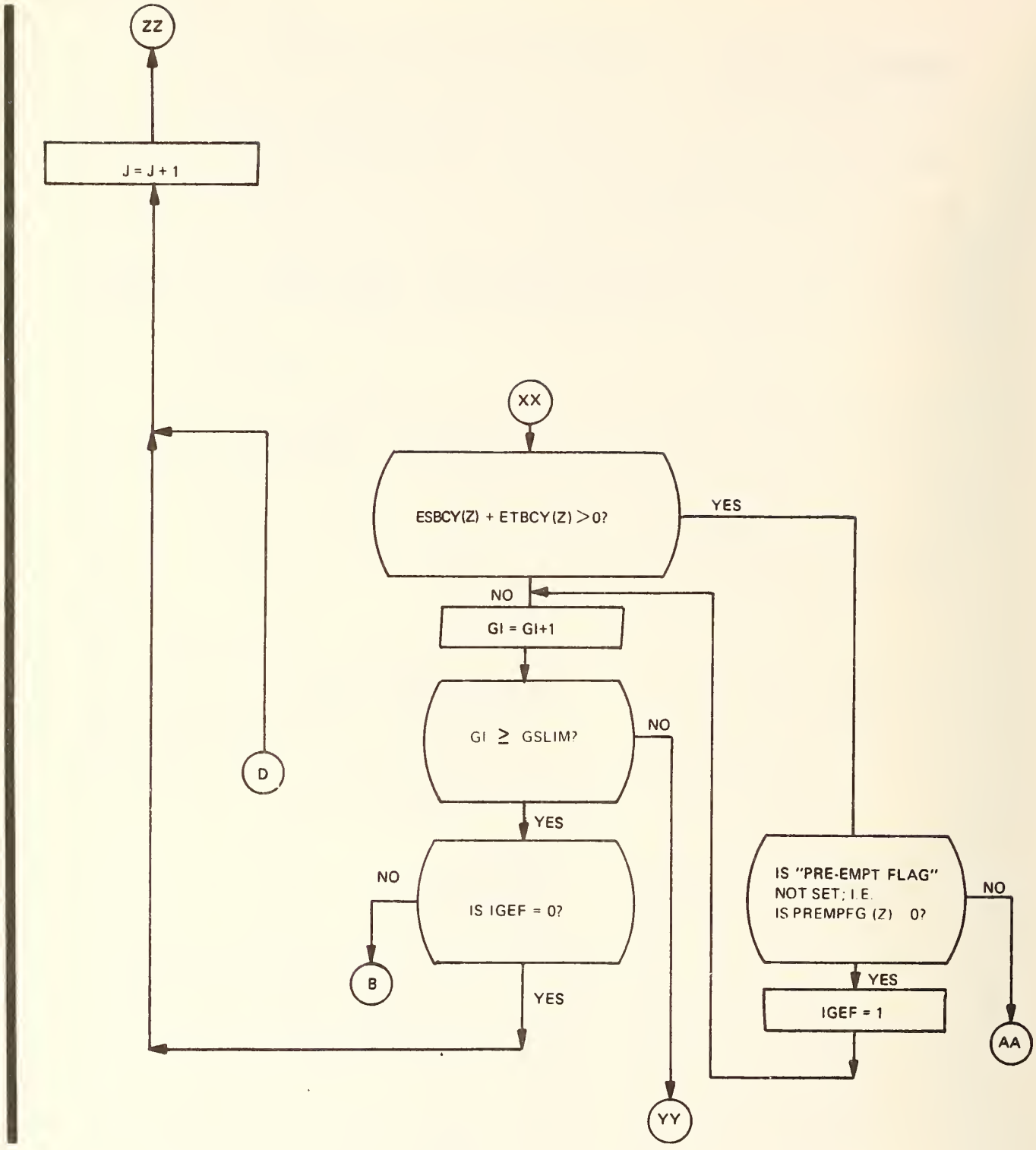

FIGURE 2.31.5.1. ROUTINE BE FLOW CHART

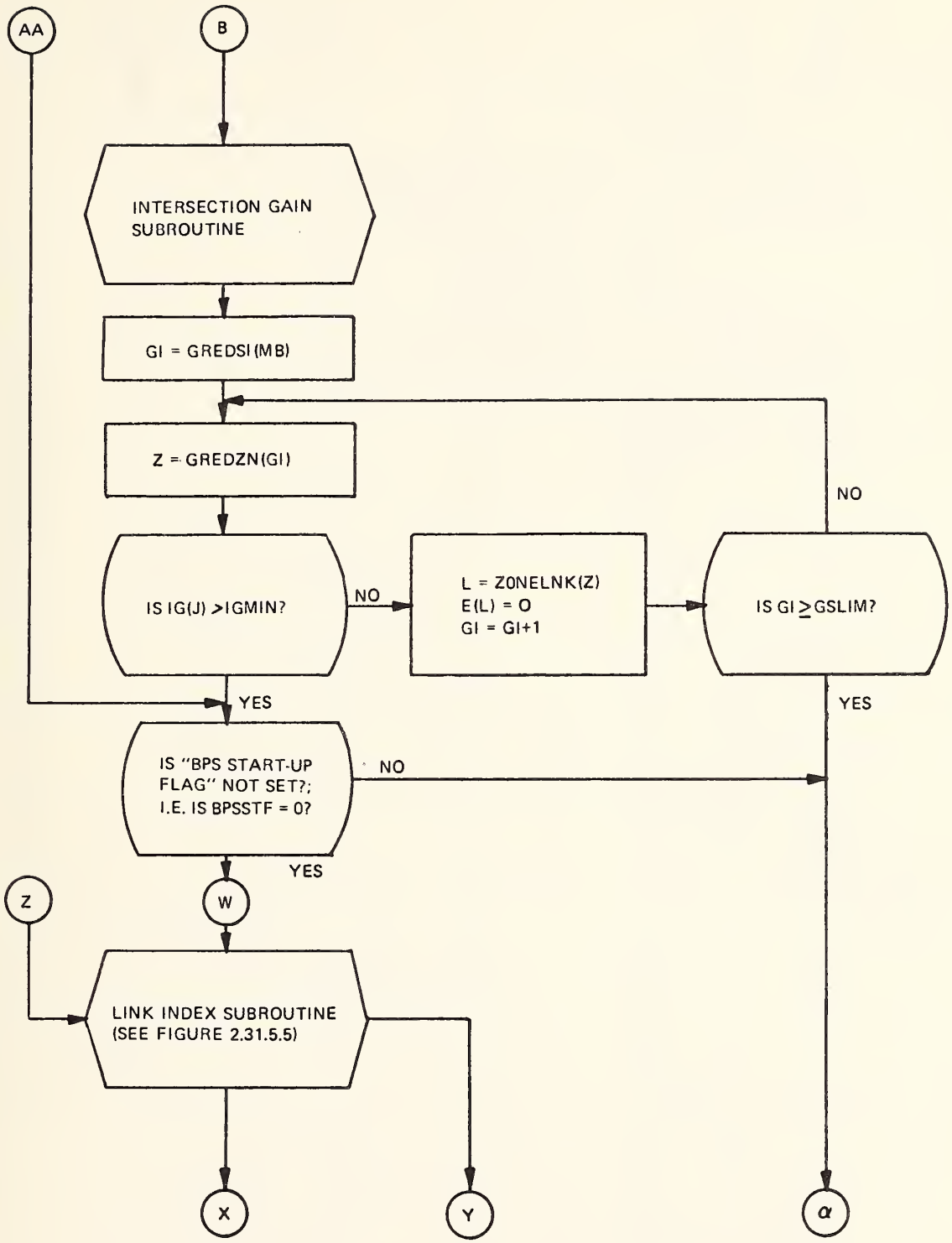

FIGURE 2.31.5.2. ROUTINE BE SPECIFICATION

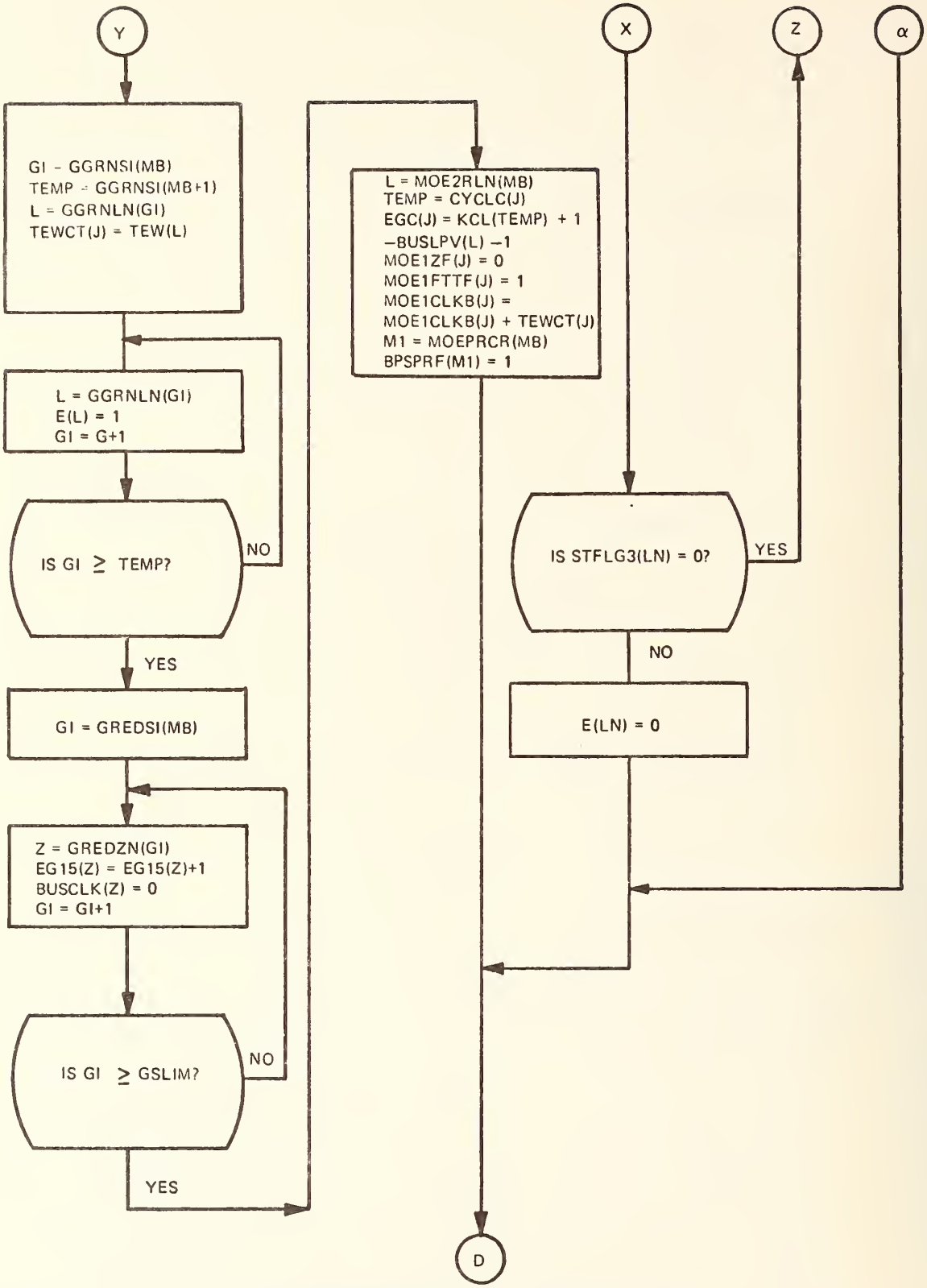

FIGURE 2.31.5.3. ROUTINE BE SPECIFICATION

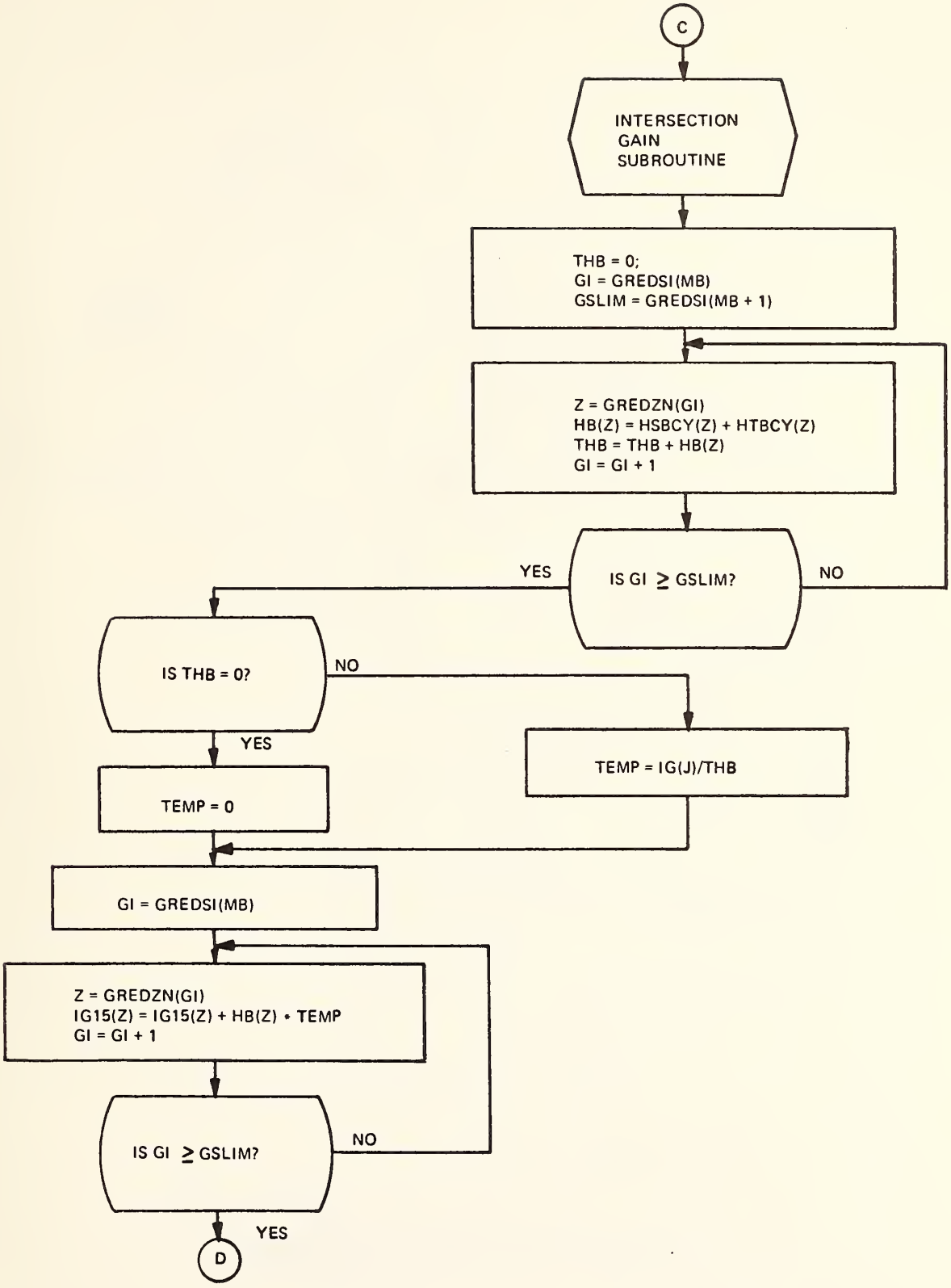

FIGURE 2.31.5.4. ROUTINE BE SPECIFICATION

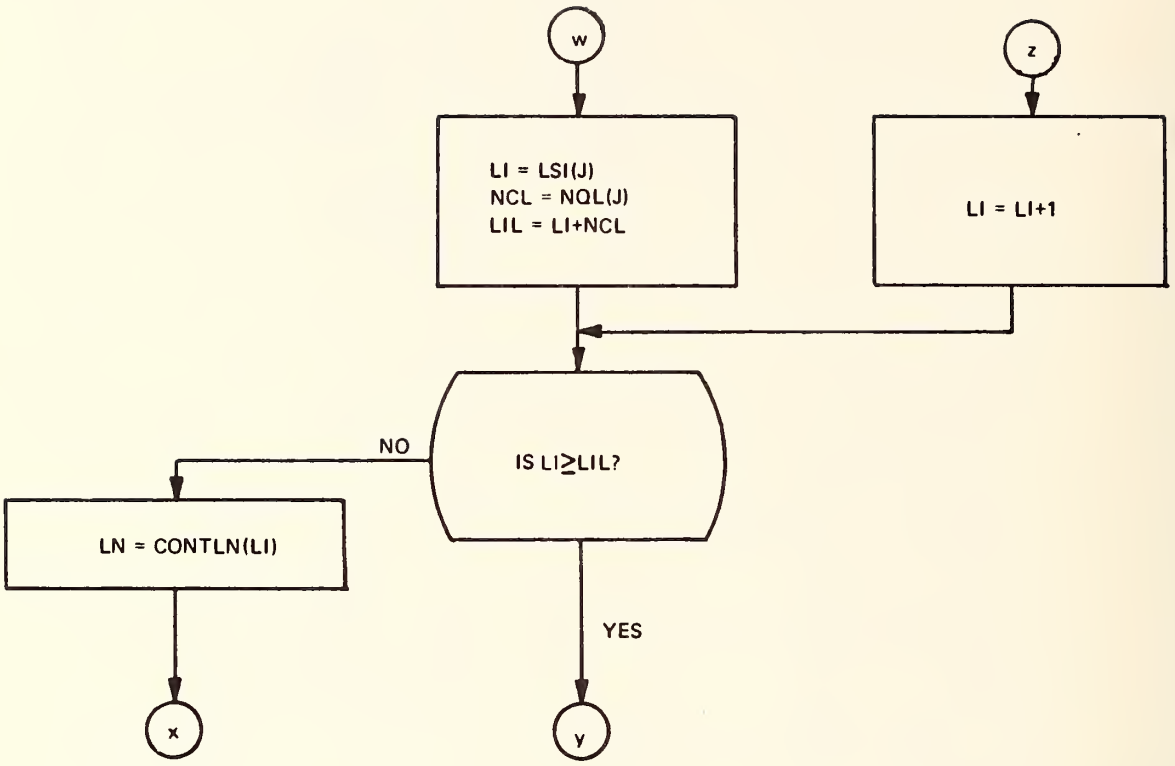

FIGURE 2.31.5.5. ROUTINE BE SPECIFICATION

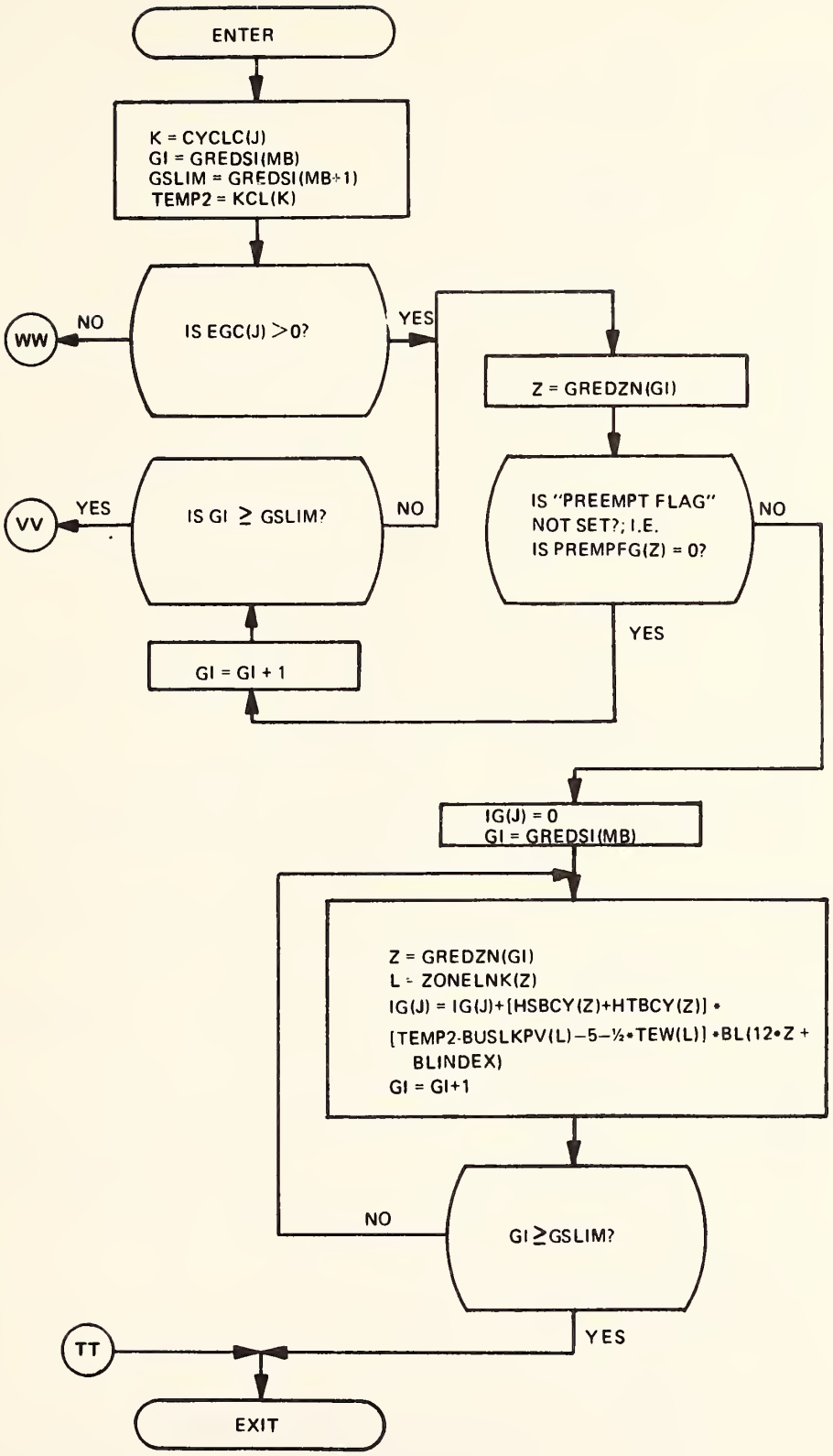

FIGURE 2.31.5.6. INTERSECTION GAIN SUBROUTINE FLOW CHART (ROUTINE BE)

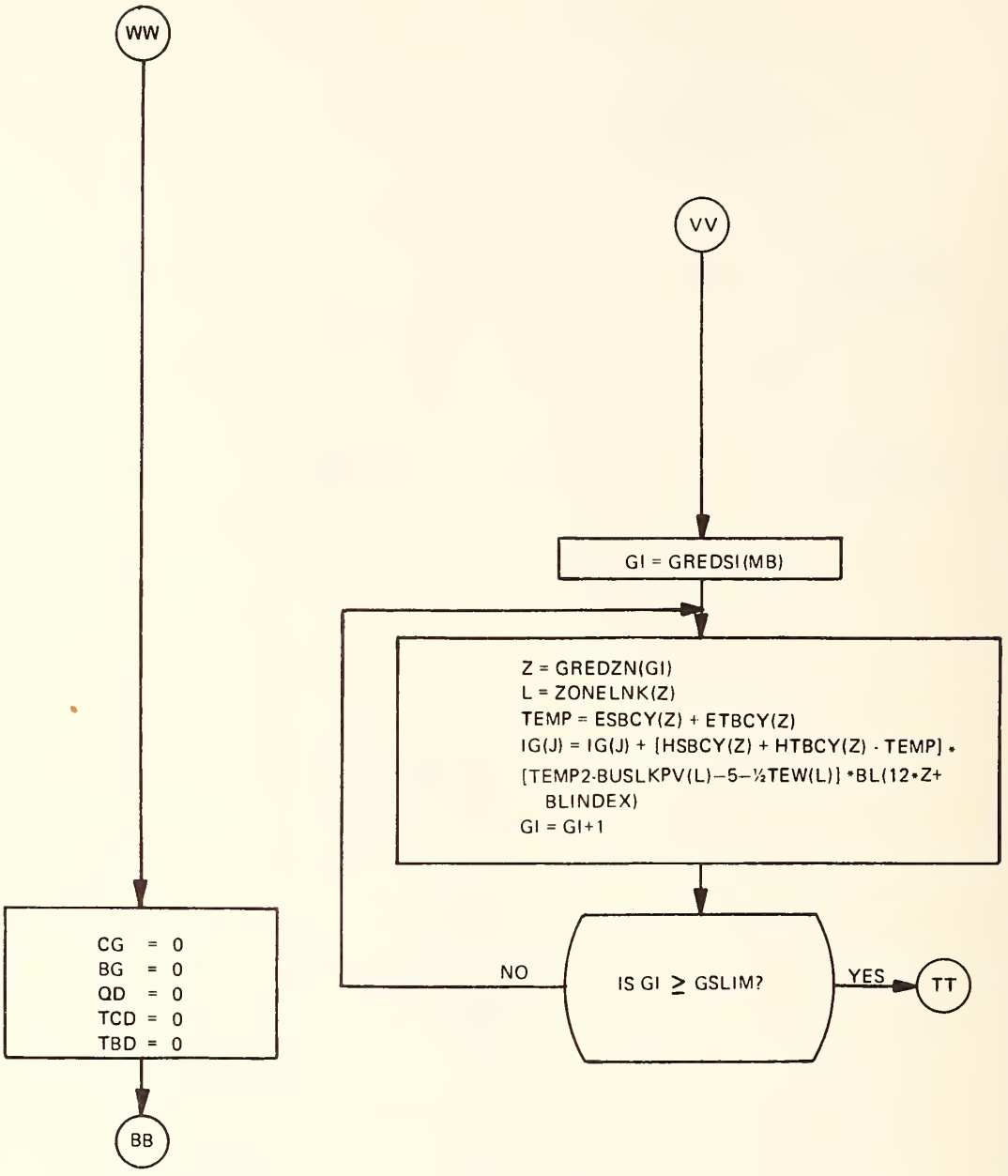

FIGURE 2.31.5.6. INTERSECTION GAIN SUBROUTINE
FLOW CHART (ROUTINE BE)

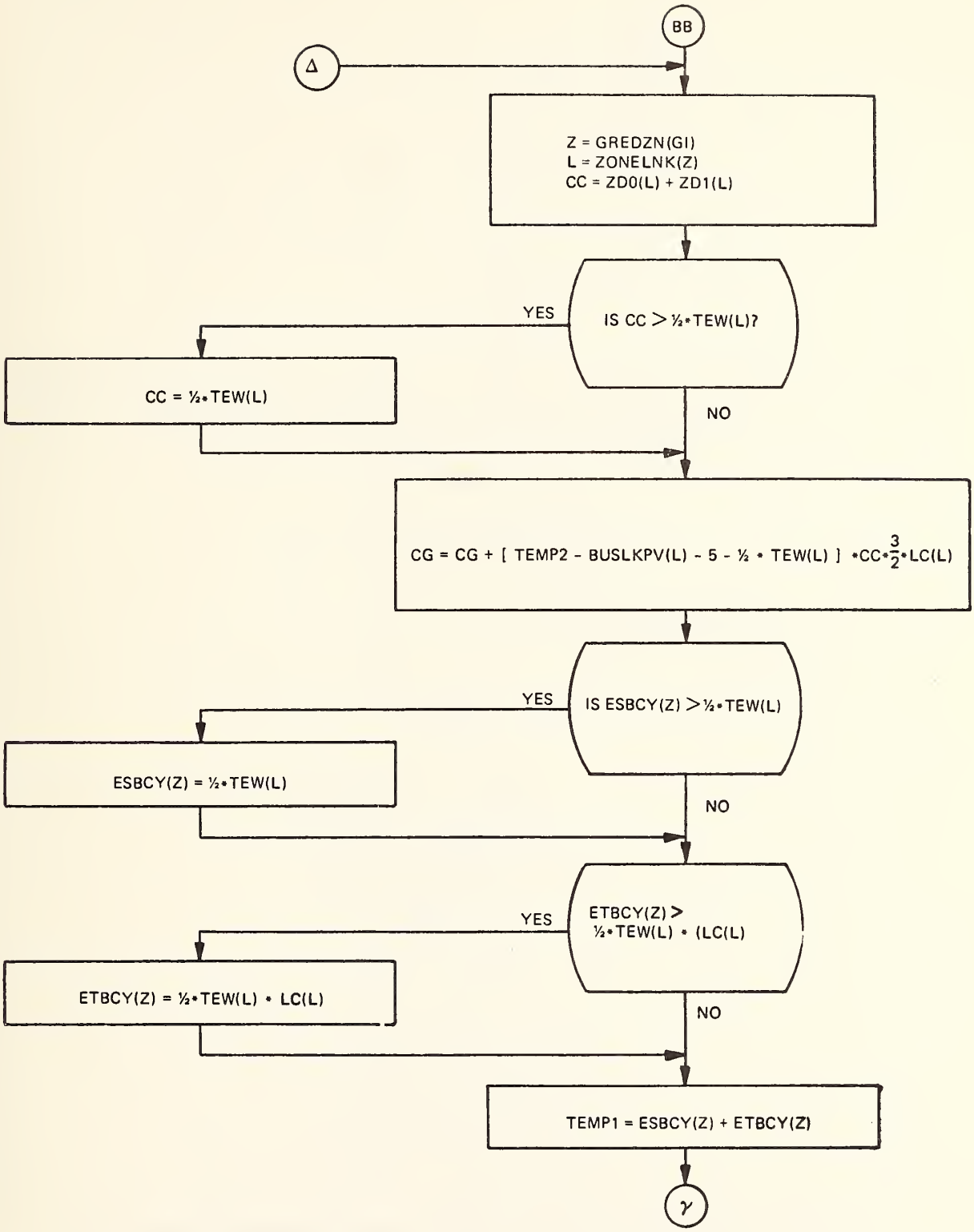

FIGURE 2.31.5.7. INTERSECTION GAIN SUBROUTINE SPECIFICATION (ROUTINE BE)

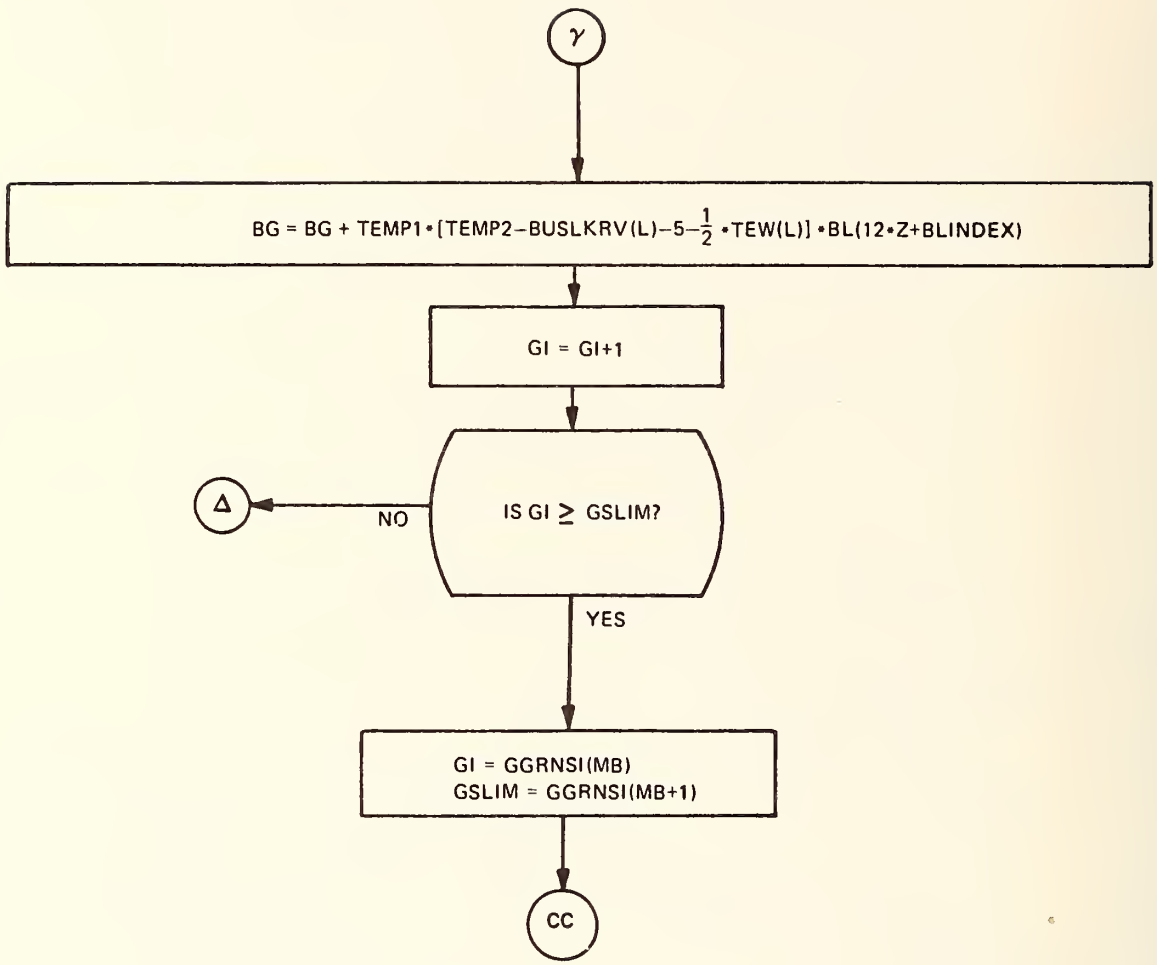

FIGURE 2.31.5.8. INTERSECTION GAIN SUBROUTINE SPECIFICATION (ROUTINE BE)

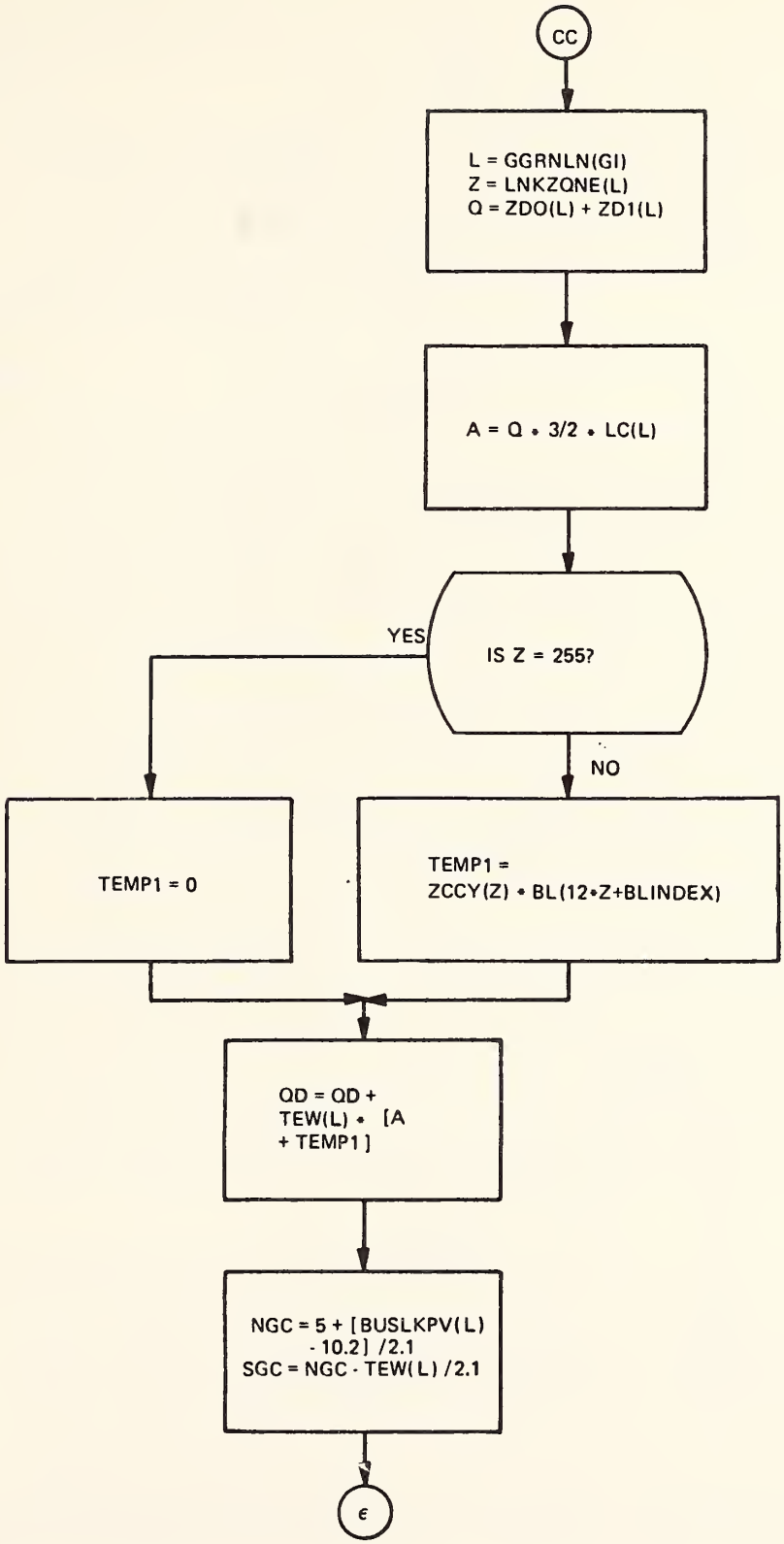

FIGURE 2.31.5.9. INTERSECTION GAIN SUBROUTINE SPECIFICATION (ROUTINE BE)

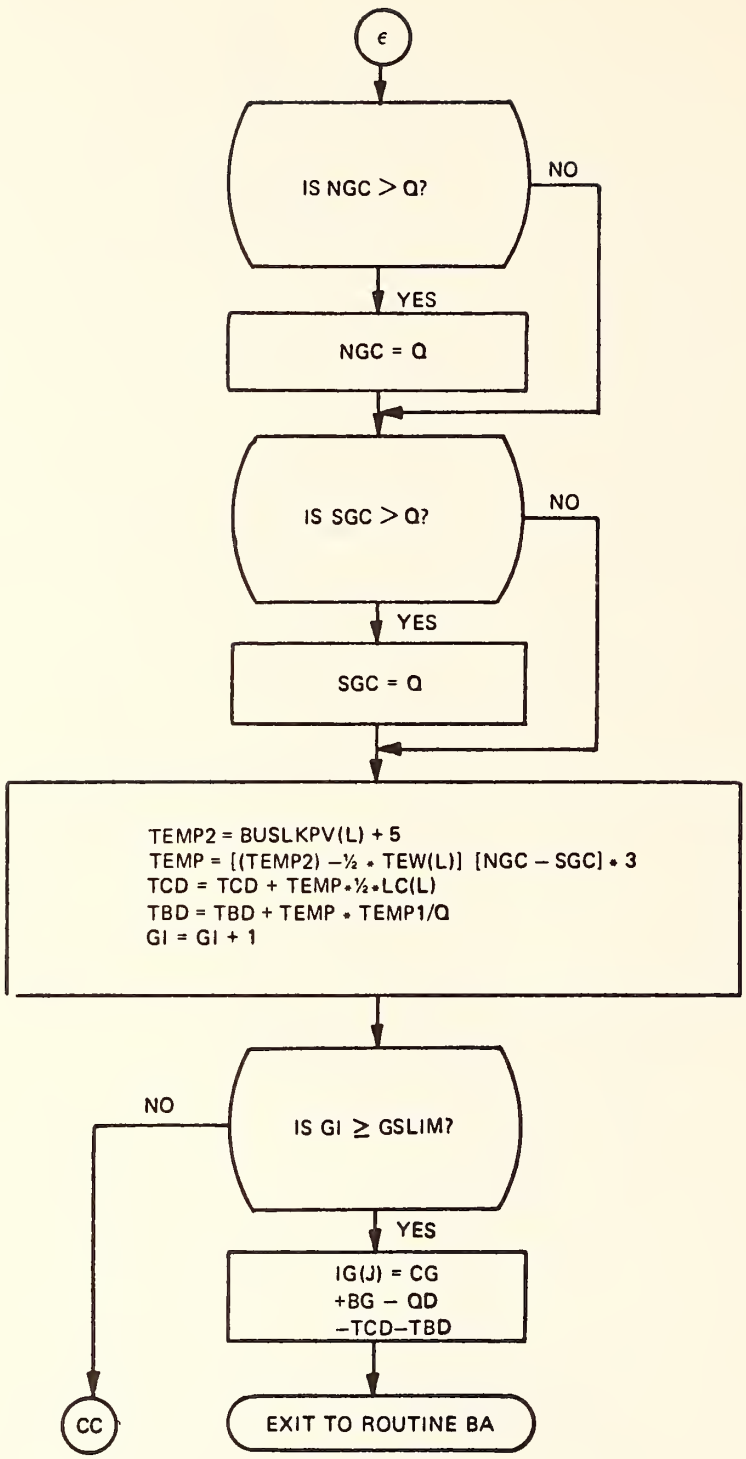

FIGURE 2.31.5.10. INTERSECTION GAIN SUBROUTINE SPECIFICATION (ROUTINE BE)

2.32 Routine BF (BPS Malfunction Detection) Specification

2.32.1 Purpose

The purpose of Routine BF is to scan the BPS failure words to see which bits have been set by routines BB and BC (where failure tests are carried out for communications and detectors). When a failure is indicated, Routine BF collects and stores data, resets the BPS Enable Flag at the intersection involved, sets the appropriate failure bit and sets Routine K active.

2.32.2 Method

Routine BF monitors the BPS detector and communications failure flags set in Routines BC and BB, respectively. When a failure flag is set, a check is made to see if it was present the last time the routine was entered. If it was not, the detector or communications number is stored and Routine K is set active. The BPS enable flag is reset to terminate BPS functions at the intersection involved. The original failure words are saved to prevent repeated response to the same error on the next pass.

BF is entered once each second from the BPS executive. After collecting time reference information, checks are made of each of the BPS failure flags organized in 16-32-bit words. This includes 256 detector failure bits and 256 communications failure bits - providing enough space for both the basic and add-on UTCS installations.

Each failure word is first scanned to see if it contains any failure indications (1's). If the word is zero, the program immediately proceeds to the next failure word. A non-zero word is processed by successive 1-bit left shifts until a negative word is indicated. At this time data processing as already described above is carried out.

Processing continues until either a zero word value remains or the bit index reaches zero. At such time the failure word is cleared and processing of the following failure word is begun. When all failure words are processed an exit is made back to the BPS exec.

Once BPS failures are stored, they will be visible to the operator as follows:

- Map - within 6 seconds or less, providing the failure display is on view (thru the failure bits in the detector and controller status words).
- CRT - within 1 minute or less, providing the failure display is on view (from failure table)

- 15-minute report - within 15 minutes or less, depending on clock time, (from failure table).

2.32.3 Repetition Rate

This routine is called once per second.

2.32.4 Cross Reference

This routine is called by and exits to the BPS Executive Routine.

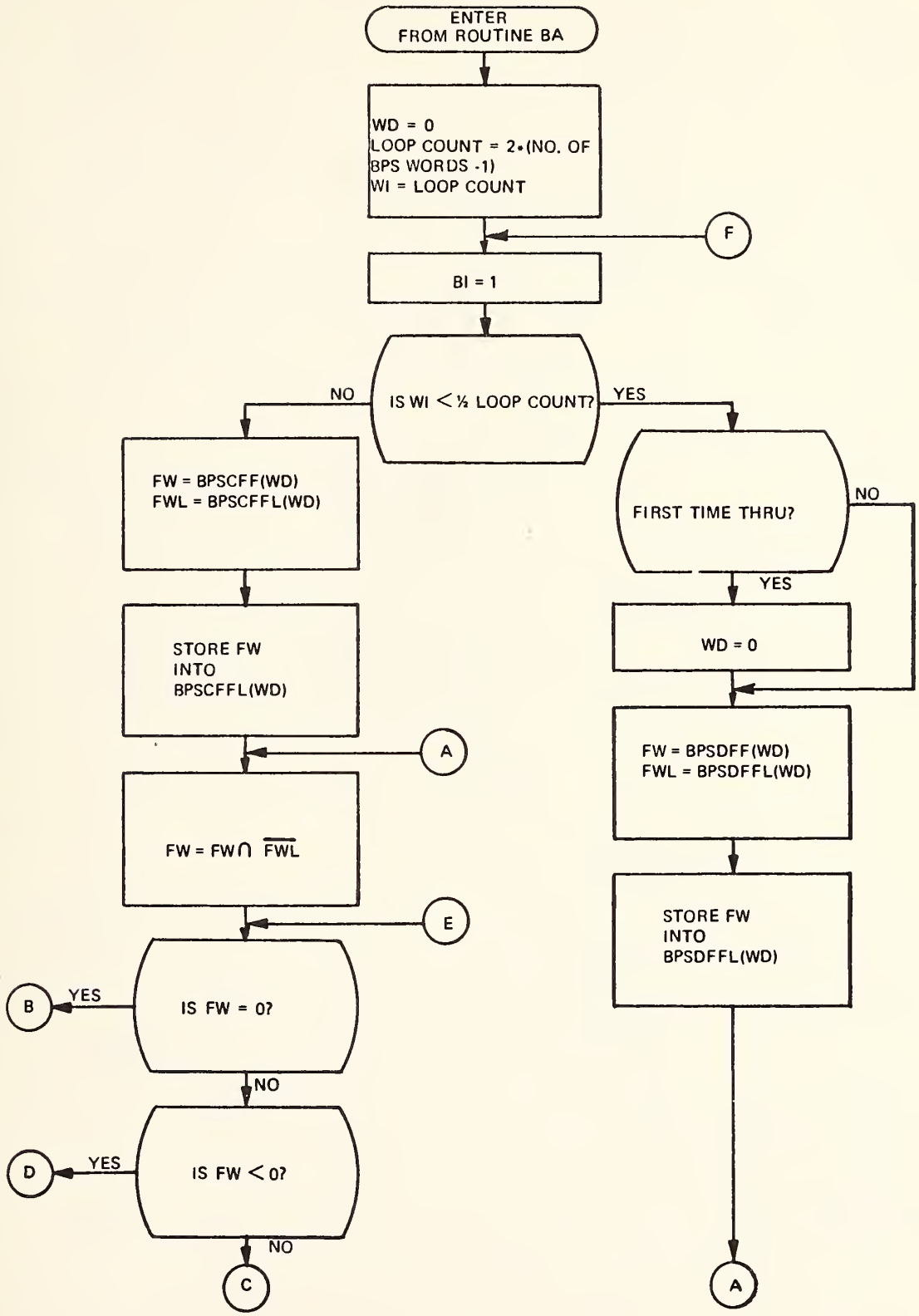

FIGURE 2.32.5.1. ROUTINE BF SPECIFICATION

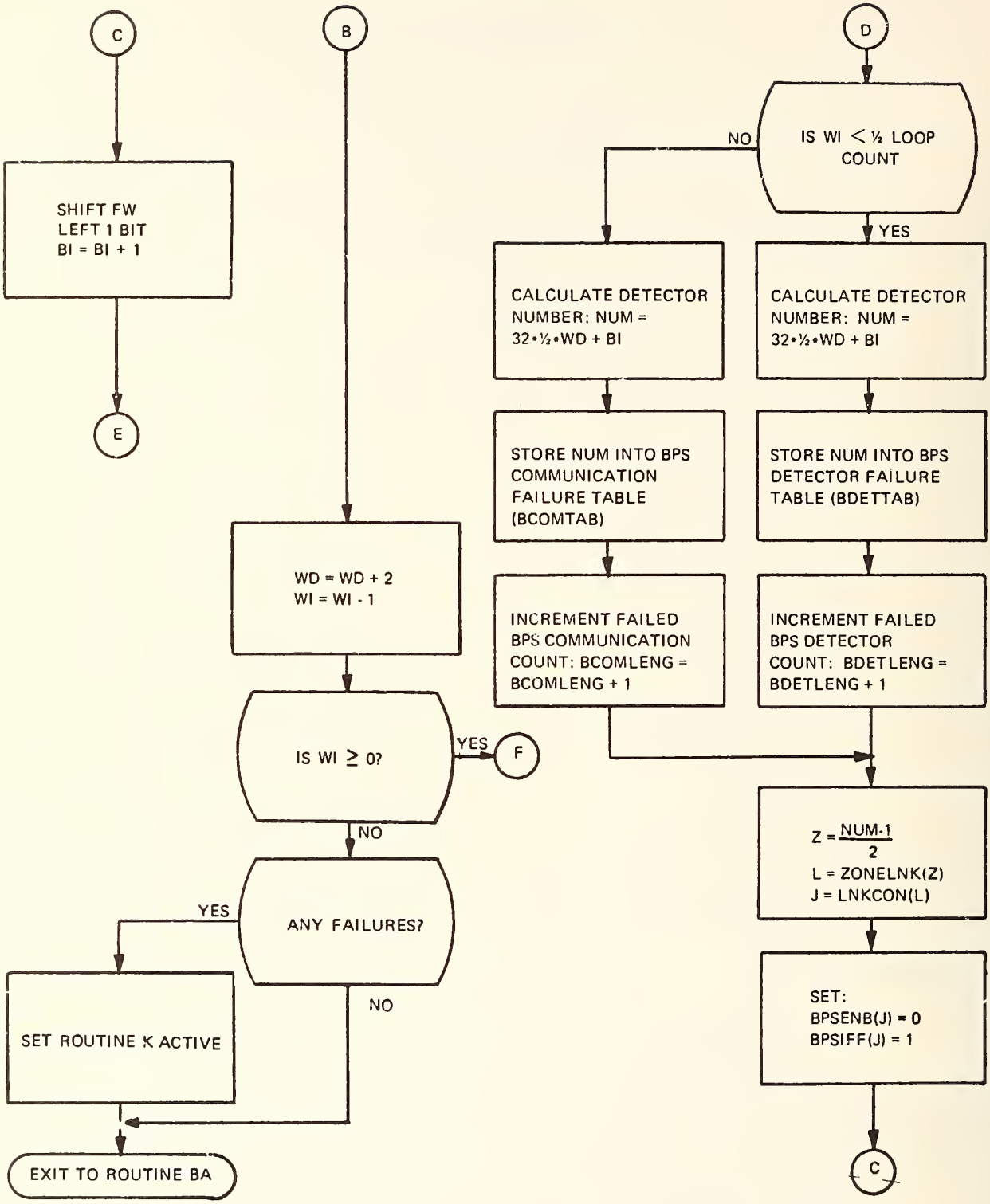

FIGURE 2.32.5 2. ROUTINE BF SPECIFICATION

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